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High-Frequency Circuit Design Oriented Compact Bipolar Transistor Modeling with HICUM

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SUMMARY An overview on the physics and circuit design oriented background of the advanced compact model HICUM is presented. Related topics such as the approach employed for geometry scaling and parameter extraction are briefly discussed. A model hierarchy is introduced, that addresses a variety of requirements encountered during the increasingly complicated task of designing analog and high-frequency circuits.

key words: *bipolar transistors, compact modeling, HICUM*

Most frequently used symbols

A_{E0}, P_{E0}	area and perimeter of emitter window
b_{E0}, l_{E0}	width and length of emitter window
b_E, l_E, A_E	effective electrical emitter dimensions and area
BE, BC	base-emitter, base-collector
EC	equivalent circuit
E_{jc}	electric field at the BC junction
f_T, f_{max}	transit and maximum oscillation frequency
h_μ, h_j, h_e	weighting function components
i_C	(time dependent) collector current
J_{Ti}, J_{Tp}	internal transfer current density, perimeter transfer current per length
μ_n	electron mobility
r_{Bi}, R_{Bx}	internal and external base resistance
R_E, R_{Cx}	external emitter and collector resistance
SCR	space charge region
T, T_j	temperature, junction temperature
v_s	saturation velocity
V_{CEs}	internal CE collector-emitter saturation voltage
V_{DCi}	internal base-collector junction built-in voltage
V_T	thermal voltage

Time dependent currents, voltages and charges are indicated with lower case letters.

1. Introduction

Bipolar transistor technology development in the past 25 years has progressed in leaps: after a period of only incremental improvements, a fundamental change of the device design brought significant improvements of the electrical characteristics and established again the traditionally existing performance gap with respect to CMOS technology. While it was the self-alignment scheme in the early eighties and the introduction of Ge (and C) in the nineties, the most recent improvement in operating speed results from the integration into CMOS mainstream processes. The utilization of advanced CMOS lithography allows not only a tremendous lateral footprint reduction but also more device design alternatives. It is indeed interesting to realize that bipolar technology is actually benefitting from CMOS process development.

The footprint reduction along with the epitaxial growth of SiGe:C base layers have led to an explosive speed increase of heterojunction bipolar transistors (HBTs)* (e.g. [1]–[9]). Values beyond 200 GHz for f_T *and* f_{max} have been obtained consistently (e.g. [1]–[6]), making SiGe-BiCMOS HBT technology attractive not only for mainstream markets such as wireless and wireline telecommunications [10] but also for niche markets such as disc drives, high-performance measurement equipment, and the emerging automotive radar applications (e.g. [11]–[14]). For instance, the system operating frequencies of interest for some of the above mentioned wireless applications are in the range of 24 to 95 GHz.

Designing such high-frequency (h.f.) circuits with confidence requires a process design kit with accurate compact models (and parameters!) for both active and passive devices as well as important parasitic effects [15], [16]. While foundries and EDA system developers have tried to keep up mostly with the directly *design related* demand, getting the *modeling related infrastructure* early enough in place, such as implementing parameter determination methods and test structures as well as integrating adequate models in the simulators, tends to be neglected. On the other hand, mask cost as high as US$ 1 Mio in 0.1 μm-BiCMOS processes increase the pressure to deploy accurate compact models in order to reduce design cost. Saving just one design cycle and its associated mask expense already pays for the annual cost of a typical compact modeling group in industry!

Optimizing circuit performance requires to make compromises regarding the electrical characteristics of transistors by selecting their proper configuration [17]; the latter is defined by emitter dimensions and contact arrangements. Figure 1 visualizes the optimization task for two different types of circuits. In a low-noise amplifier, minimum noise

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*The acronym HBT is used here for bipolar transistors in general, i.e. including homojunction transistors which are a special case of HBTs.

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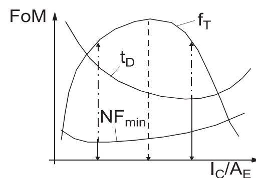


Fig. 1 Circuit optimization requirements (simplified): various transistor figures of merit (FoM) vs. collector current density.

is obtained at much lower transistor current densities than where the f_T peak occurs. Choosing the minimum allowed emitter width, the designer can achieve low noise and high gain *simultaneously* only by varying the emitter length [18]. In "digital" circuits such as frequency dividers and multiplexers, the transistors often need to be driven at high current densities to minimize gate delay t_D. Thus, *simultaneously* achieving maximum speed and low jitter requires a careful selection of the proper transistor *configuration* [14], [17], [19]. Different transistor sizes are generally also necessary in bias circuits. As a consequence of the above discussions, compact models need to be geometry scalable, which means that *every* element in an equivalent circuit (EC) has to be described as a function of the transistor *configuration*.

Both rapid process evolution and h.f. (analog) design specific demands result in a long list of requirements for compact models regarding, e.g., not only the incorporation of important physical and electrical effects but also the model formulation and implementation (e.g. [16]). In addition, design houses demand statistical modeling (and design) capability from foundries. Going even further, foundries are pressed to release well before process qualification compact models that *predict* the targeted performance sufficiently accurately. These goals can only be accomplished by using *physics-based* compact models and extraction strategies.

To meet all the before mentioned challenges, the compact model HICUM has been developed. From designing high-speed fiber-optic circuit components, it was realized in the early eighties (e.g. [20], [22]) that the charge storage description and scalability of the SPICE Gummel- Poon model (SGPM) were inaccurate and inadequate. This spurred the early work on the HIgh-CUrrent Model (HICUM) [20]–[26] and also on a tool for TRAnsistor DImensioning and CAlculation (TRADICA) [27]. Early versions of HICUM were integrated in SPICE2 and experimentally verified for large-signal transient behavior [24]; early TRADICA versions were used to generate scalable model parameters for designing high-speed circuits [17]. Over time, the model has continuously been improved and experimentally verified towards, e.g., charge storage and geometry effects, small-signal high-frequency applications, effects in advanced HBTs and also with respect to noise and distortion applications [28]–[42].

Since new process generations are constantly being developed, compact model development cannot stand still either. Unfortunately, in terms of compact models EDA vendors did not keep pace with the rapid evolution of process technologies until the beginning of this decade. In many simulators, still only the SGPM was offered. This situation has changed now, at least in the Si-based field, as advanced models such as VBIC [43], HICUM and MEXTRAM [44] have been implemented in all relevant simulators. An overview on the simulator availability of HICUM can be found at EDA vendor web sites and [45].

In this paper, the background and features of HICUM are presented from the perspectives of bipolar process technology, circuit design and modeling requirements. Due to the lack of space, the focus will be on Si/SiGe-based vertical NPN structures, although the concepts also apply to PNP devices and most of the existing III-V HBT technologies. Furthermore, since presenting the complete set of equations and their mathematical derivation cannot be accomplished within the scope of a paper, the emphasis is put on providing a guide through the references that are relevant for understanding both the formulation of HICUM and the origin of its associated infrastructure.

2. Vertical Bipolar Transistor Structures

Figure 2 shows the schematic cross-section of a SiGe HBT which shall serve as an example for the discussions in this paper. The cross-section has been partitioned into "modeling-relevant" regions, that are indicated by the different linestyles. Each subdivision can be represented by lumped elements, leading to a physics-based EC. The portion in the dashed box under the emitter is called *internal* transistor. The line in the center of the emitter window corresponds to the one-dimensional (1D) transistor that determines the *intrinsic* (or fundamental) characteristics. The other regions belong to the parasitic *external* structure.

In contrast to MOS transistor structures of the *same* process generation, bipolar and SiGe HBT structures of the *same* generation can differ significantly, depending on the selected process flow. Just for fabricating SiGe HBTs, the combination of, e.g., selective or non-selective layer growth with self-aligning or non-self-aligning BE schemes creates quite a variety of BE structures with different geometrical shape. In addition, the contact arrangement can be very flexible and different isolation schemes are possible (e.g., deep trench, junction isolation), leading to a large variety of configurations adapted for many special tasks. This structural variety has implications for modeling geometry scaling, which just becomes more complicated than for MOS transistors since a geometry scalable HBT model is expected to be applicable to all process technologies, possibly also III-V HBTs with mesa structures.

Besides the configuration, which corresponds to a variation of the lateral structure, the addition of Ge provides options for the vertical device design that are not available for homojunction BJTs. A layer with a lower emitter concentration is now possible, allowing to drastically increase the base doping and reduce the base width (e.g. [6], [8], [33]) without increasing parasitic tunneling currents. Also, sig-

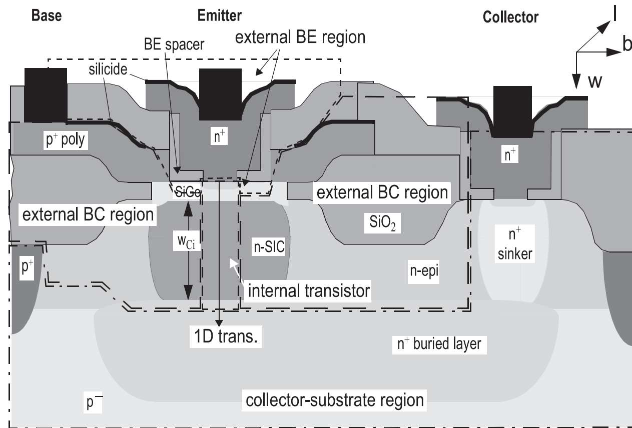


Fig. 2 Schematic cross-section for the example of a SiGe HBT fabricated with selective-epitaxial growth (SEG). In order to enhance the correspondence between the EC and cross-section, the internal nodes have been inserted.

nificant changes in the electrical properties can be achieved by varying (i) the Ge profile itself across the base and in the collector region [47] and (ii) the collector profile using just one mask.

3. Physical Effects

Modern bipolar transistors exhibit many physical effects that are discussed in this section, starting with the intrinsic transistor, which contains the essential features of bipolar transistor action. Then the external transistor regions are considered by means of Fig. 3 and Fig. 4, resulting in the construction of the associated physics-based ECs, which are the basis for a compact model.

3.1 Transfer Current

Consider a 1D line under the emitter window in Fig. 2. Due to the negligible recombination in Si and SiGe transistors (at least for not too low voltages $V_{C'E'}$ or too high current densities J_C), all electrons injected across the BE junction traverse the base and adjacent collector region, causing the transfer current I_T to flow through the collector contact C′. For d.c. operation, I_T equals the (1D) collector current I_C, while for dynamic operation $i_C(t)$ also contains the (out-of-phase) charging components.

According to [33], [48], from the transport equation an exact description of the transfer current is given by

$$I_T = \underbrace{A_E q V_T^2 \mu_{n0r} n_{ir}^2}_{c} \frac{\exp\left(\frac{V_{B'E'}}{V_T}\right) - \exp\left(\frac{V_{B'C'}}{V_T}\right)}{\int_{X_{E'}}^{X_{C'}} h(x) p dx} \tag{1}$$

with the prefactor c not depending on bias. The weighting function

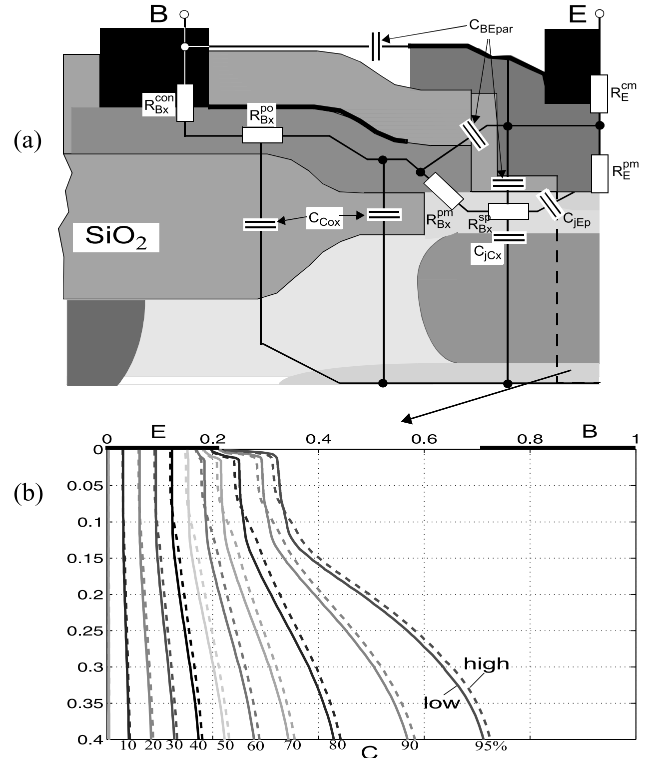


Fig. 3 Zoom-in of the schematic cross-section in Fig. 2: (a) emitter periphery and external BC region, (b) electron current distribution (flow lines) from 2D device simulation of half of the internal transistor structure for low and high bias.

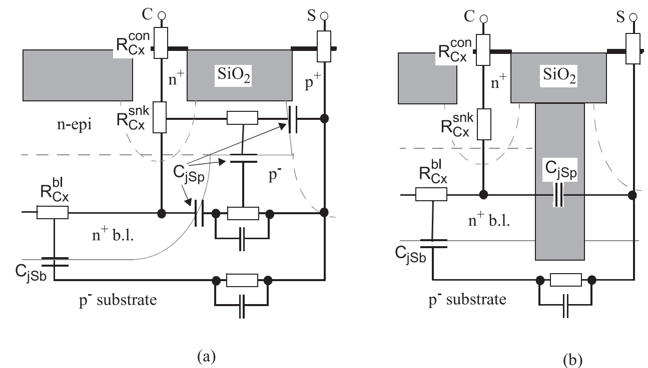


Fig. 4 Zoom-in of the schematic cross-section of the external collector and substrate isolation region with a physics-based EC: (a) shallow field oxide or trench with partial pn-isolation, (b) deep trench isolation.

$$h(x) = \underbrace{\frac{\mu_{n0r} n_{ir}^2}{\mu_n(x) n_i^2(x)}}_{h_\mu} \underbrace{\frac{J_n(x)}{-J_T}}_{h_j} \underbrace{\exp\left(\frac{V_{B'E'} - \varphi_p(x)}{V_T}\right)}_{h_e} \tag{2}$$

with $J_T = I_T/A_E$, can be split into three components. In the 1D case, J_{nx} equals $-J_T$ and the hole quasi-fermi potential φ_p equals $V_{B'E'}$ leading to $h_j = 1$ and $h_e = 1$, respectively. Thus, only the impact of h_μ on the integral in (1) has to be considered. The most important influence comes from n_i via the bandgap variation caused by both unavoidable highdoping effects and intentional Ge profile variation. Notice, that

the integration limits in Eq. (1) represent the 1D emitter and collector contact, thus obviating the complicated description of a bias dependent internal collector resistance for modeling the impact of quasi-saturation.

The hole density p consists of a zero-bias density p_0, which is concentrated in the base region only, and a bias dependent hole density Δp, which can generally be spread over the whole transistor structure. Thus, Δp can be partitioned into its components in the neutral E, B, C region and in the BE and BC space-charge regions. In each region, an average value of the weighting function turns out to be a suitable approximation over bias [25], [48] so that the remaining terms $\int \Delta p dx$ represent the respective depletion and minority charge contribution.

So far, a 1D transistor has been considered. Taking a closer look at Fig. 3(a) shows, that electron injection occurs not only under the emitter but also across the BE periphery junction, leading to an internal and a perimeter current component. Thus, the total transfer current can be written as

$$I_T = I_{Ti} + I_{Tp} = J_{Ti}A_{E0} + J_{Tp}P_{E0}. \tag{3}$$

In principle, one could try to apply a transfer current description such as Eq. (1) separately to I_{Ti} and I_{Tp}. However, first of all, this would lead to a model with two transfer current sources (and related elements); i.e. a 2-transistor model, the complexity of which is desirable neither for circuit design nor for parameter extraction. Also, as the current flow lines in Fig. 3(b) indicate, the assumption of J_{nx} in h_j of Eq. (2) being spatially independent is not quite correct anymore. The same holds for h_e, especially at higher injection levels.

According to Eqs. (1) and (2), mostly the lateral spread of J_{nx} via the weighting function h_j determines the holes and, hence, the charge that has to be included in the denominator of Eq. (1) in *lateral* direction [36]. A first-order approximation is to use in Eq. (1) an effective emitter area defined by Eq. (3) [42]

$$A_E = A_{E0} + \frac{J_{Tp}}{J_{Ti}}P_{E0} = A_{E0}\left(1 + \gamma_C \frac{P_{E0}}{A_{E0}}\right) \tag{4}$$

with γ_C as a constant for a given process that can also be easily measured [50]. As a further approximation, A_E is also used to define the charge components in $\int \Delta p dx$ [24].

3.2 Depletion Charges

According to Fig. 3(a), the total BE depletion charge consists physically of a component related to the bottom junction under the emitter window and one related to the periphery junction. Due to the different doping profiles in these regions, the components behave electrically different. The portion entering the denominator of Eq. (1) is laterally defined (to first order) by A_E.

Similarly, the BC depletion charge consists of the internal component Q_{jCi}, laterally defined by A_E, and an external component. The latter contains a portion given by the SIC extension beyond the effective emitter width and a portion given by the collector-epi background doping. These charges depend on the voltages across the respective junctions. However, the transfer current passing through the SCR also reduces at high current densities the electric field E_{jc} at the BC junction, which causes the respective charge to become current dependent. Since there is very little current spreading in the base and BC SCR, only Q_{jCi} is affected by J_T. In the literature, the current dependence of mostly the associated internal depletion *capacitance* C_{jCi} has been investigated. Unfortunately, most of the proposed analytical approximations for C_{jCi} contain various numerical instabilities and are not integrable, which is required for compact models. A physics-based solution of this problem is to model the charge via the electric field $E_{jc} = Q_{BCi}/(\varepsilon_0 \varepsilon A_E)$, with Q_{BCi} as total internal BC charge. Such a bias dependent description of E_{jc}, that is suitable for compact modeling, was presented in [51], [52] and successfully verified also for $C_{jCi}(V_{B'C'}, I_T)$ [52].

Finally, as Fig. 4 shows, the depletion charge of the CS junction can physically also be partitioned into a bottom and a perimeter portion that are expected to behave electrically different. In case of deep trench isolation, the perimeter component is strongly reduced and behaves more like a plate capacitor.

3.3 Minority Charge

For the following discussion, forward operation of the transistor is assumed. The injection across the BE junction leads to associated electron and hole minority charges in base, emitter and—at sufficiently high current densities—also in the collector region. First, a 1D structure is considered, which is then expanded to the 2D/3D case.

At low injection, the minority charge consists mostly of electrons stored in the base region and can be described analytically by classical transistor theory. The amount of holes stored in the emitter depends on the Ge profile, the junction depth, and the recombination properties of the emitter poly-silicon layer. The corresponding analytical description is quite complicated. An additional component, that causes a time delay, is located in the BC SCR, and is especially important in transistors with a thin base and low collector doping, such as in III-V HBTs and Si/SiGe power transistors.

With increasing current density J_T, the electron density $n = J_T/(qv_s)$ in the BC SCR increases, too, resulting eventually in a compensation of the ionized donor concentration in the SCR. In addition, for lower voltages $V_{C'E'}$ the current through the undepleted portion of the collector causes a voltage drop, that reduces the voltage across the SCR. The consequence is an even faster drop of the electric field at the junction with increasing J_T. This effect was first analyzed by Kirk [53] for BJTs but also occurs in HBTs. Note, that the resulting analytical equation for the BC SCR width is not suitable for compact modeling.

The critical current I_{CK} at which the electric field at

the BC junction has collapsed can be calculated from the condition of either a horizontal field distribution (equaling complete compensation in the SCR) at low $V_{C'E'}$ or—at high voltages—E_{jc} reaching the value $E_{lim} = v_s/\mu_{nCi}$ which separates the ohmic and saturation velocity regime. The consequence of the field reduction and eventual collapse to a very low value is, regardless of BJT or HBT, a more or less strong increase in electron density at the BC junction and the associated charge and transit time. In a BJT this increase is caused by a extension of n and, for charge neutrality reasons, also p into the collector in order to support an additional diffusion current component. In a SiGe HBT, the barrier in the valence band caused by the Ge drop in the BC SCR prevents holes to move into the collector. Instead, they accumulate at the end of the (neutral) base just before the barrier and start forming a dipole layer with the electrons still entering the collector [54]. This results in an electric field in opposite direction to the transfer current flow that forms a potential barrier in the conduction band, limiting the further increase of J_T with $V_{B'E'}$ and leading to a dramatic increase of n with J_T in the base region. The impact of n(J_T) on τ_f and f_T can also be accurately described by $E_{jc}(J_T)$ [52].

So far, the 1D case was considered. According to Fig. 3(b), the injection across the BE perimeter junction also leads to electron charge in the external base region. At low current densities, there is negligible spreading in the base and BC SCR underneath the emitter, so that bottom and perimeter charge can be separated experimentally according to

$$Q_f = \overline{Q}_{fi}A_{E0} + Q'_{fp}P_{E0}. \tag{5}$$

At high current densities, collector current spreading occurs (cf. Fig. 3(b)), indicating a 2D/3D carrier and charge distribution in the transistor. This effect, which depends on geometry and bias ($V_{B'C'}$, I_T), can be described analytically for the general 3D case [42]. As was also shown in [42], the critical current derived for the 1D case has to be modified by a current spreading factor f_{cs},

$$I_{CK} = I_{CK,1D}(V_{C'E'})f_{cs}(b_E, I_E, \delta_C), \tag{6}$$

with δ_C as (average) current spreading angle.

For sufficiently wide emitters (i.e. large b_{E0}) and high current densities, d.c. emitter current crowding occurs (see later), which leads to an increased injection at the BE perimeter junction compared to the bottom portion. Once significant current spreading occurs in both the external base and the collector, it becomes impossible to experimentally separate perimeter and bottom components using Eqs. (5) and (3).

3.4 Base Current Components

The most important base current component is given by the back injection into the emitter. A derivation including all occurring physical effects in detail becomes quite complicated (e.g. [55]) and is not suitable for compact models. As it turns out for Si/SiGe HBTs, the non-ideal effects can be lumped into an ideality coefficient m_{BEi}, yielding a simple relation for the back injection current,

$$I^{E}_{jBEi} = I_{BEiS}\left[\exp\left(\frac{V_{B'E'}}{m_{BEi}V_T}\right) - 1\right]. \tag{7}$$

At very low current densities, the recombination in the BE SCR causes an additional current component I^{SCR}_{jBEi}, that can be described by the same formulation as Eq. (7), but with the parameters I_{REiS} and m_{REi} instead. The same approach applies to the other junction current components.

At high current densities, excess recombination (with the lifetime τ_{Bhrec}) within the dipole layer at the BC barrier causes the base current to increase more rapidly due to the accumulation of carriers there. Denoting the resulting excess base charge by ΔQ_{fB}, the corresponding base current component can be approximated quite well by [56], [57].

$$i_{Bhrec} = \frac{\Delta Q_{fB}}{\tau_{Bhrec}}. \tag{8}$$

3.5 Series Resistances

The holes flowing from the external base region into the internal transistor supplying the internal base current components cause a (time or frequency dependent) distributed voltage drop in parallel to the emitter junction. For d.c. operation, this voltage drop can be represented by a lumped internal base resistance r_{Bi}. At high current densities, the lateral voltage drop across r_{Bi} can lead to current crowding at the emitter perimeter edge. While this effect is negligible in advanced transistors with narrow emitter stripes and fairly low internal base sheet resistance, it can become relevant for power transistors due to their larger emitter width and is very pronounced at highfrequencies or for fast transient operation (e.g. [19], [32]).

Under the assumption of negligible d.c. emitter current crowding a lumped representation of the internal base impedance z_{Bi} is possible also for *small-signal* h.f. operation (e.g. [32], [59]). However, for *large-signal switching* operation no closed-form analytical solution exists. In this case, at least a 2-transistor model is required [58] to approximate the distributed character of the (dis-) charging process of the internal transistor with reasonable accuracy. In summary, the internal base resistance is one of the most difficult elements to describe in compact analytical form, since it depends not only on geometry, bias and temperature but also on the transistor *operating mode*.

As shown in Fig. 3, the external base region can be represented physically by a series of resistors with different sheet resistance values and geometry dependence. In modern processes, often the contribution of the link region under the spacer dominates. Similar considerations apply to the external collector resistance, that consists of three physically different components. In practice, the contact and sinker portion are lumped together into a single areaspecific value since they cannot be distinguished experimentally. The emitter resistance can consist of a series of single

components representing mostly the contact resistance between the layers of the emitter material stack.

Finally, the connection between the SCR edge of the CS junction is connected to a substrate contact somewhere on the surface through a substrate *impedance*, consisting of a network with resistors and capacitors in parallel for each electrical path (cf. Fig. 4). The capacitor represents the permittivity of the substrate. For the most simple structure of a trench-isolated transistor and not too high frequencies, a single substrate resistance may be adequate, which still has a complicated geometry dependence though.

All external series resistances depend on temperature and geometry, while their bias dependence is negligible.

3.6 Self-Heating and Thermal Effects

The high speed of modern SiGe HBTs can only be achieved at fairly high current densities and, hence, at the expense of high power dissipation. The latter, which occurs mostly in the internal BC SCR, leads to an increase of the device operating temperature above chip temperature. This effect, called self-heating, can cause device and circuit failure if it is not properly being taken care of during circuit design. Therefore, self-heating needs to be taken into account in a compact model.

According to [61], the temperature T peaks close to the BC junction. While it drops quickly towards the substrate, only a small decrease is observed at the surface due to the shallow junctions. As a consequence, the temperature T_j at the BE junction,which controls the transistor characteristics, differs only slightly from the peak. This difference depends somewhat on the emitter width and metallization [60].

In a compact model, the spatial temperature distribution cannot be described directly but has to be represented by a lumped approach. This is usually done by employing the similarity between the heat and the continuity equation, allowing to represent the solution of the heat equation by an infinite lumped RC network driven by a current source for the generated power in the device. In steady-state, often a single thermal resistance element, R_{th}, is used to calculate the temperature increase at the BE junction. Obviously, due to the inhomogeneous lateral temperature distribution over the BE junction plane, R_{th} corresponds to an average value. This also holds for C_{th} during dynamic operation. As investigations have shown, for an accurate description of the transient behavior at least a 2-pole network is required [61], [62].

Note, that the thermal time constants are much larger than the usual electrical time constants. This leads to "memory"-like effects for certain types of circuits (such as laser drivers), in which transistors can spend a long time at a d.c. bias point before they switch.

3.7 Other Effects

Increasing transistor speed is also being achieved by shorter and higher doped collectors, resulting in a reduction of the breakdown voltage. The associated avalanche effect limits the transistor operation voltage $V_{C'E'}$, especially at higher collector current densities. If breakdown-sensitive transistors in circuits (such as power amplifiers) are driven by a fairly low source resistance and are operated at high current densities, the avalanche current i_{AVL} causes a reversal of the current direction through r_{Bi}. As a consequence, in a real transistor the highest voltage $V_{B'E'}$ and injection occurs then in the center of the emitter window. This so-called 3D pinch-in effect was shown in [63] to be the dominant failure mechanism in critical transistors of high-speed circuits.

If the intrinsic transistor is operated at very high frequencies or switching speed, the minority carriers experience a delay w.r.t. their controlling voltage. This delay is called non-quasi-static (NQS) effect. As a result, at forward operation the transfer current $i_T(t)$ and minority charge $q_f(t)$ do not anymore follow immediately their controlling voltage $V_{B'E'}$. Since the NQS effect can become important in certain circuits [64], it needs to be taken into account properly. Theoretically, for small-signal operation the NQS effect can be described by an infinite series in frequency for the input admittance y_{11} and the transconductance y_{21} [65]. However, this representation in frequency domain is suitable neither for compact models nor for large-signal transient operation. By limiting the solutions to their respective first-order term, they can be converted to different representations in an EC, that are suitable for both frequency and time domain analysis [32], [66], [67]. The first-order approximation of the exact NQS solution is sufficient for practical applications, since the external transistor's low-pass behavior reduces the signal speed at the terminals of the intrinsic transistor, and the frequency corresponding to the next pole is about three times the f_T of the intrinsic transistor (for a box profile).

4. HICUM Formulation Overview

Based on the discussion in the previous section, a physics-based EC and associated set of model equations can be "constructed" that define the standard version 2.2 of HICUM/Level2. Due to the lack of space, only the most important equations can be given. For a complete description of the model the reader is referred to [45], [46]. In the following sections, the model equations are split into bias, temperature and geometry dependence.

4.1 Equivalent Circuit

Each of the regions in the cross-sections of Fig. 2 to Figure 4 is represented in the EC in Fig. 5 by a corresponding network, indicated again by the different linestyles.

The internal transistor determines the fundamental transistor characteristics and is represented by a transport model. The definition of the effective emitter area (and associated width and length [42]) in Eq. (4) allows to include the perimeter contributions with a single transfer current source and a single minority charge source. The BC avalanche and a possible BE tunneling effect are taken into account by the

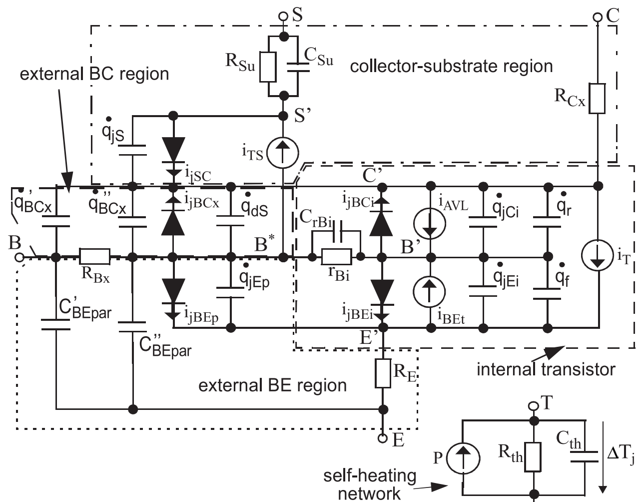


Fig. 5 Equivalent circuit of HICUM/Level2 version 2.2. The sources $\dot{q}$ indicate time dependent currents from nonlinear charges; linear charges are indicated by the notation C.

controlled current sources i_{AVL} and i_{BEt}. The lumped internal base impedance, consisting of r_{Bi} and C_{rBi}, represents the distributed voltage drop under the (effective) emitter accurately for d.c. and for h.f. *small-signal* operation.

The external BE region includes the remaining portions of the depletion charge and base current related to the emitter perimeter junction. The various base resistance components in Fig. 3 are lumped together into a bias independent resistor R_{Bx}. Similarly, the emitter resistance R_E contains all contributions from the material stack. The parasitic isolation capacitance of the BE spacer and contact metal studs is taken into account by a constant capacitance C_{BEpar}. In modern processes with shallow emitter junctions, the latter is often larger than the perimeter depletion capacitance. Depending on the process though (i.e. spacer shape, link region resistance), C_{BEpar} can be split across R_{Bx} to enable an accurate modeling of the input impedance.

The external BC region contains as most important component for typical applications the BC charge Q_{BC}. The latter includes the nonlinear depletion components of the various BC junction regions with different (collector) doping concentrations and a bias independent parasitic capacitance that represents the shallow trench and BC contact metal studs. The distributed character of the external BC region, visualized in Fig. 3(a), is approximated by a π-EC with the total capacitance (and charge q_{BCx}) partitioned across R_{Bx}. This has turned out to be sufficient for practical applications and corresponds already to one additional pole in the input network compared to conventional models such as the SGPM. If the BC junction is strongly forward biased, e.g. at hard-saturation operation in a power amplifier, holes are injected into the lightly doped external collector region. This causes not only an additional base current, i_{jBCx}, and minority charge, q_{dS}, but possibly also the parasitic (pnp) substrate transistor to turn on (see below).

For typical transistor operation, the EC of the collectorsubstrate region consists only of its nonlinear depletion charge, q_{jS}, the external collector resistance, R_{Cx}, and a substrate network (R_{Su}, C_{su} in the most simple case). All these elements are simplified lumped representations of the physically distributed character of the structure. At very high frequencies, a more sophisticated network may be necessary (e.g. [68]) which can be realized by an external subcircuit. For a highly forward biased BC junction in a structure in which the lightly doped collector touches the substrate, a parasitic substrate transistor transfer current i_{TS} can start flowing. In critical applications, this can always be avoided though by a surrounding collector sinker with sufficient high doping at the bottom, since the highly doped buried layer leads to a current gain $i_{Ts}/i_{BCx} < 1$.

4.2 Bias Dependence

In this section, the background of the most important equations employed in HICUM/Level2 to describe the bias dependence are discussed. For a complete set of equations see [45]. To make the model suitable for circuit simulators, all current and charge formulations are continuously differentiable, giving at least continuous first-order derivatives (i.e. conductances and capacitances), but in many cases also high order continuity.

Since dynamic operation is the most important application for bipolar transistors, it is useful to start with the charges. The classical equations for depletion charges (Q_j) have been extended to include the physical effects of a finite charge at high forward bias and of a possible SCR punchthrough at reverse bias. The associated depletion capacitances (C_j) in HICUM exhibit a maximum value at high forward bias which is consistent with the method for experimental determination of the (forward) transit time. The total forward minority charge in the transistor is given by

$$Q_f = \int_0^{I_{Tf}} \tau_f(I) dI. \tag{9}$$

A physics-based formulation is employed for the respective forward transit time τ_f, that combines the bias dependent components of the various structural regions in the transistor in a compact analytical form [35]. The occurring physical effects depend on the *effective* collector voltage

$$V_c = V_{C'E'} - V_{CEs} \cong V_{DCi} + V_{C'B'}, \tag{10}$$

a smoothed formulation of which (around V_{CEs}) is also being used in the model. τ_f can be split into a voltage only dependent component, $\tau_{f0}(V_c)$, and a current and voltage dependent portion, $\Delta\tau_f(I_{Tf}, V_c)$. The possible voltage behavior of the low-current portion τ_{f0} is shown in Fig. 6(a). For high-speed transistors, the collector is highly doped and the reduction of the base width with increasing $V_{C'B'}$ (Early effect) leads to a decrease in τ_{f0}. In contrast, high-voltage (power) transistors contain a wide lightly doped collector. Thus, τ_{f0} increases again towards higher $V_{C'B'}$ once the transit time through the wide BC SCR starts to dominate. This

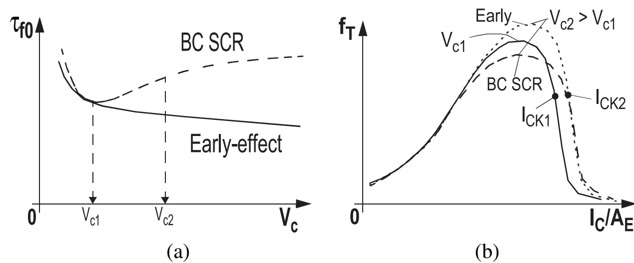


Fig. 6 (a) Low-current transit time vs. collector voltage. (b) Transit frequency vs. collector current density.

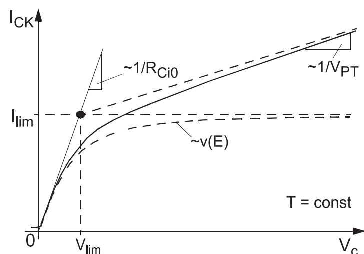


Fig. 7 Critical current I_{CK} and its voltage dependence in Si-based transistors. V_c is the effective collector voltage according to Eq. (10).

leads to the observed cross-over in f_T for power transistors (and also III-V HBTs) that is sketched in Fig. 6(b). HICUM is the only model, in which these different effects are accurately captured.

Towards high current densities, f_T decreases (for any given V_c) as shown in Fig. 6(b) due to the effects already described in Sect. 3. The resulting strong increase in τ_f is described in HICUM by the component $\Delta\tau_f$ that is composed of an emitter, base and collector contribution [35], [45]. The latter can also include bias dependent collector current spreading [42].

The *onset* of high-current effects strongly depends on V_c and can be described quite well by the critical current I_{CK}. As shown in Fig. 7 for Si/SiGe transistors, I_{CK} follows at low voltages the velocity-field relation $v(E)$; the slope at the origin is given by the low-field internal collector resistance R_{Ci0} which depends on epi doping and width, and is a model parameter. The voltage V_{lim} separates the low field (ohmic-like) and saturation region of the $v(E)$ curve. Beyond V_{lim}, the critical current approaches a linear voltage dependence with the slope given by the (reciprocal of the) collector punch-through voltage V_{PT} [26], [42].

As discussed in Sect. 3, the physical mechanisms leading to the onset of high-current effects and the I_{CK} formulation in HICUM are the same in Si BJTs and SiGe- HBTs. As a consequence, the employed transit time description in HICUM has been successfully applied to many generations of bipolar technologies since the early eighties.

Using Eqs. (1) and (2), the quasi-static transfer current can be expressed by measurable quantities leading to the Generalized Integral Charge-Control Relation (GICCR) [33], [48]

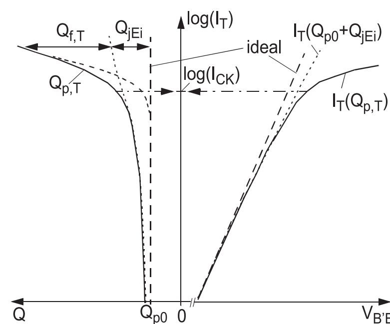


Fig. 8 Visualization of the GICCR Eqs. (11)–(14), assuming $h_{jE} = 1$ for simplicity.

$$I_T = I_{Tf} - I_{Tr} = c_{10} \frac{\exp\left(\frac{V_{B'E'}}{V_T}\right) - \exp\left(\frac{V_{B'C'}}{V_T}\right)}{Q_{p,T}} \tag{11}$$

with the bias independent constant

$$c_{10} = A_E^2 q^2 V_T^2 \mu_{n0r} n_{ir}^2 \tag{12}$$

in which n_{ir} and μ_{n0r} are defined in the neutral base. The *transfer current related* hole charge (index "T")

$$Q_{p,T} = Q_{p0} + h_{jE} Q_{jEi} + h_{jC} Q_{jCi} + Q_{f,T} \tag{13}$$

with

$$Q_{f,T} = h_{fE} Q_{fE} + Q_{fB} + h_{fC} Q_{fC} \tag{14}$$

represents all effects impacting the ideal exponential dependence and also includes the influence of the bandgap variation in the transistor structure on electron transport. The charge Eq. (13) consists of a zero-bias component Q_{p0}, the internal depletion charges Q_{jEi} and Q_{jCi}, and the minority charges Q_{fE}, Q_{fB}, Q_{fC}, in the various transistor regions. Taking the neutral base region as reference, Eq. (1) leads for the charge components in the other regions to weighting factors (h $\cdots$), that are determined mostly by the bandgap changes [33], [48], [49]. For simple cases, Eqs. (1) and (2) can be evaluated analytically, yielding compact expressions for the weighting factors [48], [49]. In general though, these factors are average values. Figure 8 visualizes the impact of the various charges on the transfer current. Numerical comparisons can be found in [25], [33], [36], [48].

Although the GICCR usually is derived for the d.c. case, it can be shown that it is valid up to high frequencies [32], [67] or high-speed transient operation [19], until NQS effects start. Existing compact models for bipolar transistors in one way or the other all employ a GICCR, usually in some simplified form, i.e. as ICCR [69]. The GICCR (11) is actually based on a 1D transistor structure and—as mentioned in Sect. 3—obtained by making certain simplifying assumptions about the lateral distribution of the weighting function, especially h_j in Eq. (1). Considering the 2D/3D case allows to clearly define the charge contributions also in lateral direction [36] and, thus, to establish a master equation for deriving accurate formulations of I_T that enable a

compromise between accuracy and simplicity.

In HICUM, all base currents in Fig. 5 (such as $I_{\rm jBEi} = I^{\rm E}_{\rm jBEi} + I^{\rm SCR}_{\rm jBEi} + I_{\rm Bhrec}$) are modelled independently of the transfer current, reflecting the physically *independent* mechanisms governing base and collector current. This way, realistic shapes of the bias dependent current gain can be described accurately from very low to very high injection. The avalanche current $i_{\rm AVL}$ (Fig. 5) can become a quite complicated function of bias at high $J_{\rm T}$, even for just the 1D case. As investigations of critical transistors in highspeed circuits have shown [63], the pinch-in effect explained in Sect. 3 is the dominant mechanism compared to 1D breakdown, making any lumped representation of this effect questionable in terms of accuracy for practical circuit design. Thus, rather than offering a computationally expensive 1D breakdown model, HICUM contains only a weak avalanche model with the main purpose of indicating the onset of breakdown and of constructing a distributed 3D model to properly capture the pinch-in effect.

HICUM contains an accurate compact analytical formulation for the bias dependence of $r_{\rm Bi}$ that includes emitter current crowding and is valid up to very high current densities [29]–[31]. The frequency dependent current crowding for small-signal operation is also explicitly accounted for (to first order) via the shunt capacitance $C_{\rm rBi}$ in Fig. 5 [32]. Unfortunately, a similar approach is not possible for the general case of (high-speed) large-signal switching. Therefore, using $C_{\rm rBi}$ in the latter case can lead to incorrect results and is not recommended. Investigations have shown though that at least for the class of high-speed current-mode circuits the different values of $r_{\rm Bi}$ during switching-off and -on tend to compensate each other [19], giving fairly accurate results using the d.c. value.

Vertical NQS effects for both y_{21} and y_{11} are taken into account in HICUM, based on the first-order solution discussed in Sect. 3. Note, that all other compact models neglect NQS effects in the minority charge, i.e. for y_{11}.

4.3 Temperature Dependence

An important quantity determining the temperature dependence is the bandgap, which enters the transfer and junction currents as well as the built-in voltages. Assuming the bandgap to be linear dependent on T, the following formulation is usually employed in simulators for junction related saturation currents,

$$I_{\rm jS}(T) = I_{\rm jS}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{\rm T}} \exp\left[\frac{V_{\rm geff}(0)}{V_{\rm T}}\left(\frac{T}{T_0}-1\right)\right] \qquad (15)$$

with T_0 as reference temperature and $\zeta_{\rm T}$ as a coefficient; $V_{\rm geff}(0)$ is the towards $T=0$ *extrapolated effective* bandgap, which includes a bandgap-change $\Delta V_{\rm g}$ due to high-doping and material composition. While Eq. (15) has been sufficient in the consumer products temperature range, most recent interest in deploying SiGe technology in, e.g., cars, airplanes and power devices, requires modeling a larger temperature range, especially at higher temperatures up to even 300°C.

To extend the accuracy of the temperature description, while maintaining the simple form of Eq. (15), in HICUM a special nonlinear expression for $V_{\rm g}$(T) is used [70],

$$V_{\rm g}(T) = V_{\rm g}(0) + K_1 T \ln(T) + K_2 T \qquad (16)$$

with $V_{\rm g}(0) = 1.774\,{\rm V}$, $K_1 = -8.459 \times 10^{-5}/K$, and $K_2 = 3.042 \times 10^{-4}/K$ [71]. As a consequence of the above equation, the parameters in Eq. (15) now have a different meaning; i.e. $V_{\rm geff}(0) = V_{\rm g}(0) - \Delta V_{\rm g}$ and

$$\zeta_{\rm T} = 4 - \frac{qK_1}{k_{\rm B}} - \zeta_\mu \qquad (17)$$

with ζ_μ (> 0) from $\mu \sim T^{-\zeta_\mu}$, the T dependence of the mobility. ($k_{\rm B}$ is the Boltzmann constant.) The values of these parameters are different for each junction.

Using Eq. (16), the GICCR constant in Eq. (12) reads

$$c_{10}(T) = c_{10}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{\rm CT}} \exp\left[\frac{V_{\rm gBeff}(0)}{V_T}\left(\frac{T}{T_0}-1\right)\right]. \quad (18)$$

The saturation current $I_{\rm S} = c_{10}/Q_{\rm p0}$ of the transfer current $i_{\rm T}$ also contains the temperature dependence of $Q_{\rm p0}$.

The temperature dependence of the built-in voltages in HICUM is described by a smooth physics-based formulation that guarantees positive values also for very high temperatures [46], [72].

The transit time $\tau_{\rm f}$ is a strong function of temperature, mostly via the parameters of the critical current $I_{\rm CK}$ and the diffusivity [26], [42]. For instance, the shift of $\tau_{\rm f}$ (and $f_{\rm T}$) at higher current densities is strongly determined by the T dependence of the internal low-field collector resistance

$$r_{\rm Ci0}(T) = r_{\rm Ci0}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{\rm Ci}} \qquad (19)$$

with $\zeta_{\rm Ci}$ directly from the electron mobility in the collector.

In the EC of Fig. 5, the series resistances, avalanche and tunneling current, and storage time for the BC diffusion charge $Q_{\rm dS}$ are all modeled also as function of temperature.

4.4 Geometry Dependence

As already pointed out in the Introduction, transistor sizing is mandatory for circuit design and optimization. Thus all elements in the EC of Fig. 5 have been made a function of the transistor configuration. This leads to quite a sophisticated set of scaling equations due to the large variety of vertical device designs and lateral configurations that are demanded by designers (cf. discussion in Sect. 3). The complexity of geometry modeling varies from process to process. While for a given process the scaling equations for some EC elements are fairly simple, they can become *very complicated* for other elements. Below, a brief overview is provided on the presently existing scaling approach for HICUM.

Currents are scaled following the same form as Eq. (3), allowing the partitioning into a component per area and per

perimeter length. As shown in [42], defining an effective width and length (analogous to Eq. (4)) of a junction, the corner component can be included with sufficient accuracy as well. The same principle can also be applied to all charges (and their associated capacitances). Since the elements of the internal transistor are scaled with the effective emitter area, the possibly remaining contributions are modified accordingly and included in the respective EC portion of the external transistor. For instance, the BE depletion components in Fig. 5 are given by

$$Q_{jEi} = \overline{Q}_{jEi} A_E,$$
$$Q_{jEp} = Q'_{jEp} P_{E0} - \overline{Q}_{jEi}(A_E - A_{E0}) \quad (20)$$

with the constraint $Q_{jEp}\,(V_{B*E'} > 0) > 0$ and $Q_{jEi} \leq Q_{jE,meas}$.

Scaling of the base and collector resistance is less simple. The latter depends on the number of emitter fingers and the location of the collector contact (finger), e.g. in parallel on one or both sides or perpendicular to the emitter. For the base resistance, the case is much more complicated as illustrated in Fig. 9 for a structure with a single base and emitter contact. The lower part corresponds to a plane through the base region in parallel to the surface (indicated by the arrows in the upper part). This allows to use a quasi- 3D device simulation to obtain the current flow and equipotential lines related to the base current in such a structure. As can be seen from Fig. 9, the missing second base contact on the r.h.s. leads to a non-symmetric current flow in the internal base (which is even larger under h.f. dynamic conditions). This non-symmetry increases with increasing aspect ratio l_{E0}/b_{E0} until at large ratios all current is flowing from one side only, leading to an increase of R_{Bx} (R_{Bi}) by a factor of 2 (4) compared to a double base contact. Circuit optimization requires to find the suitable configuration quickly, using compact models. Fortunately, in [28], [30], [31] a set of compact equations was developed for single and multiple base and emitter contact configurations, with aspect ratios ranging from 1 to infinity. Of course, the discrete nature of contact (stripe) variation requires a number of case distinctions in the implementation.

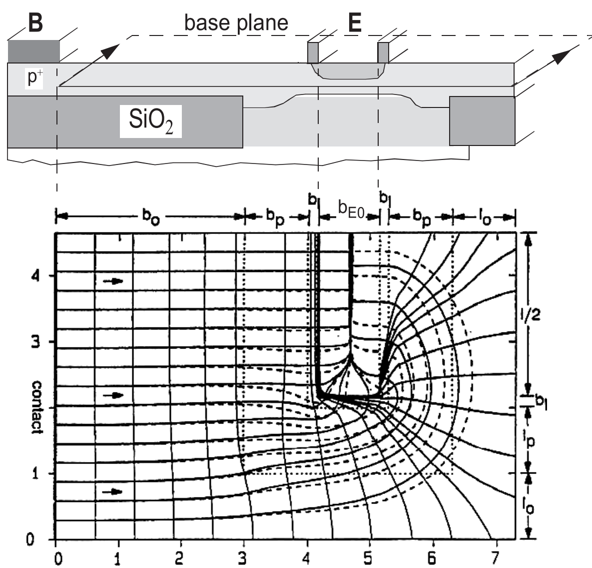


Fig. 9 Base resistance calculation for a single-base transistor: (a) schematic cross-section with conducting plane through the base, (b) current flow and equipotential lines in the base plane for an emitter aspect ratio of 5.

Even more complicated cases than the above are encountered for the elements of the substrate and thermal network. So far, no *compact analytical* scaling equations are known that *accurately* describe the elements of those networks for the layout *variations* found in circuits. Thus, different types of numerical solutions of the underlying differential equations are employed, ranging from more or less time consuming finite difference/element methods to relatively fast, but less flexible, semi-numerical methods. As a suitable compromise, the Green's function approach has been shown to yield sufficiently accurate results for typically encountered device configurations (e.g. [61], [73]).

Design kits typically provide libraries containing model parameter sets for a certain number of *discrete* bipolar transistor configurations. During circuit design often additional device configurations are requested to be added to the library, or models with continuously differentiable scaling properties are even required for circuit optimizers. Therefore, from a design point of view, it would without any doubt be advantageous to have a geometry scalable model available *within* the design system. In this case, just the desired transistor configuration needs to be specified, and the design process can be continued instantaneously.

Implementing scaling equations in a simulator either along with the bias dependent model formulation or as preprocessor script is a feasible solution to the above problem only for a sufficiently simple set of equations and a given process. However, it has significant disadvantages and limitations from both the "production" modeling and design point of view as discussed below. In contrast, pooling geometry scaling equations and (more sophisticated) calculations within a single tool, TRADICA [27] (cf. Fig. 10), sep-

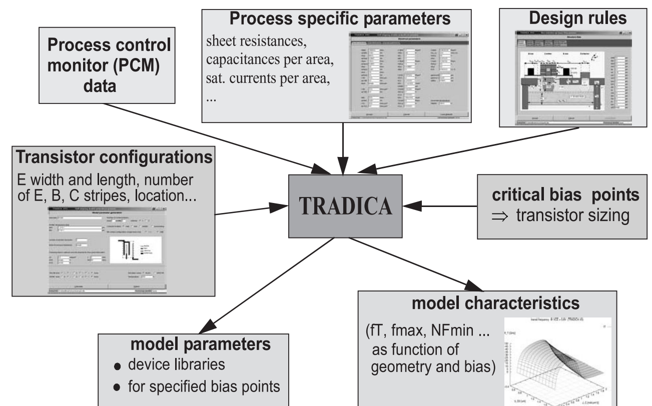


Fig. 10 Overview on the geometry scaling and predictive modeling approach using the TRADICA tool [27].

arately from the simulator has turned out to be a much more efficient solution, enhancing productivity on the modeling side and flexibility on the design side. Over time, a very sophisticated set of scaling calculations for HICUM (and also SGPM) has been developed for fundamentally different device designs, such as Si BJTs, SiGe HBTs and III-V HBTs, allowing to address almost any type of configuration. Originally, the program was written for supporting *transistor sizing* for optimizing high-speed circuits using continuously scalable models. In the nineties, sophisticated but fast predictive modeling capabilities were added to capture the impact of intentional and statistical process variations. Furthermore, a fast thermal analysis [61], [62] enables to view the tempera-ture distribution in realistic layouts and to generate distributed models (cf. Sect. 7). Most recent enhancements include: a modular set of parameter extraction procedures allowing automation; the coupling with device simulators for supporting concurrent engineering during early process development.

The overall goal is to provide an integrated environment enabling a quick and accurate comparison of different process technologies regarding their suitability for given circuit design targets. This is supported by an integration of TRADICA into design systems [74] which will significantly improve design productivity and at the same time reduce maintenance effort on the modeling side. Such a goal is not achievable by just implementing simple scaling equations into model codes. The latter, in particular, does not allow efficient transistor sizing both within and outside a design system and a quick preview of model characteristics vs. transistor *configuration*.

5. Parameter Determination

The still most widely found methodology for model parameter determination relies on fitting a set of measured electrical characteristics of a transistor with fixed geometry; i.e. only bias and temperature dependence are being considered. This generally does not lead to physics-based model parameters and, thus, prohibits any geometry scaling as well as predictive or statistical modeling. The biggest drawback though is, that every transistor configuration needed for circuit design has to be not only modeled but also available on a test chip. Since measurement time and test chip space are quite limited, such a methodology severely limits circuit design.

In contrast, HICUM parameter extraction is based on a well-defined and small set of test structures, which then enables generation of consistent parameters also for any other configuration that is not available on a test chip. This parameter determination methodology, which has also been applied to the SGPM (within its validity limits), is described in more detail in, e.g. [45], [75]–[80]. As example, the resistance from a measurement on tetrode structure with different emitter widths (and constant length) is shown in Fig. 11. Any corner and crowding effects have been corrected simply by using two structures with different length. Thus, the internal base sheet resistance as function of bias is obtained

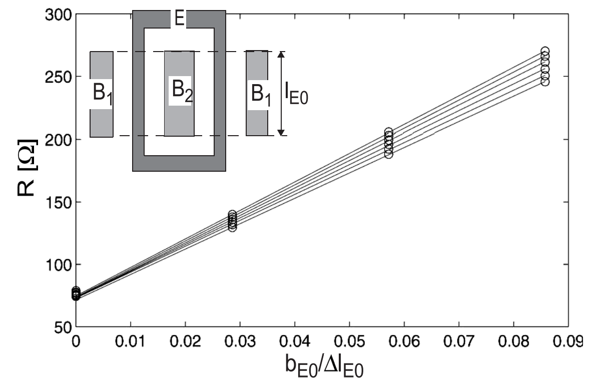


Fig. 11 Tetrode measurements for determining the internal base sheet resistance. For the determination principle see [29].

from the slope and the remaining (external) resistance is obtained from the intercept.

6. Experimental Results

Using the *process-based scalable* approach described above, "production" HICUM parameters have been delivered for a variety of process technologies from foundries such as Atmel, IBM, Jazz, ST, TSMC; publicly available results can be viewed in, e.g. [15], [34], [35], [37]–[41], [45], [76]–[83]. Due to the lack of space, only a few selected examples can be presented here, which are key results related to the high-frequency transistor behavior and are typical for the accuracy achievable with HICUM in an *industrial* environment.

Figures 12 to 15 show most recent results for comparisons of HICUM with measurements for transistor fabricated in advanced SiGe-BiCMOS production processes. For device and process characterization, typically forward Gummel and transit frequency curves are measured. The good agreement obtained with HICUM in Figs. 12 and 13 confirms the accuracy of charge storage modeling, that can be observed directly through f_T and indirectly in I_C via the GICCR. Note the strong temperature increase at higher J_C and V_{CE} also indicated Fig. 13.

Geometry scaling results are shown in Fig. 14 [77]. Good agreement its obtained for a wide and practically useful width range of the whole relevant bias region. Similar agreement is obtained for an emitter length variation, except for the smallest device ($0.17 \times 0.51\,\mu m^2$), for which the vertical profile has most likely changed due to its small emitter window.

As an interesting non-standard characteristic, highfrequency harmonic distortion results up to fifth order are shown in Fig. 15. At low current densities, the transistor operates very close to f_T for the highest harmonics. At higher current densities, the charge storage effects cause troughs and peaks in the higher harmonics which are closely related to the curvature of f_T. HICUM follows quite well the various distortion curves, indicating its suitability for h.f. nonlinear circuit design tasks.

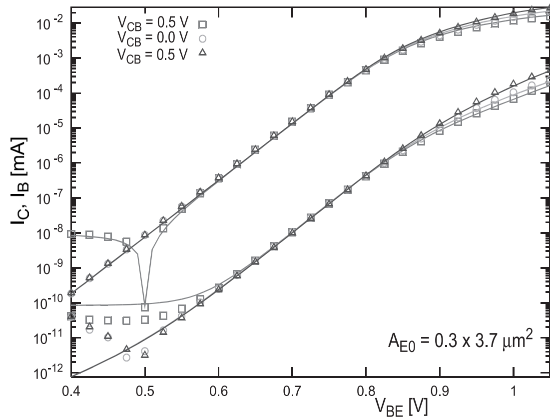


Fig. 12 Forward Gummel plot: comparison between HICUM (lines) and measurements (symbols) of an ST BiCMOS process.

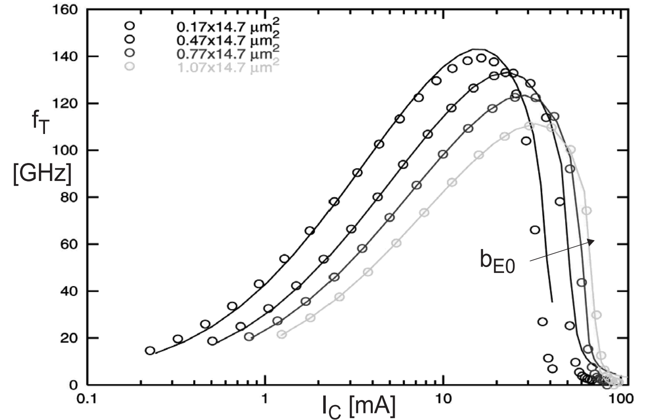
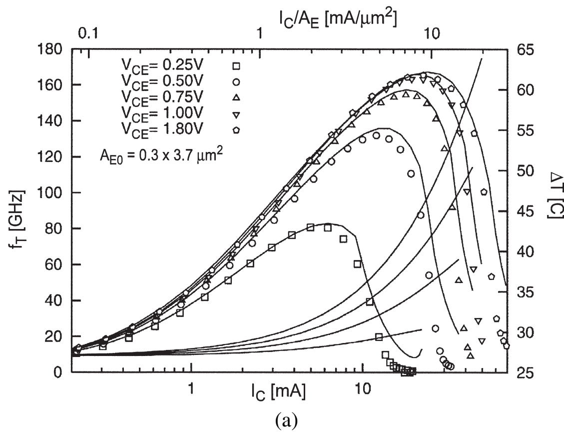
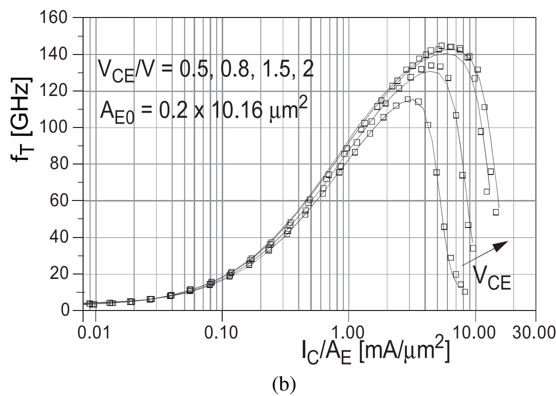


Fig. 14 Transit frequency vs. collector current density for different emitter widths: comparison between HICUM (lines) and measurements (symbols) from an ST SiGe BiCMOS process.



(a)



(b)

Fig. 13 Transit frequency vs. collector current density: comparison between HICUM (lines) and measurements (symbols) from SiGe BiCMOS processes of (a) ST and (b) JazzSemi.

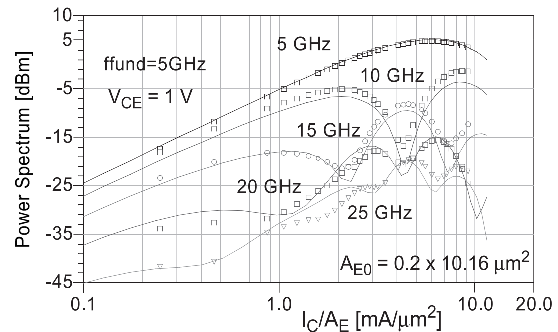


Fig. 15 Harmonic distortion output power up to fifth order at 5 GHz fundamental frequency: comparison between HICUM (lines) and measurements (symbols) for a Jazz BiCMOS process. Input power: −11.34 dBm.

Similar results have been obtained for processes with transit frequencies of more than 200 GHz [84], [87].

7. Model Hierarchy

The increasing complexity of device designs and associated number of physical effects have led to fairly complicated compact model forms that are being less and less understood by circuit designers. Model complexity is defined here by number of nodes and elements in the EC along with the element equations. For design tasks though often a fairly simple model is sufficient, at least during the initial phase(s). Final verification and some critical cases (may) require more complicated models, even beyond that in Fig. 5. For instance, a power amplifier transistor may require a distributed representation to accurately describe high-frequency and electro-thermal effects, that lumped models cannot capture. Meeting these very different design needs with a single model form is likely to be computationally inefficient and, hence, makes a model hierarchy very attractive [16]. Such a hierarchy, which has been developed around HICUM, is visualized in Fig. 16.

The simple model, HICUM/Level0 [85]–[87], has been developed recently with the goal to eliminate the problems of the SGPM for modern processes *without* increasing the *computational* and *parameter extraction effort*. Thus, HICUM/L0 has the same number of electrical nodes as the standard SGPM (Level0), but significantly improved model equations. The latter have been borrowed from HICUM/L2 and have then partially been reformulated in a simplified explicit form. They include first-order effects such as a

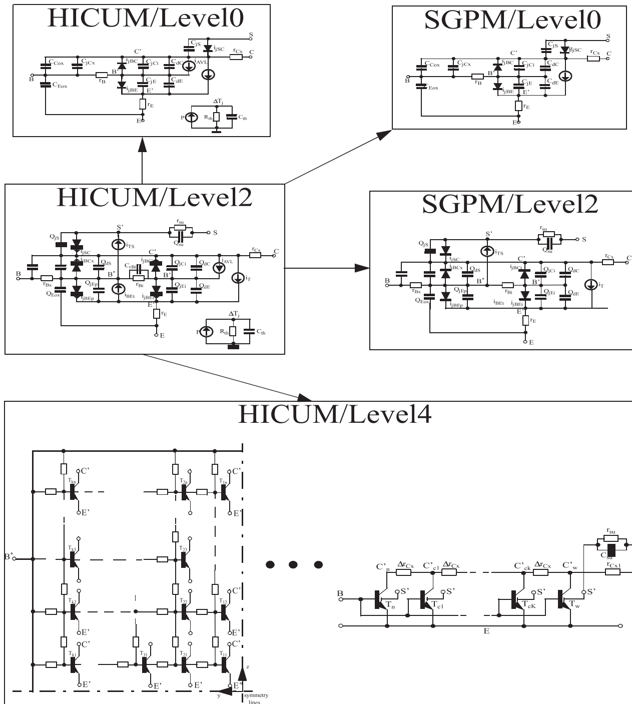


Fig. 16 Model forms with different complexity for building a compact model hierarchy.

much improved minority charge model, CB breakdown, self-heating and collector punch-through.

The distributed model (HICUM/Level4) can be generated from process-specific parameters and layout dimensions that are already available for HICUM/L2. Depending on the application, different partitionings of the actual transistor structure into discrete single cells are possible. Such a cell can be

- a transistor within a PA array, addressing distributed feed lines and time dependent thermal coupling [62], [88] between the array transistors;
- an emitter finger (with its associated surroundings) in a multi-finger structure to address mostly the inhomogeneous T distribution and thermal coupling between fingers;
- a discrete portion of an emitter finger in order to properly model the 3D pinch-in effect caused by BC breakdown.

Both the more simple and more sophisticated models can be *generated without any additional parameter extraction effort*, using the medium complexity model (HICUM/L2) as reference. Since the relevant processspecific parameters and layout dimensions are already available in TRADICA, the latter allows to realize a selfconsistent model hierarchy very quickly and with low maintenance effort for a foundry. Furthermore, within each of the hierarchy levels, the user can still create intermediate levels by turning off certain effects independently (without the necessity of reformulating equations). Integration of TRADICA in a design system enables the user to quickly adapt the employed model(s) to the design task. Obviously, the need to flexibly change the EC topology makes such a hierarchy generation difficult to realize with just simulator preprocessor scripts (within a model).

8. Conclusions

Based on a discussion of circuit design requirements and the most important physical effects occurring in advanced bipolar transistor process technologies, the underlying ideas and operation principle of HICUM have been presented. Its charge-based formulation enables an accurate description of the dynamic transistor behavior up to both high frequencies and high current densities. The bias and temperature dependent model formulation is presently available in all major commercial circuit simulators. Over many years, also a sophisticated set of equations for geometry scaling has been developed that satisfies today's demand for the large variety of transistor structures employed for product design. The implementation in the TRADICA scaling and sizing tool together with an efficient model parameter extraction methodology and its integration into a widely available framework has enabled the successful application of HICUM to production circuit design in various (foundry) technologies over the past few years. Most recently, also a simplified HICUM version has been developed addressing various needs of the design community.

The present model development effort is targeted towards, e.g., improving the description of effects associated with heterojunctions (incl. III-V HBTs), lateral and vertical geometry scaling, h.f. noise, and electrothermal interaction. In parallel, work is being continued on improving parameter extraction methods and test structures as well as design efficiency. The latter is being accomplished by integrating TRADICA into process design kits to enable fast (partially automated) circuit optimization, statistical design and concurrent engineering for highfrequency applications in an industrial environment.

The biggest bottleneck for deploying new models and model versions is still the simulator implementation. The hope is that for future releases the use of Verilog-A in combination with model compilers (e.g. [90], [91]) will significantly reduce implementation effort and time.

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