Methodology for Bipolar Model Parameter Extraction

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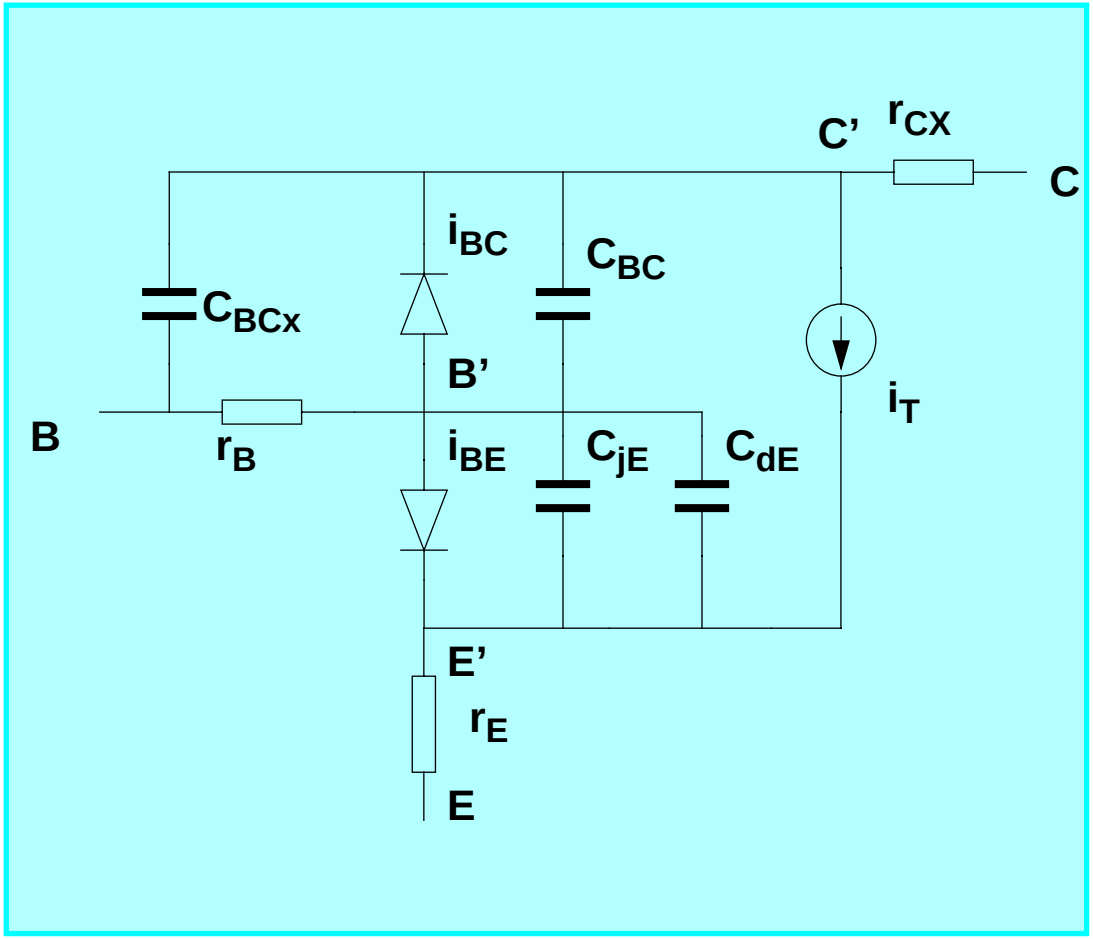
Outline

- General Remarks
- Brief overview of TRADICA
- Parameter extraction flowchart
- Process-specific parameter extraction
- HICUM-specific parameter extraction
- SGPM-specific parameter extraction
- Model generation and verification
- Conclusion

General Remarks

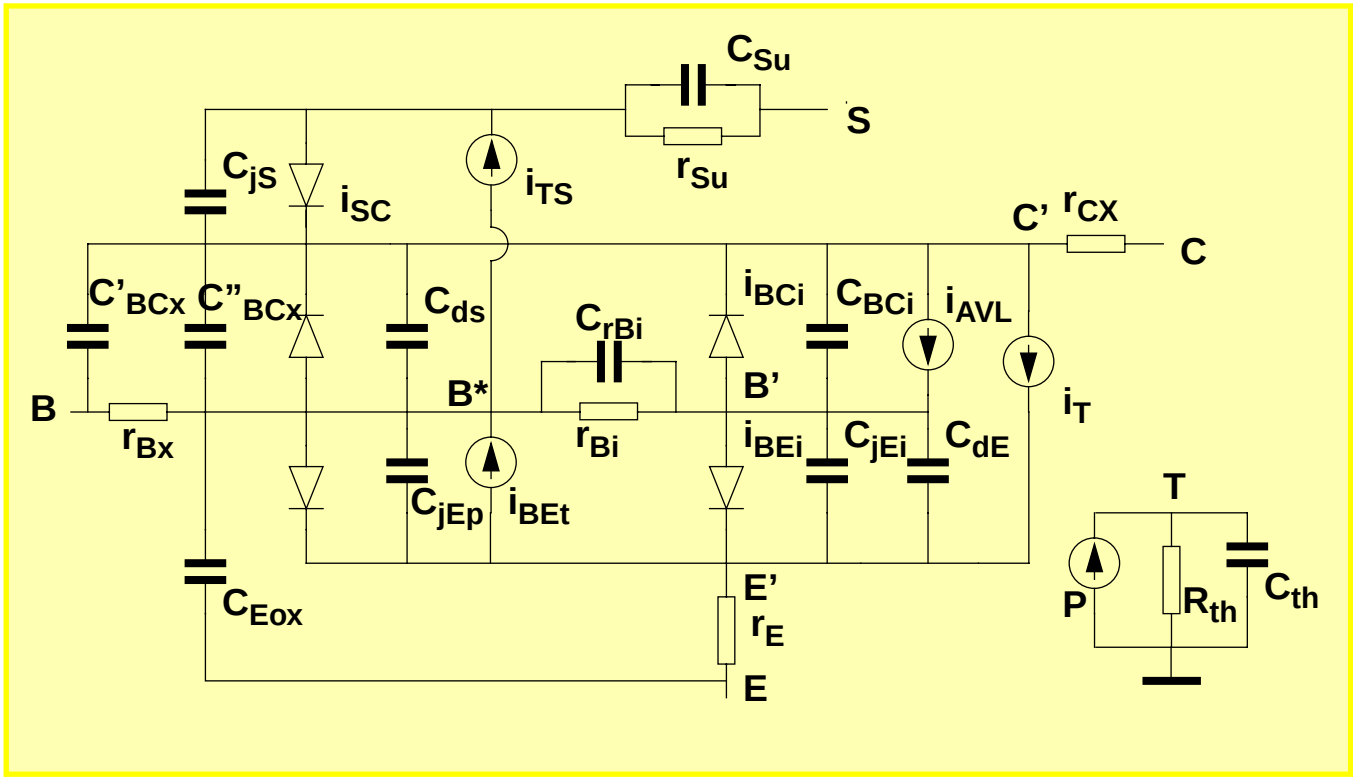
- **Objectives**
  - Concurrent engineering requires physics-based and predictive modeling strategy
  - Generation of scalable models
- **Single transistor fitting**
  - relies on a “golden” wafer which is typically very difficult to obtain, or is simply not available.
  - often results in unrealistic/non-physical parameter values.
  - can only produce the simple equivalent circuit shown to the right due to lack of sufficient geometry related information.
  - usually provides a library with a very limited number of transistors, unless time and resource are unlimited.



General Remarks (cont.)

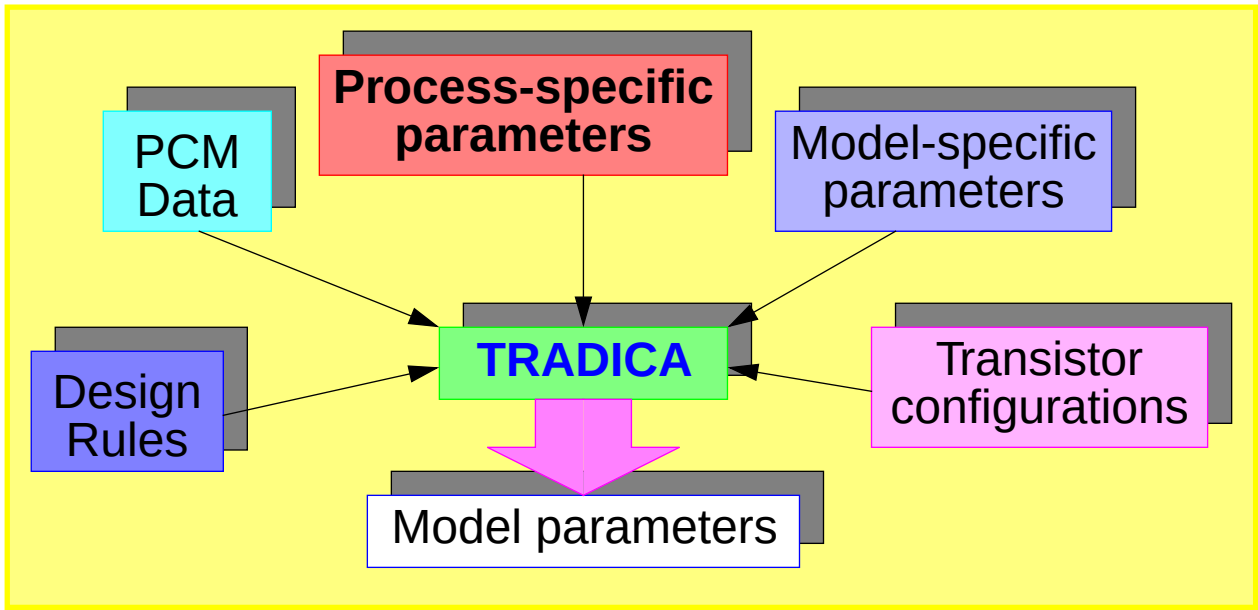
- **A process-based scalable approach**
  - enables extraction of an accurate physics-based equivalent circuit (see fig. below) with a realistic representation of parasitic components.
  - maintains physical values of extracted parameters, therefore enabling later shift on the extracted parameters in accordance to process changes as well as statistical variation.
  - enables efficient model generation of transistors with different configurations.

- **The process-based scalable methodology described in this presentation has been implemented as a Matlab toolbox called Bipax and used for production parameter extraction.**



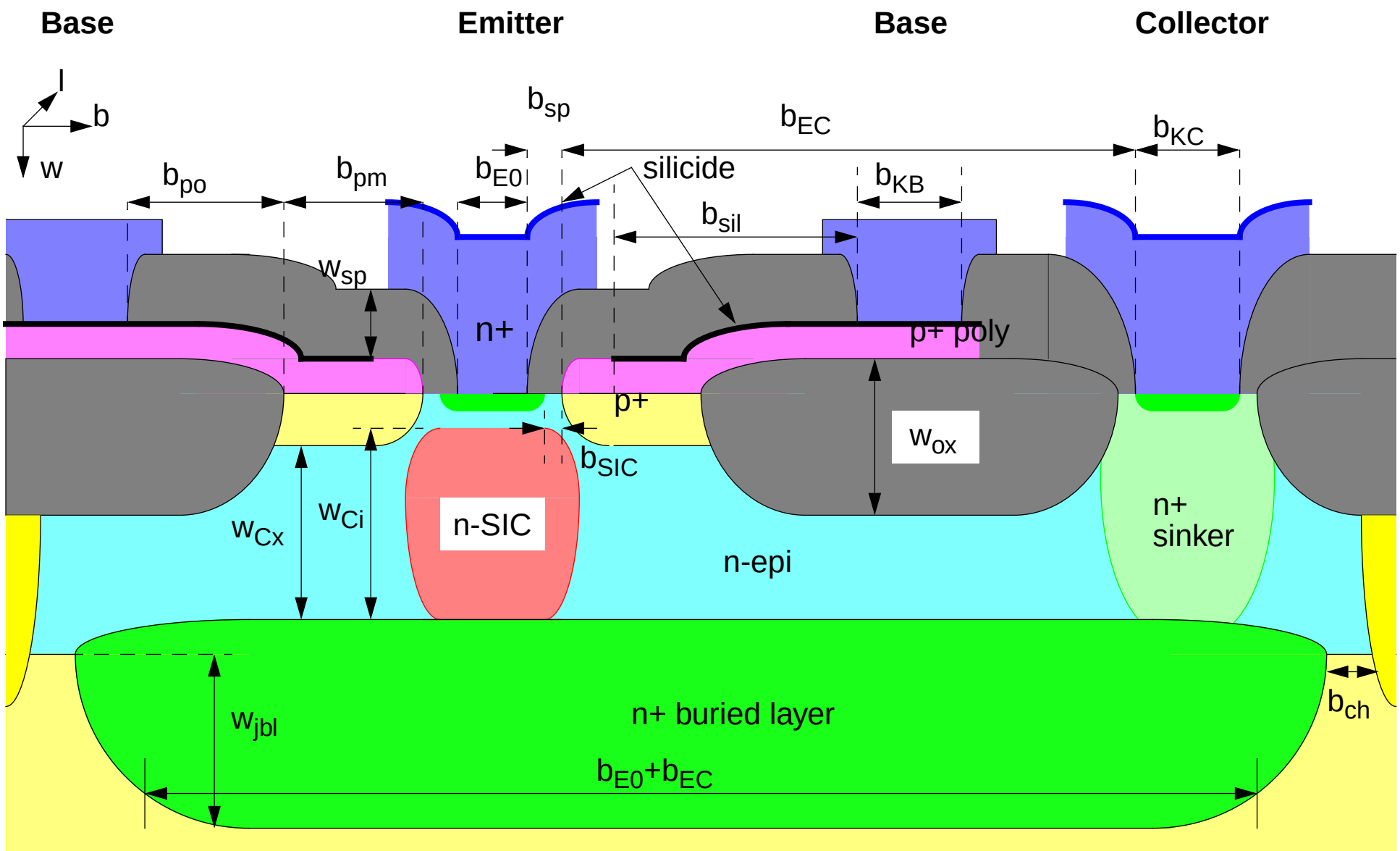
Brief overview of TRADICA - Model generation

- **While initially being developed as a transistor dimensioning tool, TRADICA can also be used as a model generation and prediction tool [1].**
- **TRADICA takes process-specific and model-specific parameters as well as geometry description to generate model parameters for transistors of various configurations, which are defined by emitter width and length, number of emitter, base, and collector contacts (stripes), and their spatial arrangement.**



- **Given specific parameters extracted from an arbitrary wafer, TRADICA can shift model parameters for wafers subject to various process variations based on respective process control monitor (PCM) data and analytical prediction equations.**
  - Eliminating the need of a golden wafer
  - Enabling predictive and statistical modeling

TRADICA Geometry Dimensions from Design Rules



Process-specific parameters

- r_{SBi0}, r_{Ssp}, r_{Spm}, r_{Sil}: pinched-base sheet resistance, base sheet resistance under spacer (link resistance), poly-on-mono sheet resistance, sheet resistance of silicided base.
- r_{KB}, r_{KC}, r_{KE}, r_{Sbl}: base, collector, emitter contact and buried layer sheet resistance
- C_{jEi0}, V_{DEi}, z_{Ei}, α_{jEi}, C_{jEp0}, V_{DEp}, z_{Ep}, α_{jEp}: C_{jE} related parameters
- C_{jCi0}, V_{DCi}, z_{Ci}, V_{PTCi}, C_{jCb0}, V_{DCb}, z_{Cb}, V_{PTCb}, C_{jCp0}, V_{DCp}, z_{Cp}, V_{PTCp}: C_{jC} related parameters including punch-through voltages.
- C_{jSi0}, V_{DSi}, z_{Si}, C_{jSp0}, V_{DSp}, z_{Sp}: C_{CS} related parameters
- γ_C, γ_B: Ratio of peripheral component to bottom component of specific collector and base currents
- δ_C: Collector spreading angle
- Temperature coefficients and bandgap
- τ_{p0}/τ_{i0}: Ratio of peripheral component to bottom portion of the low-current transit time τ_{f0}.

HICUM-specific parameters

- c_{10}, Q_{p0}, J_{ch}, h_{fe}, h_{fc}, h_{jEi}, h_{jCi}: Transfer current parameters including GICCR HBT model extension
- J_{BEiS}, m_{BEi}, J_{REiS}, m_{REi}, J_{BCS}, m_{BC}: Base current parameters
- r_{Ci0}, V_{lim}, V_{PT}, V_{CEs}: Critical current (I_{CK}) parameters
- τ_0, $d_{\tau 0h}$, τ_{Bvl}: Low-current transit-time parameters
- τ_{fE0}, $g_{\tau fE}$: Emitter transit-time parameters
- τ_{hcS}, α_{hc}: Collector high-current transit-time parameters
- f_{AVL}, q_{AVL}: Avalanche current parameters
- J_{BEtS}, α_{BEt}: Tunneling current parameters
- A_F, K_F: Flicker noise parameters
- R_{th}, C_{th}: Parameters for self-heating
- α_{IT}, α_{QF}: Parameters for modeling NQS effect

SGPM-specific parameters

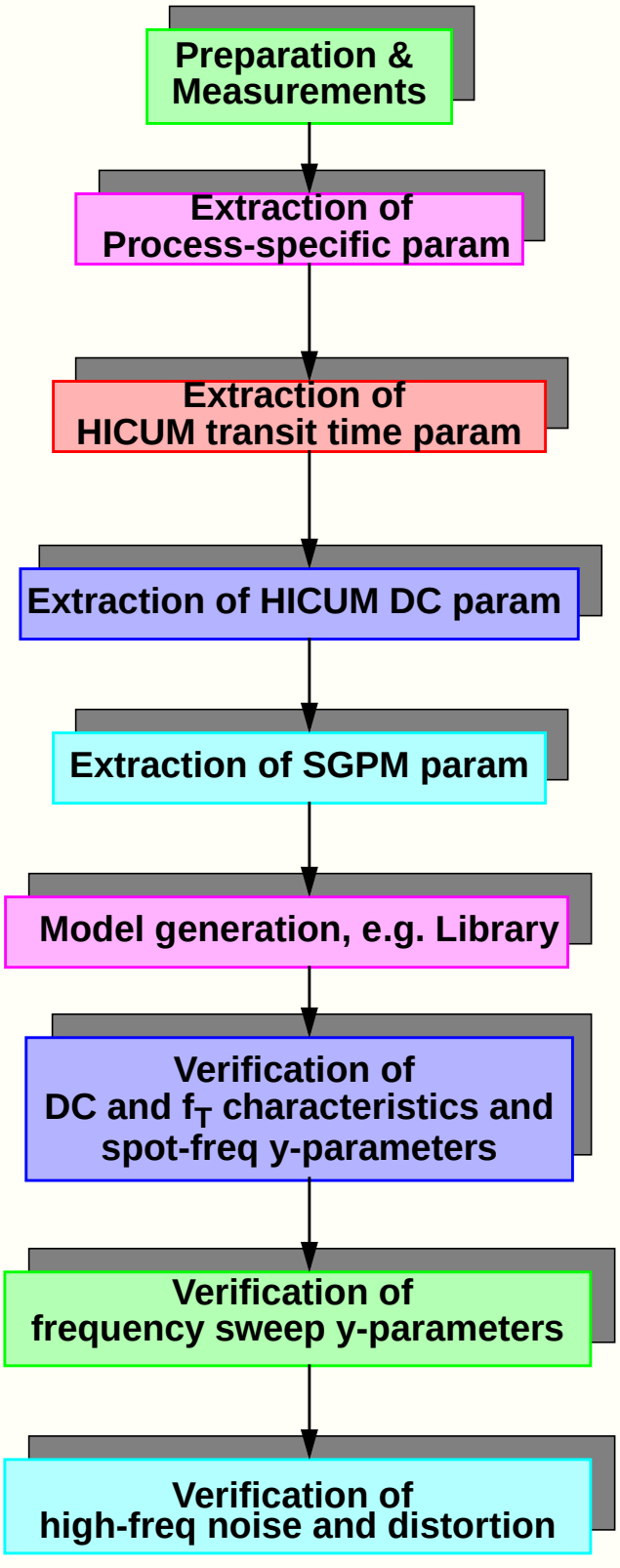
- **JS, NF, BF:** Collector current and current gain parameters
- **VAF, VAR:** Early voltages
- **JKF:** Knee current density
- **JSE, NSE:** Base recombination current parameters
- **TF, XTF, VTF, ITF:** Transit-time/f_T parameters
- **apo, JRB:** Parameters for modeling the internal base resistance
- **EG:** Bandgap
- **AF, KF:** Flicker noise parameters
- **PTF:** Excess phase (non-quasi-static effect in transfer current)

Process control monitors for predictive modeling

Except δb_{E0} and δw_C all the parameters listed here are the percentage changes relative to their values in the base-line process.

- **δb_{E0}: emitter width change [μm]**
- **δr_{Sbi}: internal base sheet resistance change [%]**
- **$\delta \rho_{Ci}$: internal collector sheet resistance change [%]**
- **δN_{Cx}: external collector doping change [%]**
- **δw_C: internal collector thickness change [μm]**
- **δr_{Spm}: poly-on-mono sheet resistance change [%]**
- **δr_{Sbl}: buried-layer sheet resistance change [%]**
- **δr_E: emitter resistance change [%]**
- **$\delta \rho_{su}$: substrate sheet resistance change [%]**

Bipolar Parameter Extraction Flowchart



- Collect design rules
- Collect SEM/TEM pictures
- Perform Measurements

- Extraction of resistance and capacitance related parameters
- Check scaling

- Determine collector spreading angle
- Extraction of transit time parameters

- Extraction of HICUM collector and base current related parameters

- Extraction of SGPM collector and base current related parameters
- Optimization to obtain f_T related parameters

- Use TRADICA to generate model parameters

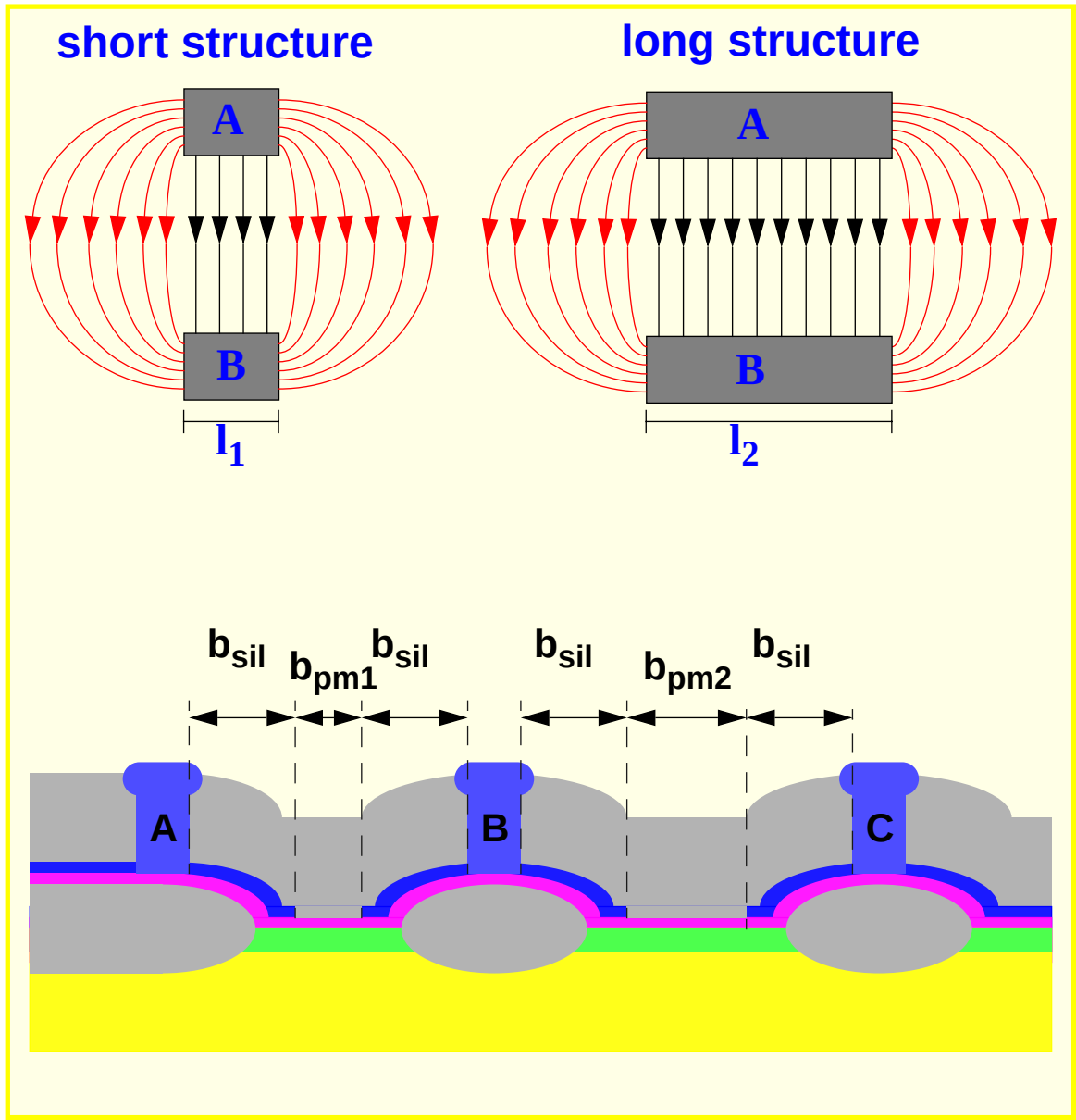
- Tune extrinsic base resistance
- Tune transit time parameters (on transistors with different configurations simultaneously)

- Tune NQS parameters: excess phase... (on transistors with different configurations simultaneously)

- Check RF related performance (on transistors with different configurations simultaneously)

Process-specific parameter extraction - Base silicide and poly sheet resistance

- Use two 3- (or 4-) terminal contact chain structures with different lengths, l_1 and l_2.
- Correct current spreading by subtracting current of short structure from that of long one.
- Obtain corrected resistance between terminals A and B, R_{AB}, and terminals B and C, R_{BC}

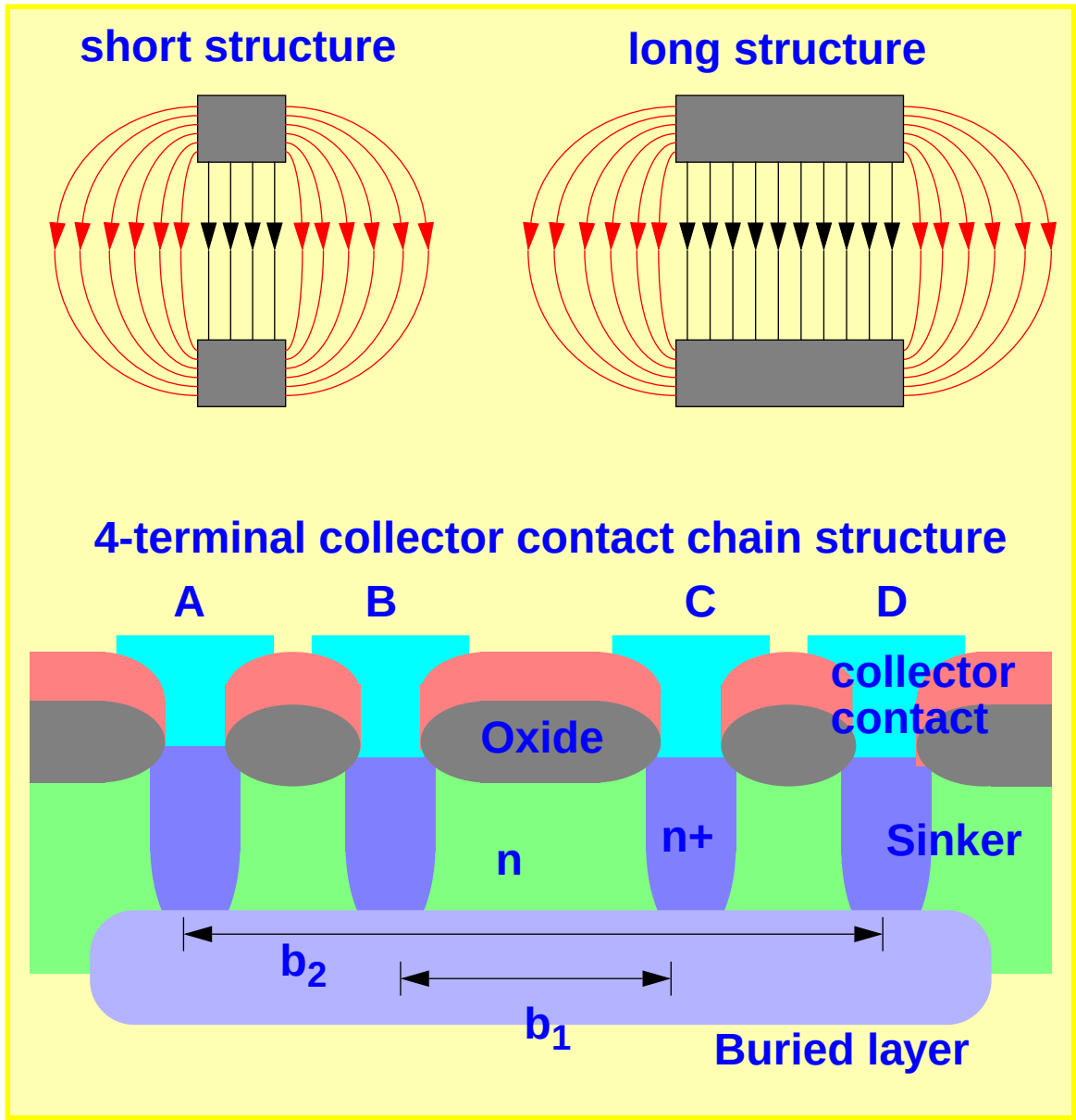


Process-specific parameter extraction - Base silicide and poly sheet resistance (cont.)

- Calculate the base poly sheet resistance as $r_{pm} = \frac{R_{BC} - R_{AB}}{2(b_{pm2} - b_{pm1})}\Delta l$ and silicide sheet resistance as $r_{Ssil} = \frac{\left(R_{BC} - r_{pm}\frac{2b_{pm2}}{\Delta l}\right)}{b_{sil}}\Delta l$, where $\Delta l = l_2 - l_1$ is the length difference of the long and short structures.
- A similar structure with $b_{pm}=0$ can be used to extract the specific base contact resistance (and the silicide sheet resistance).

Process-specific parameter extraction - Collector contact-sinker resistance and buried-layer sheet resistance

- Use two 4-terminal collector contact chain structures with different lengths, l_1 and l_2.
- Correct current spreading by subtracting current of short structure from that of long one.

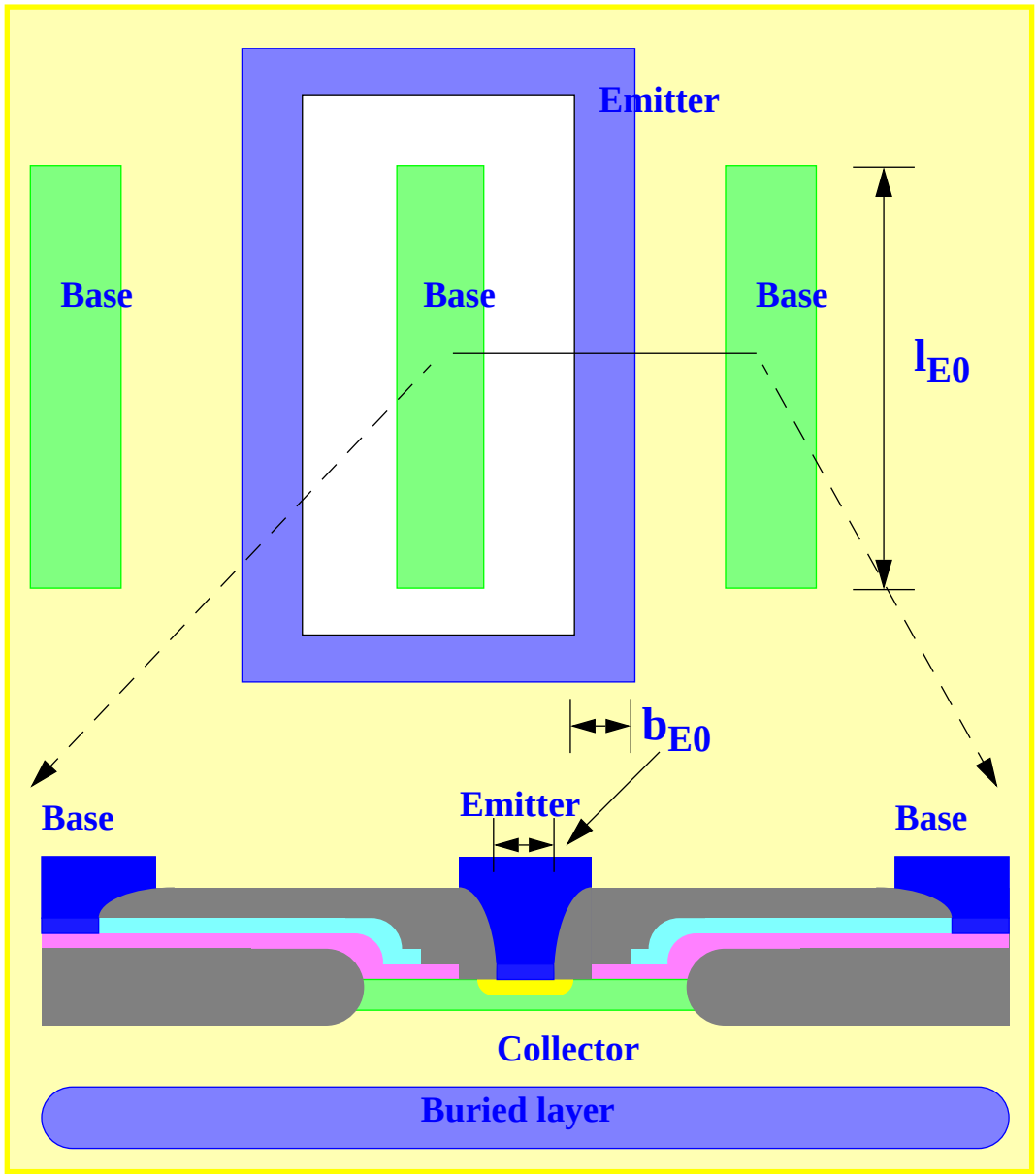


Process-specific parameter extraction - Collector contact-sinker resistance and buried-layer sheet resistance (cont.)

- Force current through terminals A and D, measure voltage at B and C, resulting in resistance R_{BC}^{AD}, that contains no contact and sinker contribution. Buried layer sheet resistance is then $r_{Sbl} = R_{BC}^{AD}(\Delta l / b_1)$.
- Measure resistance directly between B and C giving $R_{BC} = R_{BC}^{AD} + 2R_{KC}$. The combined specific contact-sinker resistance is then $r_{KC} = \frac{R_{BC} - R_{BC}^{AD}}{2}(b_{KC} \cdot \Delta l)$ in $[\Omega \cdot \mu m^2]$.

Process-specific parameter extraction - Base pinch resistance

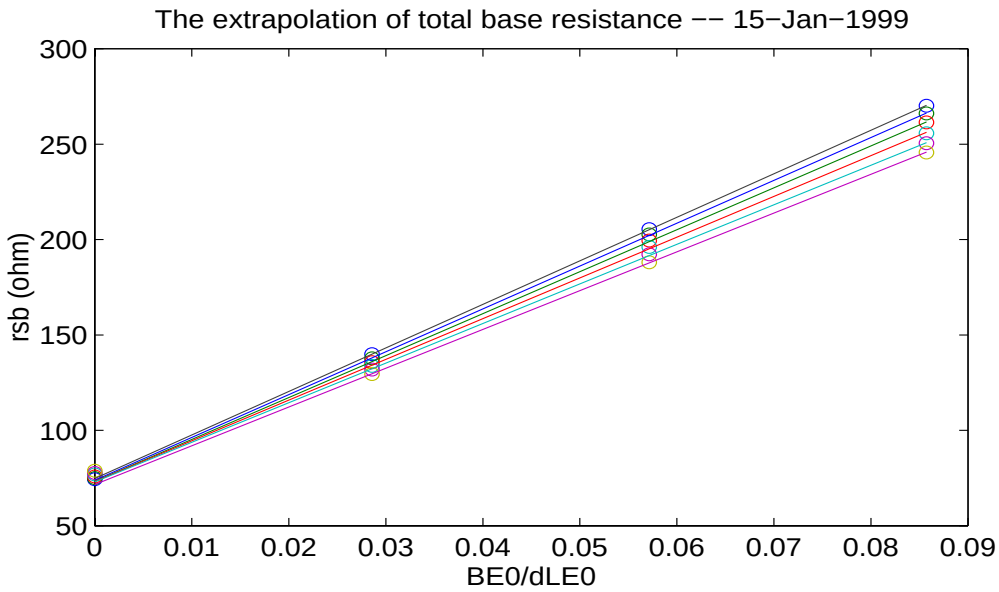
- Use enclosed structures to ensure current flowing under the emitter [2]-[5].
- By using two structures with different lengths (l_{E0}), the corner and fore-side current crowding can be canceled ($\Delta l = l_{E02} - l_{E01}$).
- Measure bias-dependent total resistance R for test structures with various emitter widths (b_{E0}).

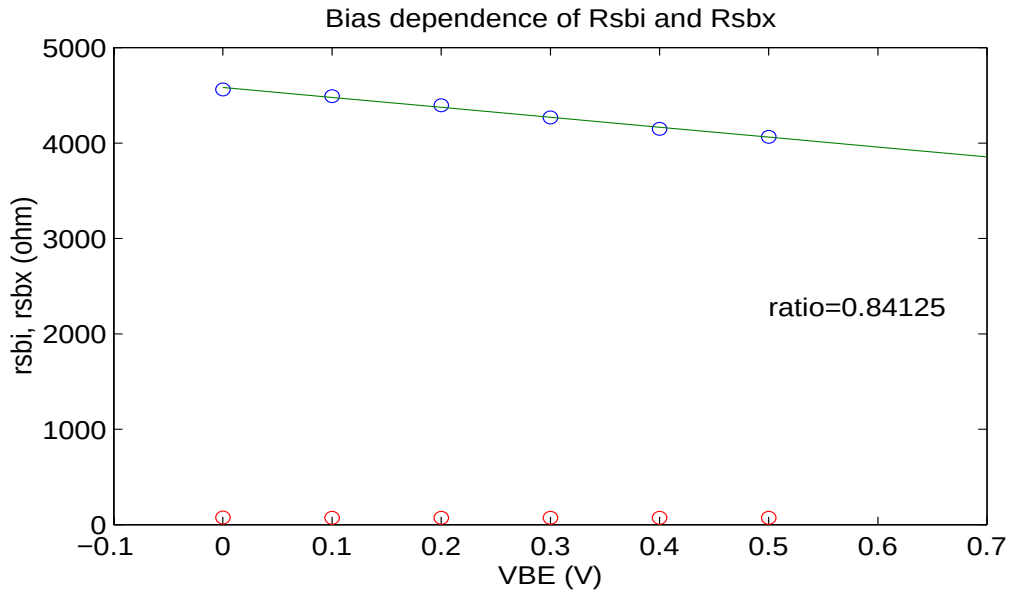


Process-specific parameter extraction - Base pinch resistance (cont.)

- **Extract the bias-dependent base sheet resistance values from the slopes of the fitted lines at different V_{BE}.**
- **The external base link resistance can be determined from the extrapolated value,**

  $R_{bx} = R_{KB} + R_{sil} + R_{pm} + R_{link}$**, where R_{KB}, R_{sil}, R_{pm}, and R_{link} are the base contact, silicide, poly-on-mono, and link resistance, respectively.**



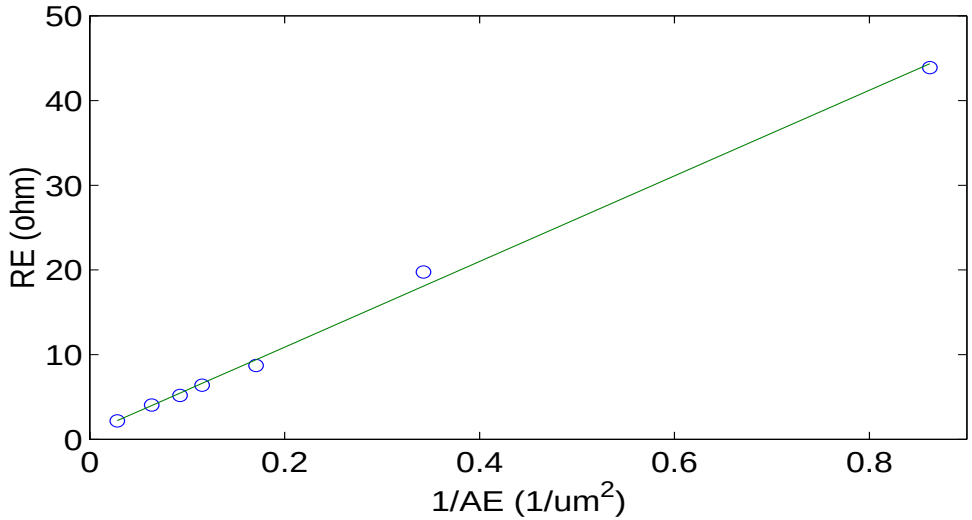


Process-specific parameter extraction - Emitter contact resistance

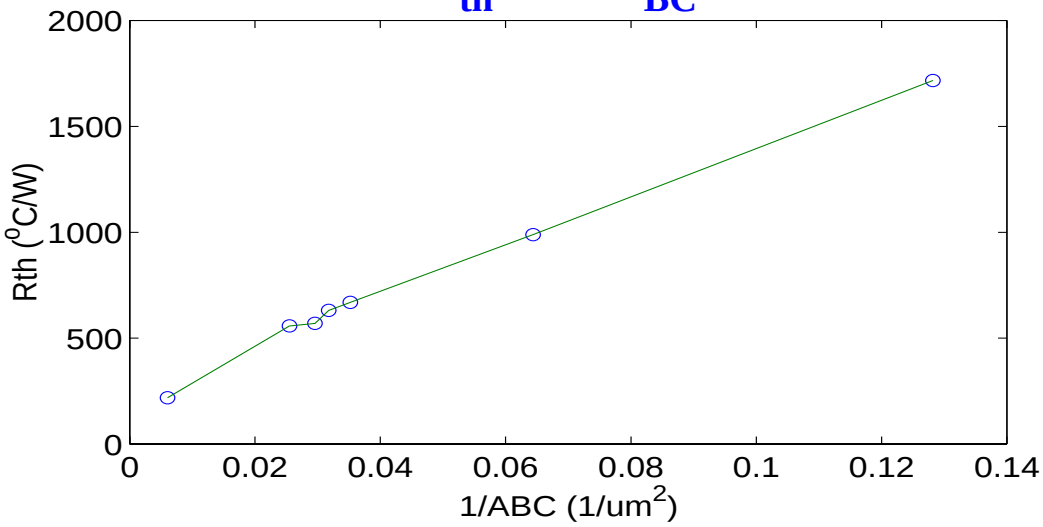
- Extract the emitter series and thermal resistance for transistors of various sizes using the simultaneous r_E-R_{TH} extraction method [6].
- Plot r_E vs. $1/A_E$ to obtain the specific emitter contact resistance (in $[\Omega \cdot \mu m^2]$) from the slope.
- Emitter resistance can also be extracted using the modified open-collector method [7], in which self-heating effect is insignificant.

Simultaneous r_E-r_{TH} extraction

r_E vs. $1/A_E$

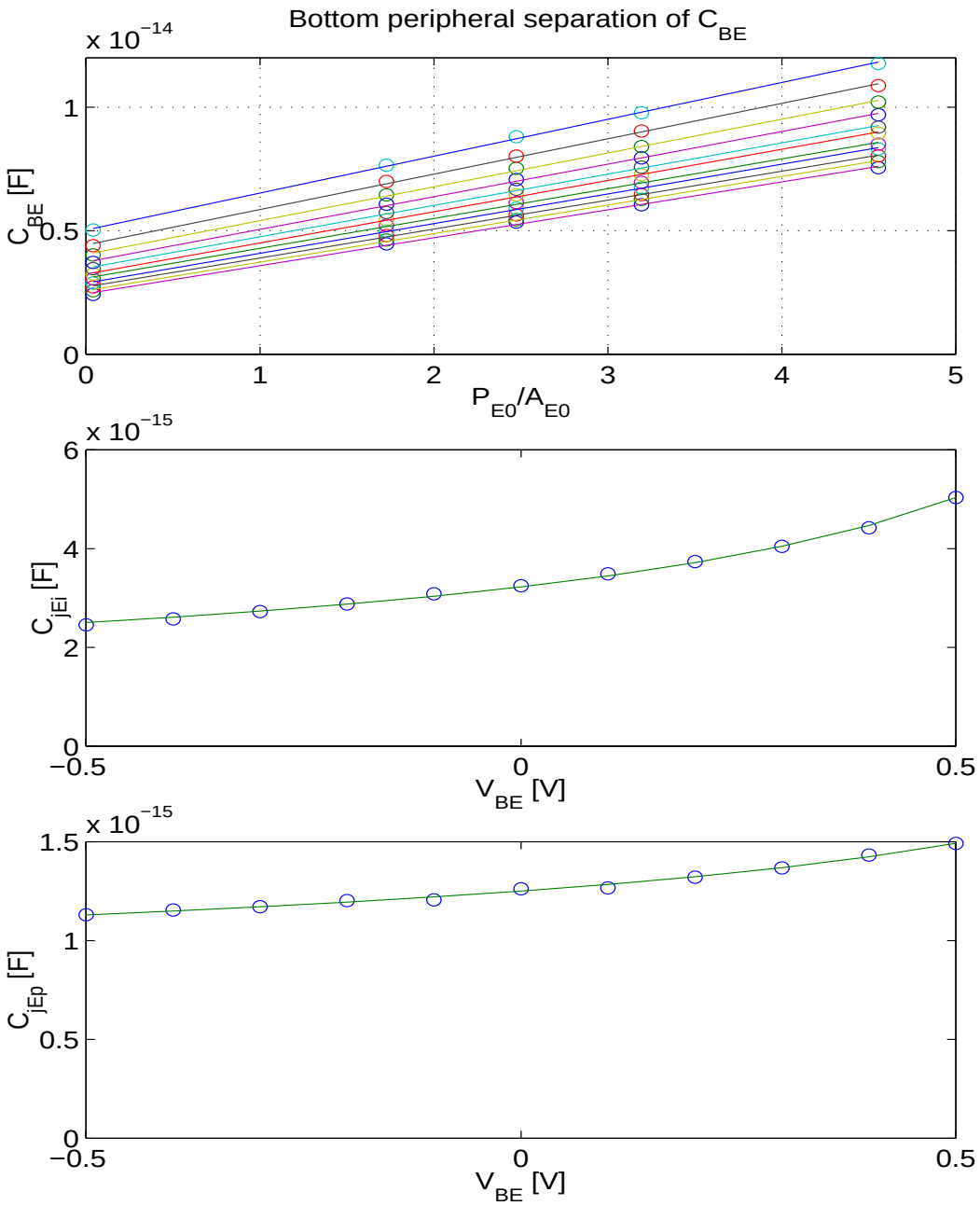


R_{th} vs. $1/A_{BC}$



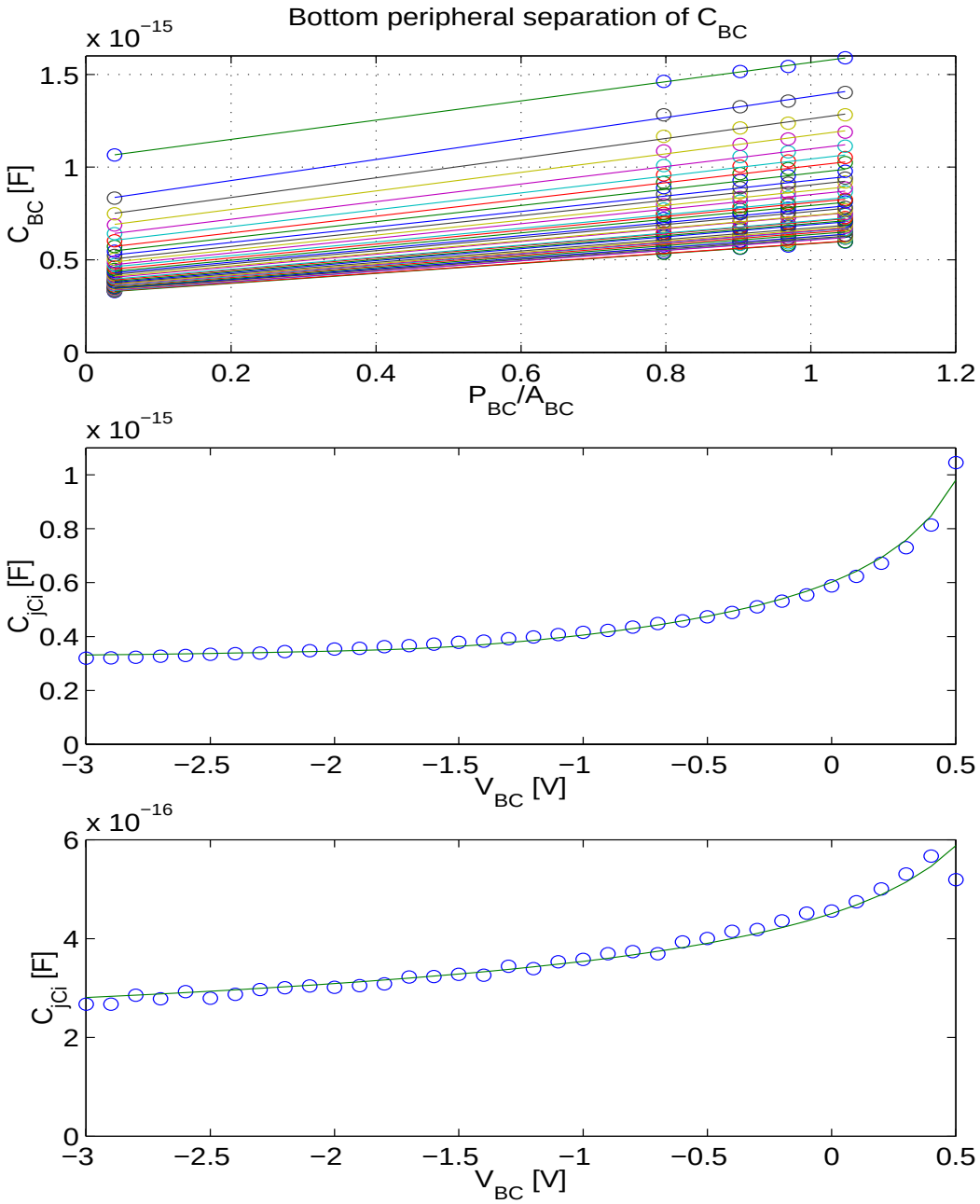
Process-specific parameter extraction - C_{jE} and C_{EOX}

- **Components to be considered:**
  $C_{jEi} \propto A_{E0}$, $C_{jEp} \propto P_{E0}$, **and** $C_{EOX} \propto P_{E0}$, **i.e.** $C_{BE} = A_{E0} \cdot C_{jEi0} + P_{E0} \cdot (C_{jEp0} + C_{EOX})$
- **Measured test structures: a large area transistor, measured with CV meter, and several long-stripe transistors with different P/A ratios, measured with s-parameter technique.**
- **Obtain C_{jEi} for each bias from the zero x-axis intercept and C_{jEp} from the slope.**
- **Optimization to obtain the corresponding parameters.**



Process-specific parameter extraction - C_{jC} and C_{COX}

- **Components to be considered:**
  $C_{jCi} \propto A_{BC}$, $C_{jCp} \propto P_{BC}$, **and** $C_{COX} \propto P_{BC}$, **i.e.** $C_{BC} = A_{BC} \cdot C_{jCi0} + P_{BC} \cdot (C_{jCp0} + C_{COX})$
- **Measured test structures: a large area transistor, measured with CV meter, and several long-stripe transistors with different P/A ratios, measured with s-parameter technique.**
- **Obtain C_{jCi} for each bias from the zero x-axis intercept and C_{jCp} from the slope.**
- **Optimization to get the corresponding parameters.**



Process-specific parameter extraction - C_{CS}

- **Components to be considered:** $C_{jSi} \propto A_{CS}$ **and** $C_{jSp} \propto P_{CS}$ **, i.e.** $C_{CS} = A_{CS} \cdot C_{jSi0} + P_{CS} \cdot C_{jSp0}$
- **Measured test structures: a large area transistor, measured with CV meter, and several long-stripe transistors with different P/A ratios, measured with spot-frequency s-parameter technique.**
- **Obtain C_{jSi} for each bias from the zero x-axis intercept and C_{jSp} from the slope.**
- **Note that P_{CS} can be larger than the value from design rules (or mask) due to additional contributions at the perimeter (depending on process).**
- **Optimization to obtain the corresponding parameters.**

Extraction of transit-time from f_T

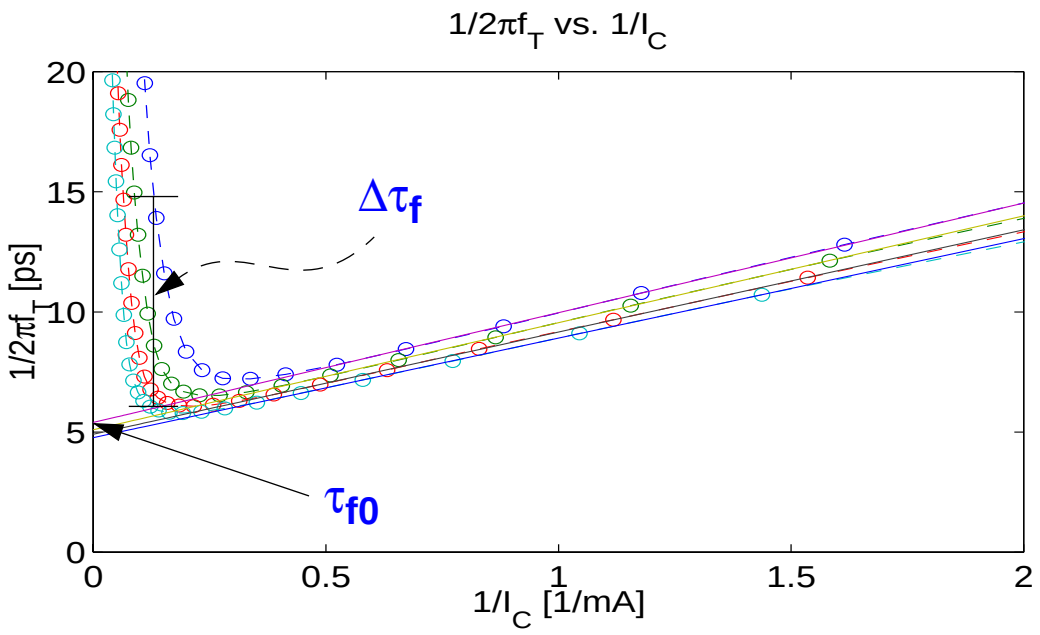
- Extract τ_f from f_T [8]
- Plot $1/(2\pi f_T)$ versus $1/I_C$.
- Extract low current τ_f, τ_{f0}, from the intercept of the straight lines at low current with y axis and applying

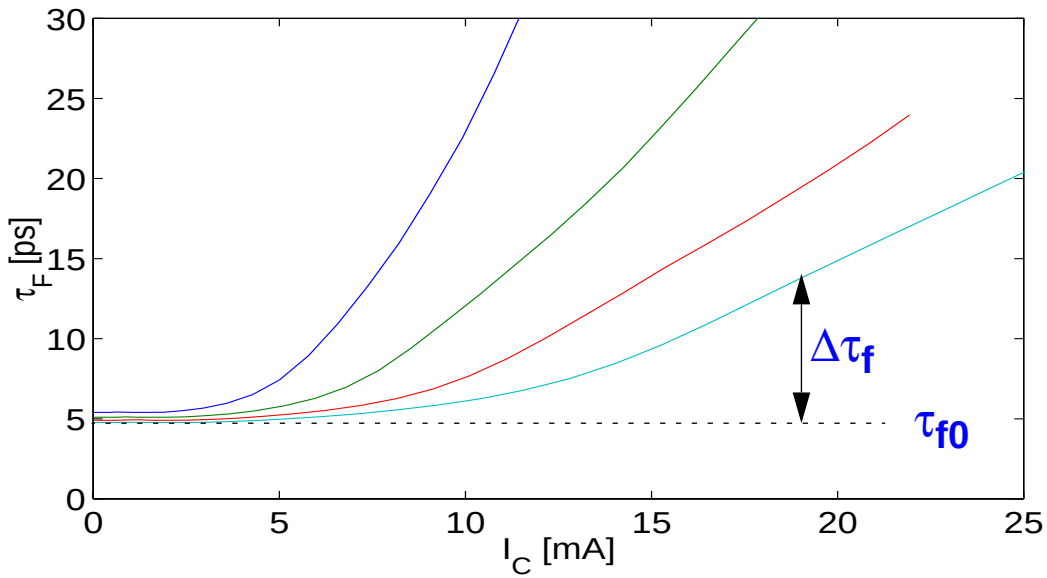
$$\tau_f = \frac{1}{2\pi f_T} - (R_{CX} + R_E)C_{CB} - \frac{\sum C}{g_m}$$

, giving τ_{f0}.

- Obtain $\Delta\tau_f$ at high current densities from the difference between the straight lines and $1/(2\pi f_T)$ data.
- Then the transit-time as a function of I_C and V_{CE} can be obtained as

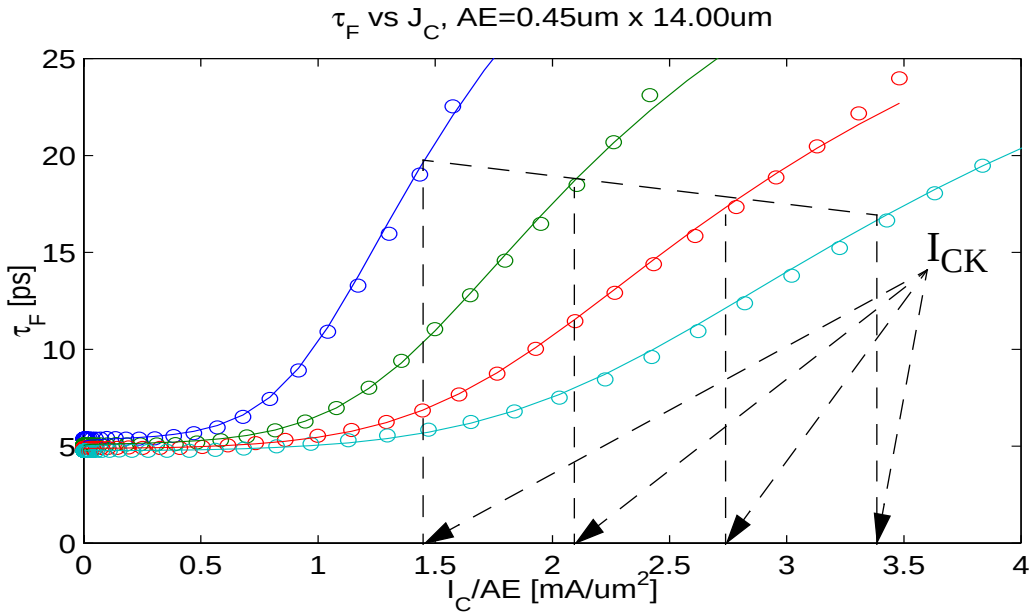
$$\tau_f(I_C, V_{CE}) = \tau_{f0} + \Delta\tau_f(I_C, V_{CE}).$$

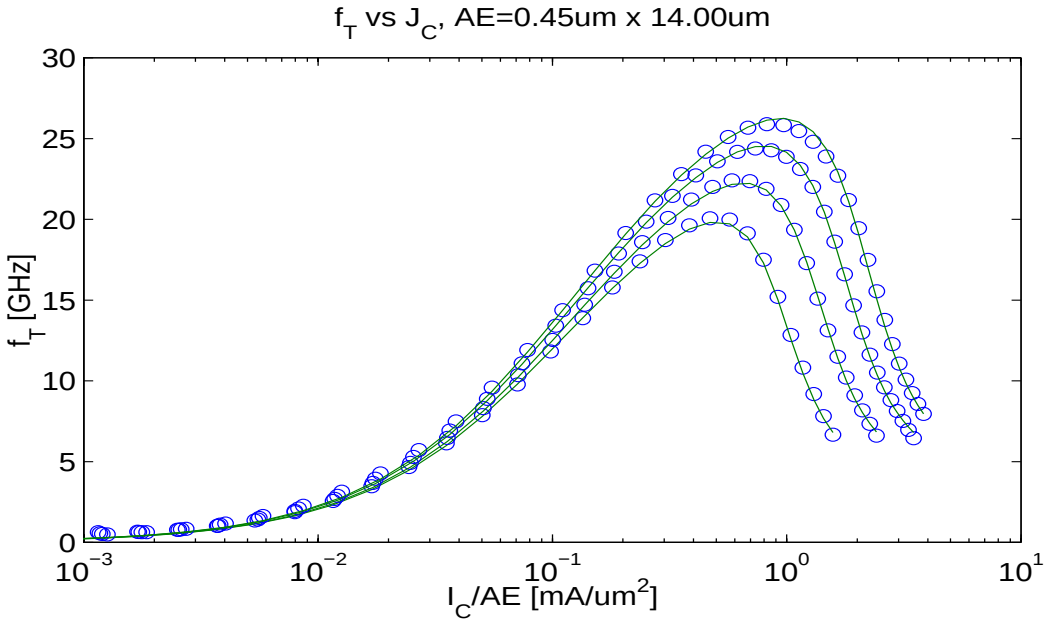




HICUM-specific parameter extraction - Transit-time

- Extract τ_{f0} vs. V_{CE} from low-current τ_f. (cf. next page)
- Extract I_{CK} vs. V_{CE} from , e.g., τ_f inflection points [9].

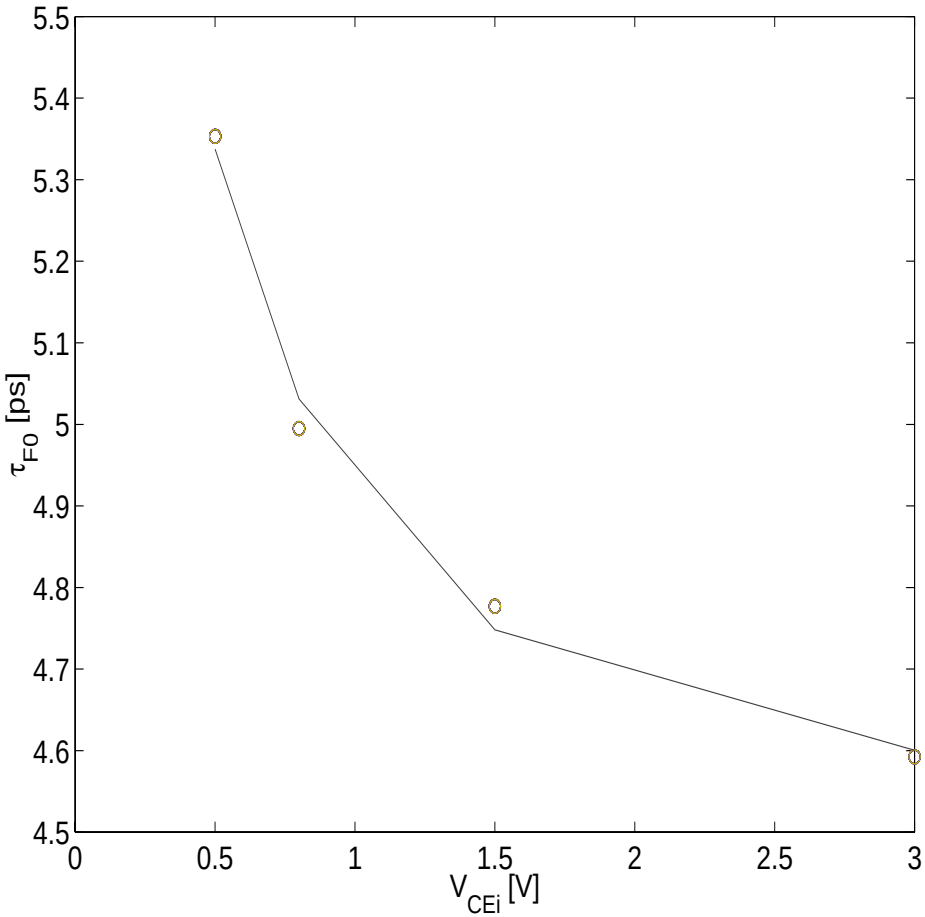




HICUM-specific parameter extraction (cont.) - Low-current transit-time parameters

- Low-current transit-time τ_{f0} parameters (τ_0, $d_{\tau 0h}$, and τ_{bvl}) are obtained through optimization of the τ_{f0} vs. V_{CE} curve.
- Geometry scaling of τ_{f0} is realized through the ratio of peripheral component to bottom portion of the low-current transit time τ_{f0}, τ_{p0}/τ_{i0} [10].

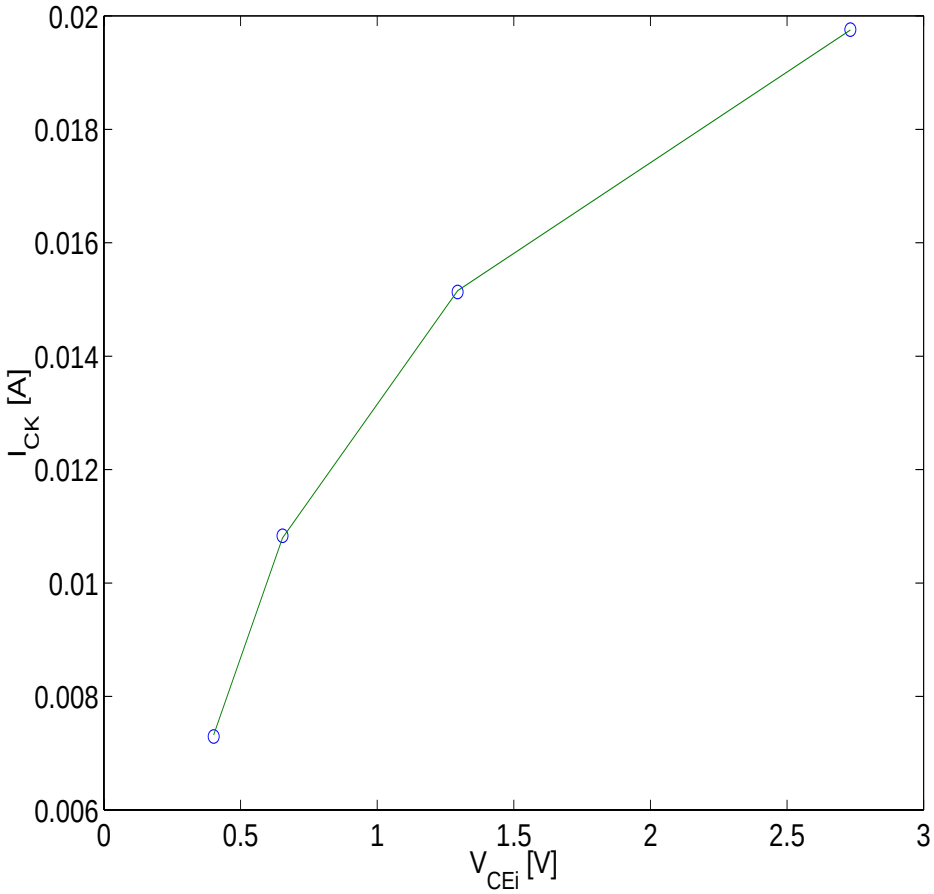
Fitting of τ_{f0}



HICUM-specific parameter extraction (cont.) - Critical current I_{CK} and high-current transit-time parameters

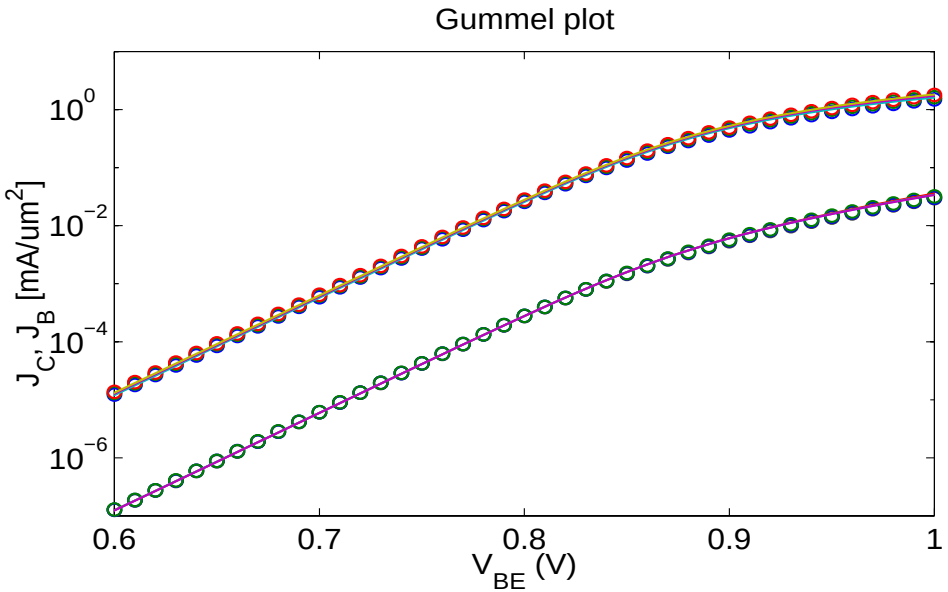
- I_{CK} parameters (r_{Ci0}, V_{lim}, V_{PT}, and V_{CEs}) are obtained through optimization of the I_{CK} vs. V_{CE} curve.
- Geometry scaling of I_{CK} is realized through the collector spreading angle δ_C. δ_C can be obtained by comparing the I_{CK} values extracted from transistors with different emitter sizes at a given V_{CE} [10].
- Then perform optimization to obtain high-current transit time parameters (τ_{Ef0}, $g_{\tau fE}$, τ_{hcS}, α_{hc}).

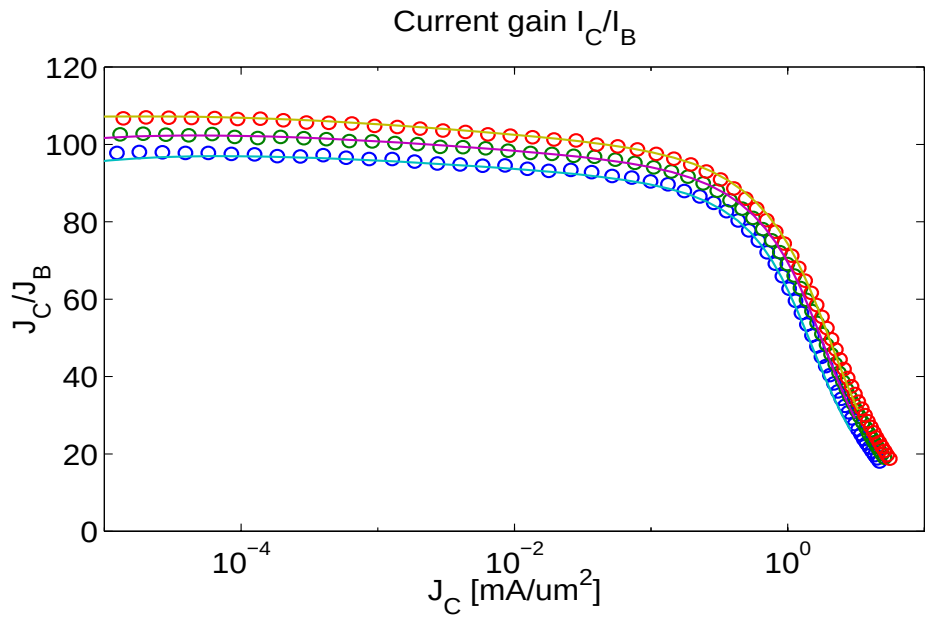
Fitting of I_{CK}



HICUM-specific parameter extraction - DC characteristics parameters

- Extract Q_{p0} from r_{Sbi} vs. bias
- Extract c10 at low collector current density (e.g. VBE=0.6.. 0.7V), where the influence of series resistance is negligible.
- Extract I_{ch} from high collector current
- Extract I_{BEi} and m_{BEi} from medium base current
- Extract I_{REi} and m_{REi} from very low base current region
- Extract h_{jCi} from forward Early effect
- Geometry scaling is realized through γ_C and γ_B (ratio of peripheral component to bottom component of specific collector and base currents)





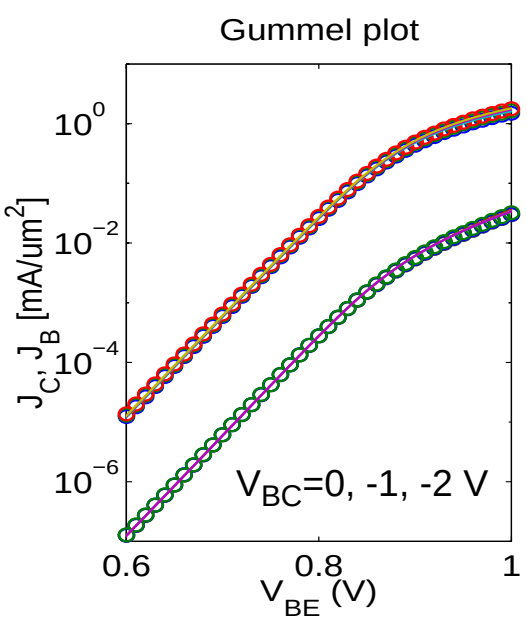
SGPM-specific parameter extraction - DC and Transit-time parameters

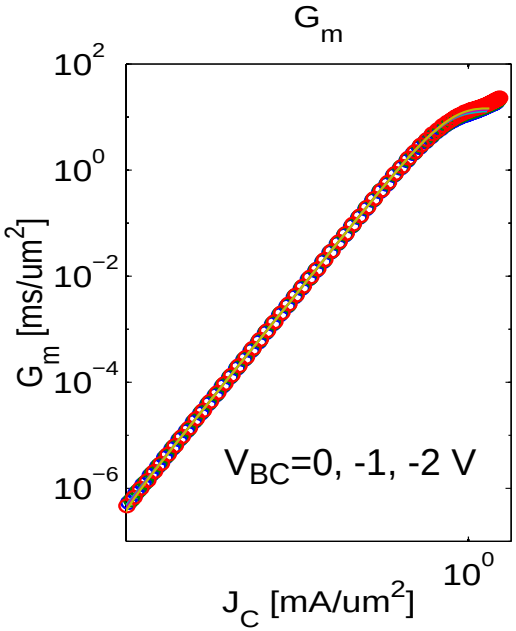
- Because SGPM couples f_T characteristics with intrinsic current-voltage characteristics, transport parameters need to be extracted first.
- Extraction of SGPM transport parameters is similar to that of HICUM.
- SGPM f_T parameters TF, XTF, VTF, and ITF are obtained from optimization, which is often a lengthy process.
- Geometry scaling is realized through γ_C and γ_B (ratio of peripheral component to bottom component of specific collector and base currents) and δ_C (collector spreading angle).

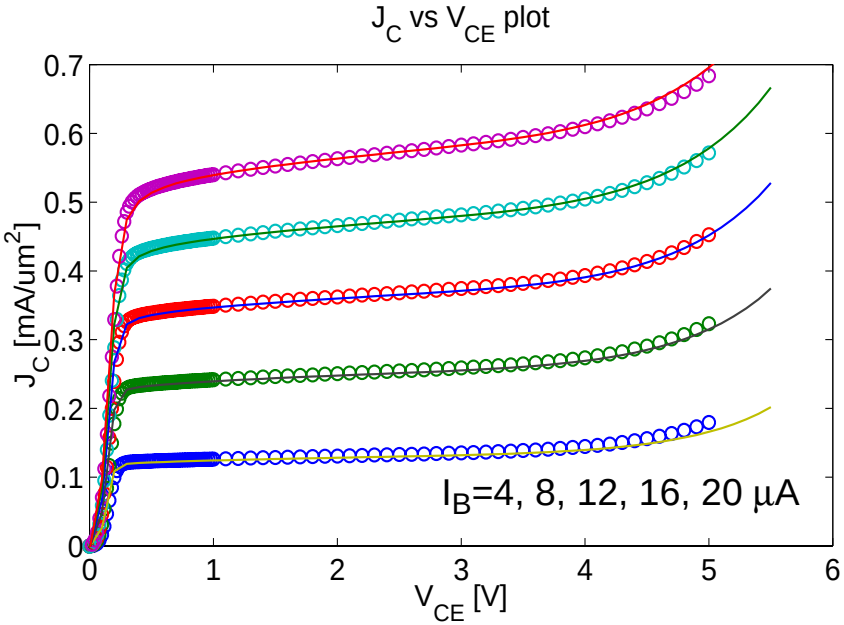
Model verification

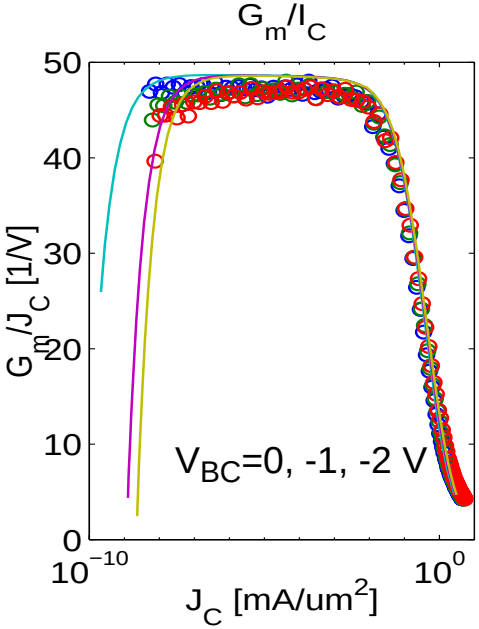
- **Model verification is performed simultaneously on transistors with different configurations to confirm the accuracy of the scalable model generation.**
- **Model verification can also be used to tune parameters which can not be precisely determined from previous steps (e.g. parameters for NQS effect).**
- **For design of RF applications, verification of a model should include**
  - DC characteristics: Gummel plot, transconductance g_m, output conductance g_o.
  - f_T vs. J_C at different V_{CE}
  - y-parameters @ freq=constant vs. J_C at different V_{CE}
  - y-parameters vs. frequency for different bias conditions
  - Temperature dependence
  - Noise (low and high frequencies)
  - Distortion
- **A process-based scalable parameter extraction methodology and its result when applied to industrial high-speed bipolar process are presented. For more results please refer to the material presented to the Compact Model Council CMC on Dec. 10, 1998 [11].**

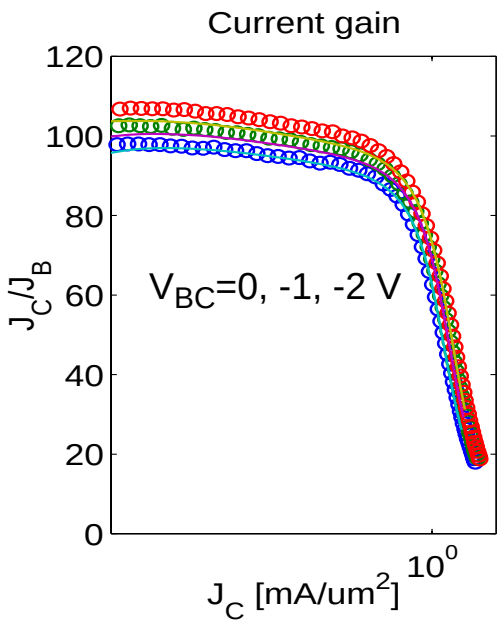
HICUM - DC Verification

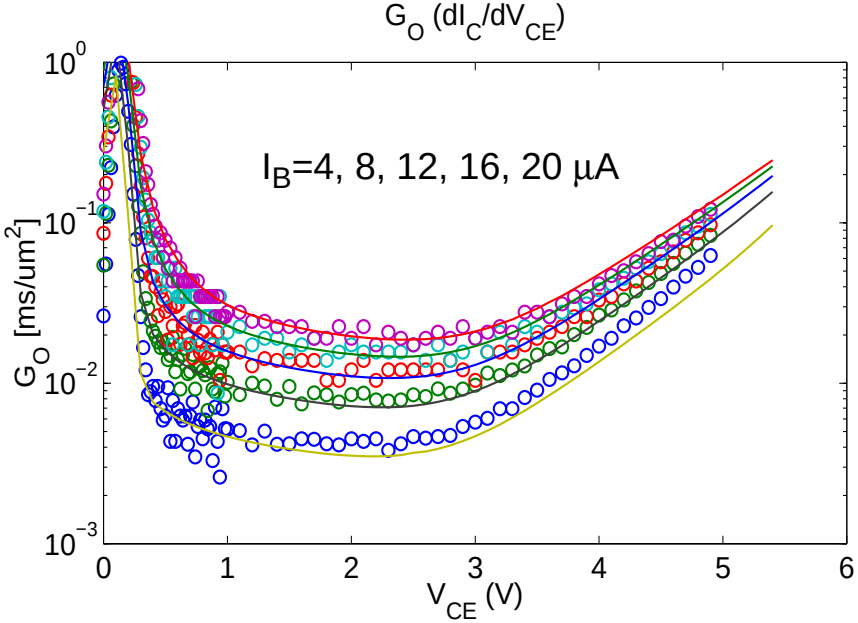






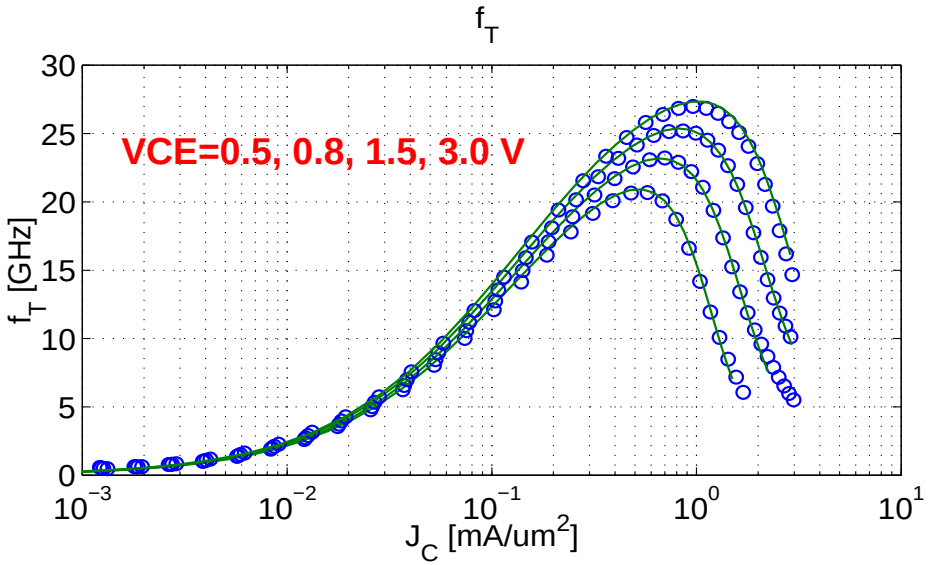


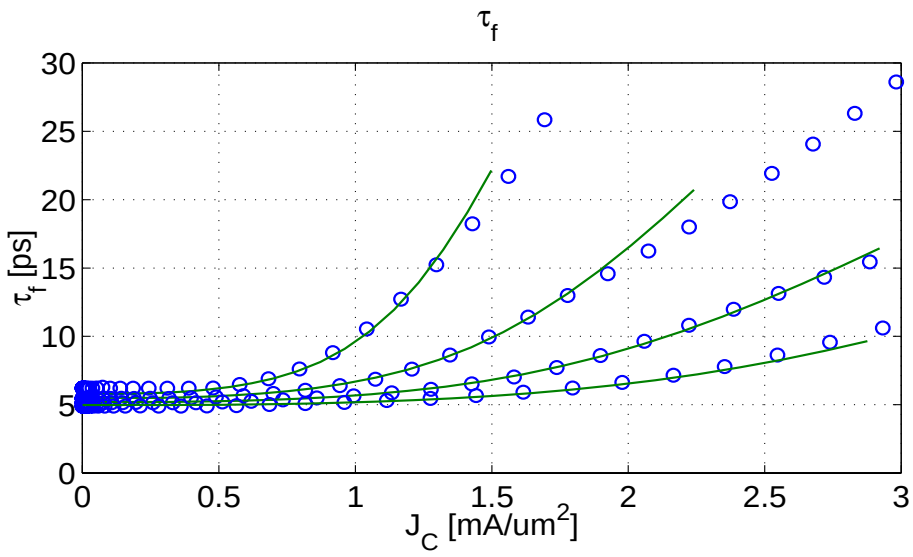




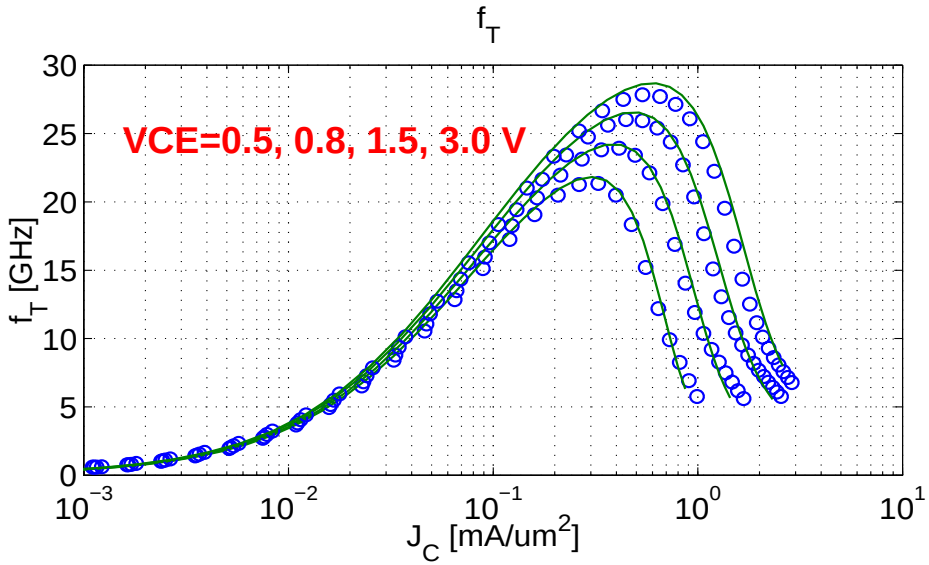
HICUM - f_T verification

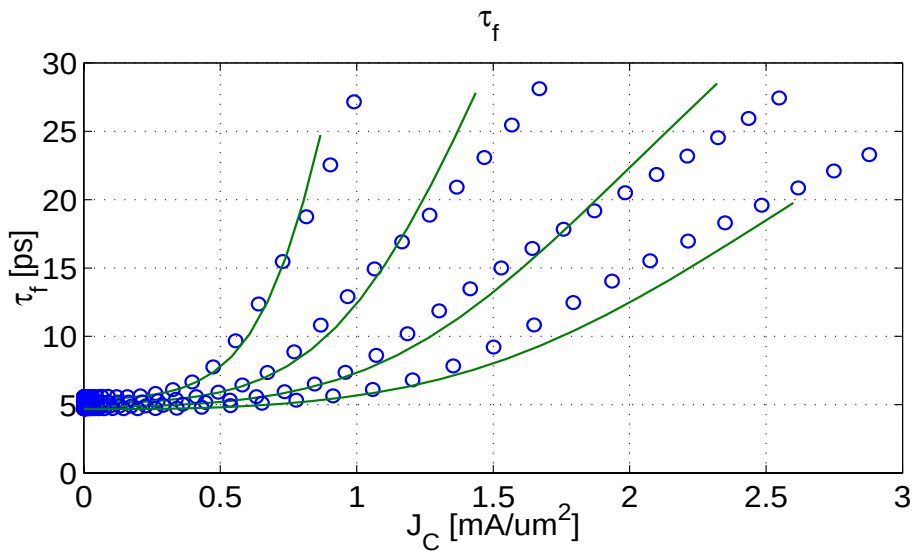
HICUM f_T characteristics A_{E0}=0.4μmx14μm





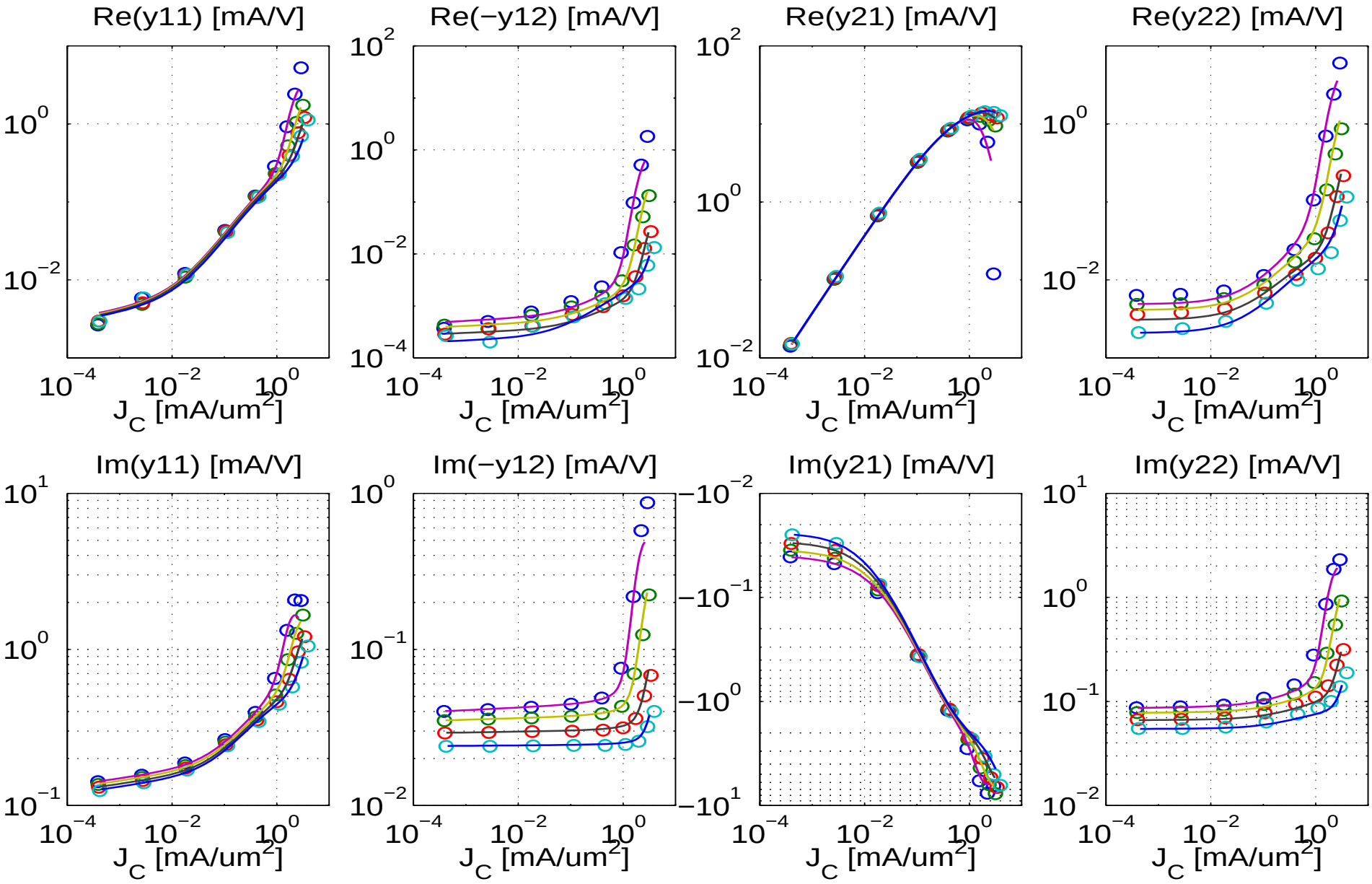
HICUM f_T characteristics A_{E0}=1.1μmx14μm





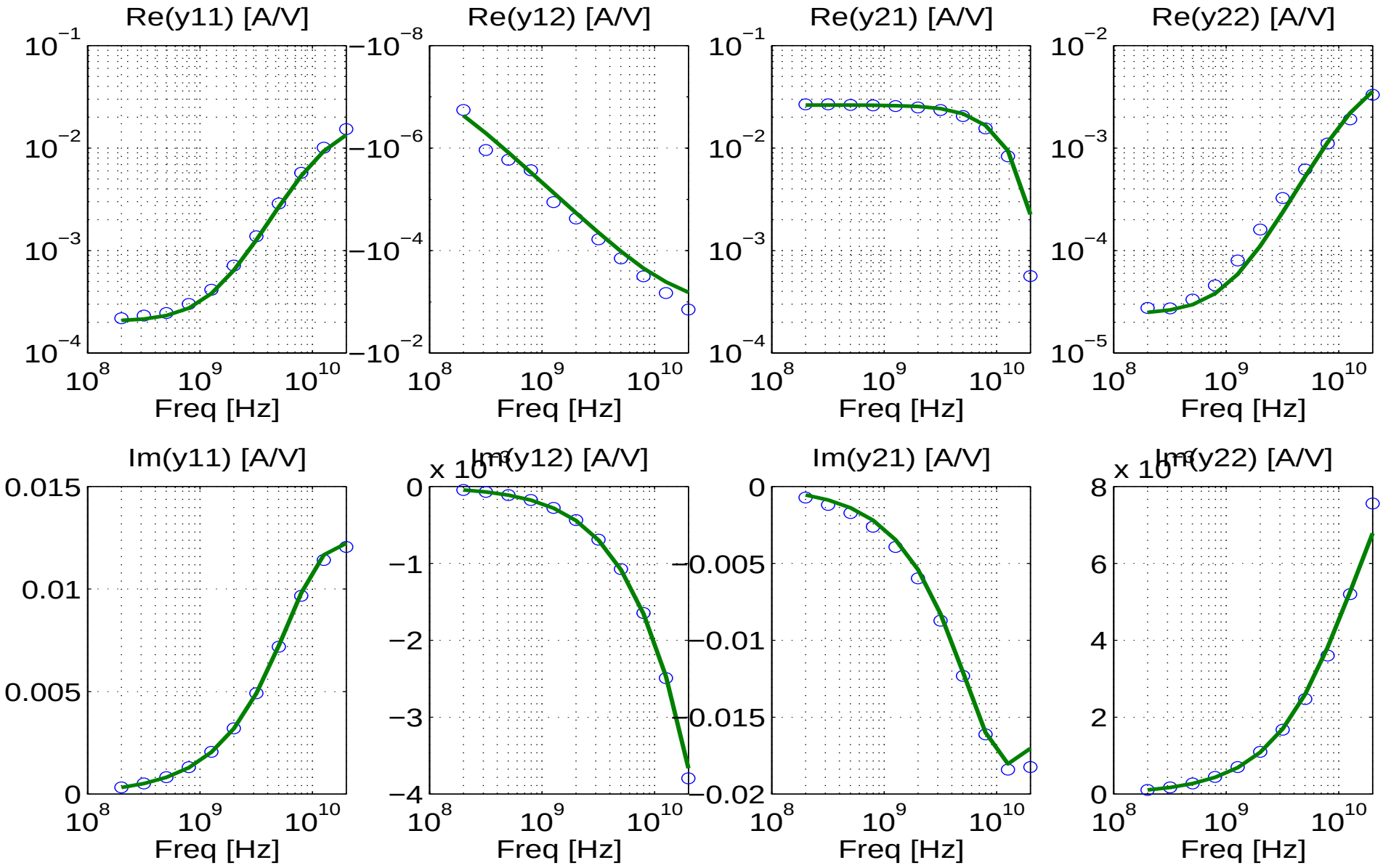
HICUM: Spot-frequency y-parameters vs. JC @ freq=1.0GHz

V_{CE}=0.5, 0.8, 1.5, 3.0 V



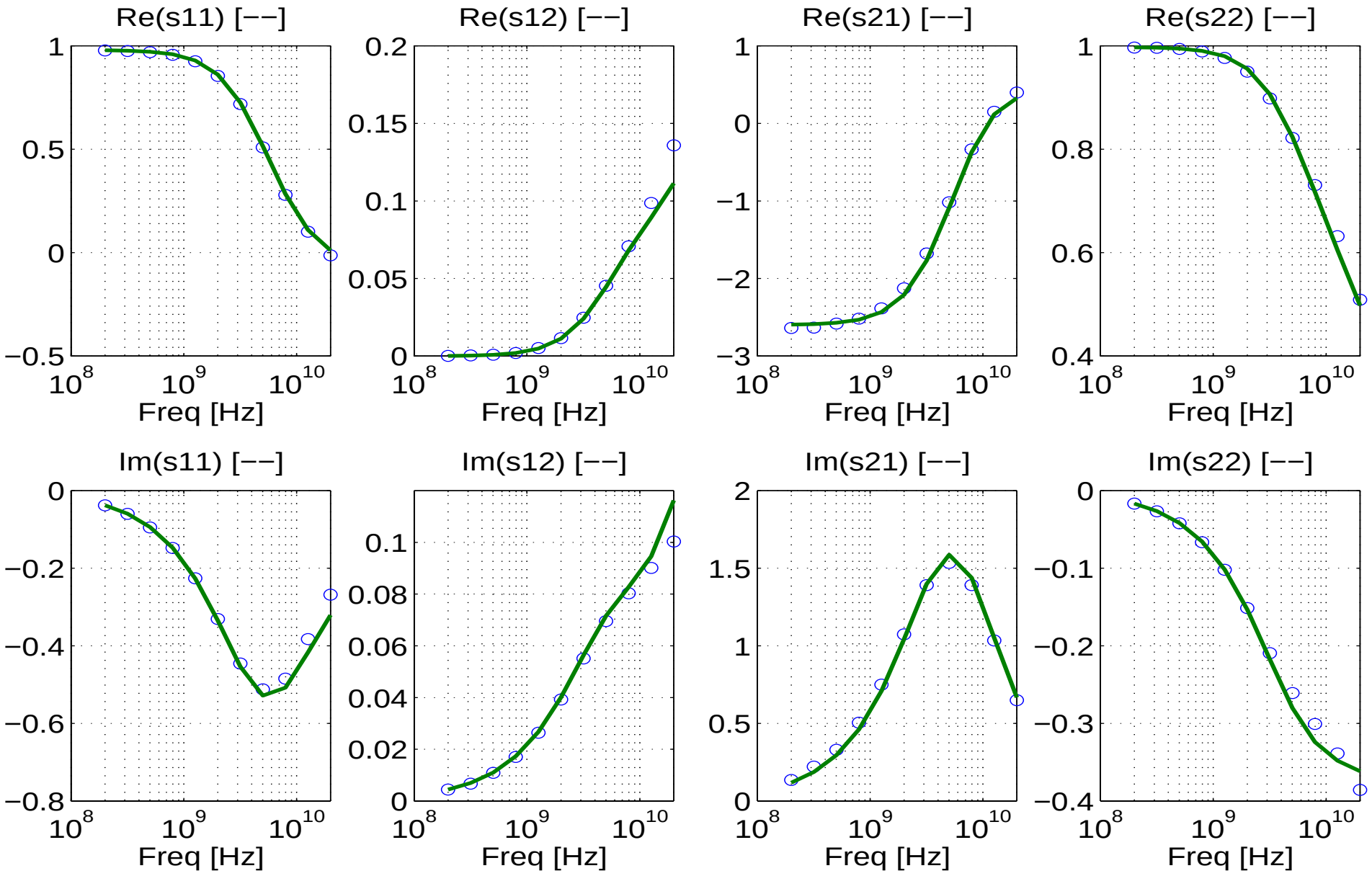
HICUM: Frequency-sweep y-parameter verification

V_{BE}=0.86V V_{CE}=0.8V J_C=0.11549mA/um^2 J_B=0.0008423mA/um^2



HICUM: Frequency-sweep s-parameter verification

V_{BE}=0.86V V_{CE}=0.8V J_C=0.11549mA/um^2 J_B=0.0008423mA/um^2



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