4.3.1 Device sizes and test structures

It is assumed that test structures for sheet resistances and contact resistances are available as, e.g., process monitors (PCM). For processes that are employed for high-frequency applications, large area capacitance test structures should also be available in PCMs. These structures have been included in the list for the sake of completeness. The selection of the particular die for the subsequent extraction related measurements should be based on the results obtained for the above PCMs.

The transistor configurations usually requested by designers span from the minimum size device with an area $b_{E,min}*l_{E,min}$ and a single base contact over single emitter transistors with $b_E \geq b_{E,min}$, $l_E \geq l_{E,min}$ as well as one or two base and collector contacts to multi-finger devices with $l_E \gg l_{E,min}$. This is illustrated in the b_E vs. l_E chart below. The multiplication factors are example values.

Transistors with longer emitter fingers ($\dot{l_E} \gg b_{E,min}$) usually have 2 base stripes per emitter and are also often realized in multi-finger configuration with n_E emitter stripes, $n_B=n_E+1$ base stripes, and 2 collector stripes or even a collector stripe at the emitter fore side. Model parameters for all these different configurations need to be generated and verified!

The emitter dimensions of the transistors that are selected for parameter extraction should fulfil the relation $l_E \gg b_E$ in order to enable accurate modeling of 2D effects. According to [Sch96], the extracted information can then also be used for modeling of 3D effects. The emitter length of these transistors should be chosen carefully to reduce self-heating and the related corrections as much as possible. Besides the minimum set of transistors, it is always useful to include few more transistor sizes in the parameter extraction; those structures should be selected according to the intended circuit applications. For instance, low-power CML circuits often employ minimum size transistors, while power amps and drivers employ multi-finger transistors with long emitters.

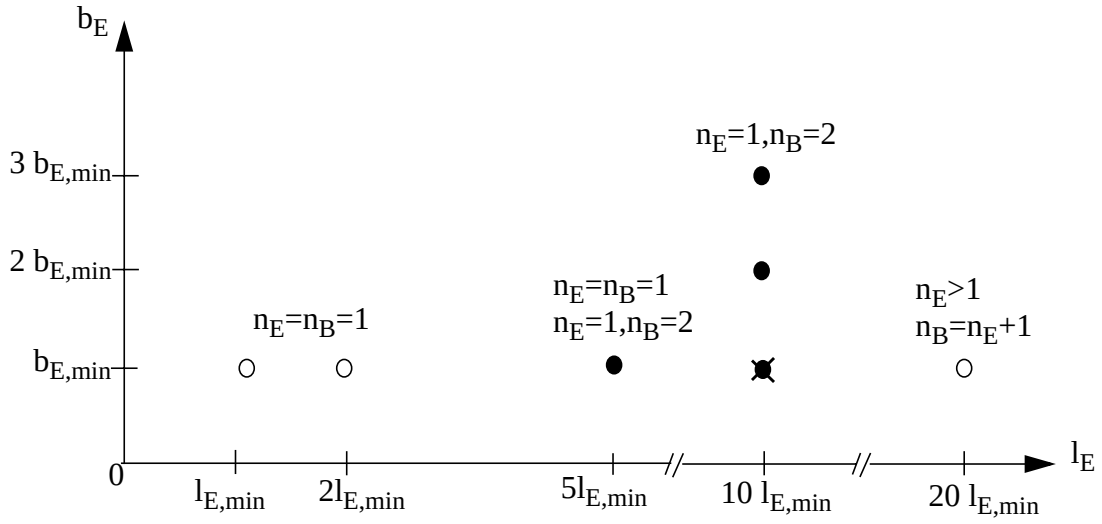

Fig. 4.3.1/1: Preferred distribution of emitter dimensions of test transistors used for geometry scaleable parameter extraction. Full circles indicate required test structures, open circles indicate optional structures recommended for model parameter verification. The cross indicates the “reference” transistor. Scaling factors are examples and depend on the process.

4.3.2 Measurements

A few remarks are necessary concerning the measurement specification listed below:

- The extraction sequence and some basic test structures are described in the web-document [Lee99].
- All measurements should be taken from the same location (die) of a chip.
- To generate scaleable model parameters, the dimensions of the measured devices have to be known. In most cases, design rules and mask biases are sufficient. For the emitter-base and base-collector region, however, SEM photos are preferred to obtain as accurate as possible structural data.
- S-parameters are preferred to be provided as “raw” data, i.e. not de-embedded. As a consequence, data of the corresponding OPEN (and SHORT) structures are also required not only for de-embedding but also for checking the quality of the measurements. This way, effort for extracting model parameters on inconsistent or incorrect data can be avoided.
- Measurement conditions are given for Si-based processes.
- Measurement time for parameter extraction can be reduced by determining fT (and related characteristics) from “spot-frequency” measurements rather than full frequency sweeps. However, the integration time has to be sufficiently long to ensure accuracy. For full frequency sweeps, certain bias points can be selected for later verification.

#	type and conditions	data	result
1	• internal base pinch resistance from at least 3 structures with different b_E; V_{BE}=[-0.5,0.5]V @ V_{CE}=0, ΔV_{BE}=0.1V, ΔV_{BB}=0.01V • sheet and contact resistances of ext. base region, buried layer, collector (sinker, contact)	V_{BE} I_{B1} I_{B2} ΔV I (or r_S, r_{con} ...)	base and collector series resistance components
2	• C-V on large area transistor V_{BE}=[-0.5,0.5]V, V_{BC}=V_{SC}=0, ΔV_{BE}=0.1V V_{BC}=[-5,0.5]V, V_{BE}=V_{SC}=0, ΔV_{BC}=0.1V V_{SC}=[-5,0.5]V, V_{BE}=V_{BC}=0, ΔV_{SC}=0.1V • C-V on large area BC diode (only for transistors with selectively implanted collector) V_{BC}=[-5,0.5]V, V_{BE}=V_{SC}=0, ΔV_{BC}=0.1V	V_{BE} C_{jE} V_{BC} C_{jC} V_{SC} C_{jS} V_{BC} C_{jC}(epi)	depletion and parasitic dielectric capacitance components
3	cold S-parameters on ≥ 3 transistors (diff. b_E << l_E) V_{BE}=[-0.5,0.5]V, V_{BC}=0, ΔV_{BE}=0.1V V_{BC}=[-5,0.5]V, V_{BE}=0, ΔV_{BC}=0.1V	V_{BE} S V_{BC} S	depletion and par. dielectric capacitance components
4	S-parameters on at least 3 transistors (diff. b_E << l_E) I_C/A_E=[0.01,1]mA/μm^2 (max. dep. on process) and (at least) 3 V_{CE}, e.g. V_{CE}/V=0.5,1.5,3 for a high-speed process with BV_{CEO}>3V	V_{BE} V_{CE} I_C I_B S	f_T, τ_f, certain forward I-V parameters; verification
5	d.c. output characteristics (reference transistor only) V_{CE}=[0V, $V_{CE,max}$] @ I_B=const / V_{BE}=const ($V_{CE,max}$<BV_{CEO}(high I_C/A_E)) I_C/A_E=[0.01,1]mA/μm^2 (dep. on process)	V_{CE} I_C I_B V_{BE}	Avalanche, certain I_C parameters; verification
6	d.c. reverse characteristic (reference transistor only) V_{BC}=[0.4, 0.8]V @ V_{BE}=0V	V_{BC} I_B [I_C]	BC diode
7	Temperature dependence: T=[-40, 75, 125] ^{o}C • repeat 1 for all relevant resistances • repeat 4 for ref. transistor (only one V_{CE} value is required for extraction)		

Table 4.3.2/1: Measurement type and sequence for extraction of geometry scaleable model parameters (HICUM and SGPM) for T_{ref} (e.g. = 300K). Only the minimum number of measurements is specified, and more data is always useful.