HICUM

-

A scalable physics-based compact bipolar transistor model

Michael Schroter

Description of model version 2.1

December, 2000

List of often used symbols and abbreviations

A_{E0} , L_{E0}	emitter window area and perimeter
A_E , L_E	effective (electrical) emitter area and perimeter
b_{E0} , l_{E0}	emitter window width and length
b_E , l_E	effective (electrical) emitter width and length (for definition see [Rei83, Sch96])
γ_C	ratio of periphery to area specific collector current; equal to emitter width increase due to periphery injection, e.g. $b_E = b_{E0} + 2\gamma_C$
I_T , i_T	DC and time dependent transfer current of the vertical npn transistor structure
I_{CK}	critical current (indicating onset of high-current effects)
μ_n, μ_p	electron (hole) mobility
N_{Ci}	(average) collector doping under emitter
N_{Cx}	collector doping under external base
w_B ,w_{B0}	neutral/metallurgical base width
w_{Ci}	(effective) collector width under emitter
w_{Cx}	(effective) collector width under external base
w_i	width of collector injection zone (for charge storage calculation in collector region)
GICCR	Generalized Integral Charge-Control Relation

1 Introduction

1.1 Preliminary remarks

The purpose of the following remarks is to provide (i) a motivation behind the compact modeling approach pursued with HICUM, (ii) an overview on its targeted application area, and (iii) a list of requirements for a compact model from different point of views

Bipolar technology has recently seen a tremendous growth, fuelled mostly by applications that require high speed and driving power on one hand and low noise and distortion on the other hand. Presently, major applications of bipolar technology are:

- Wireless communications in the 0.9 to 2.4 GHz range for, e.g. GSM, GPS, DECT, in the 4-12 GHz range for, e.g. satellite TV, WLAN, and in the 20 to 60GHz range for short range communications, with the first application dominating.
- Fiber-optic communications in the 5 to 40 Gb/s range for, e.g. fast internet access and data transfer (LAN, WAN) as well as TV/HDTV (FTTC, FTTH); production and related design has started for systems up to 10Gb/s, seeing a significant push also for higher integration, such as cross-point switches in BiCMOS processes with emphasis on low-power high-speed bipolar circuits. Systems operating at 40Gb/s are already coming close to deployment.
- “Linear analog” circuits for, e.g. disc drives, consumer electronics in general, power and automotive electronics. Many of these components require reliable and well-established processes with higher breakdown voltages rather than advanced high-speed bipolar processes.
- Fast data acquisition and conversion (ADCs) for, e.g., instrumentation and measurement equipment.
- Advanced automotive components at very high frequencies in the 24 to 77 GHz range for, e.g. collision warning and avoidance. The respective circuits so far have been realized in III-V processes, such as HBTs.

The above sequence is assumed to be roughly in the order of present importance from a business point of view; exact breakdowns are difficult to find, and the ranking can change quickly in areas of rapid growth. The first two applications are perceived to comprise the largest number of designs. As a consequence, compact bipolar transistor modeling should focus on these areas which, fortunately, include most of the critical issues of the second two applications.

Compact modeling is also strongly connected to development and deployment of process technologies. A physics-based compact model together with the related parameter extraction and generation methodology can contribute significantly to improving the alignment of process development with product design needs by enabling quick evaluations of the impact of process

changes on device and circuit performance. (Compact) modeling basically provides a link between processing and design.

In general, bipolar processes span quite a variation in device structure but also device types. It is recommended to split compact bipolar models into at least two categories:

- vertical devices including high-speed npn transistors
- lateral devices, mostly pnp transistors.

HICUM is targeted towards the first category. It might be necessary though to divide the first category again into “low-power” ($BV_{CEO} < 10V$) and “high-power” ($BV_{CEO} > 10V$) transistors if the difference in device design and the electrical application range turns out to be too large for a single model. So far, HICUM has been verified to be accurate for transistors with BV_{CEO} values up to about 15V.

From the above, the following requirements for a compact model can be derived from an industrial point of view:

- high accuracy over a wide electrical (and temperature) range;
- laterally scalable parameter calculation, including variable contact configurations, in order to allow circuit optimization;
- numerical stability and fast execution time, although this is somewhat dependent on the application.
- physics-based, allowing predictive and statistical modeling;
- reliable and well-defined extraction procedure should be available together with test structures; also, the use of standard equipment and set ups only is important for, e.g., fast throughput.
- modular formulation of the model equations, minimizing interrelations between different electrical regions and facilitating simple implementation into circuit simulators.

Since the limitations of the standard SPICE Gummel-Poon model (SGPM), especially for designing high-speed circuits, have been well-known for many years (cf. examples in [40]), the advanced model HICUM has been developed.

1.2 Model features overview

HICUM is a semi-physical compact bipolar transistor model. Semi-physical means that for arbitrary transistor configurations, defined by emitter size as well as number and location of base, emitter and collector fingers (or contacts, respectively), a complete set of model parameters can be calculated from a single set of technology specific electrical and technological data (cf. [42]). For this, the value of each element in the equivalent circuit is related to a function describing the dependence on so-called specific electrical data (such as sheet resistances and capacitances per area or length), technological data (such as width and doping of the collector region underneath the emitter), physical data (like mobilities), transistor dimensions (such as design rules), operating point, and temperature. The availability of such a semi-physical compact model is an important precondition for circuit optimization with respect to, e.g., maximum speed and low power consumption as well as for including process variations in the design.

The name HICUM was derived from *hi*gh-*cu*rrent *m*odel, indicating that HICUM initially was developed with special emphasis on modelling the operating region at high current densities which is very important for certain high-speed applications. The first version was described in detail in [30,45,25,31,32] and was verified for digital applications based on a conventional technology. Later, formulas for the calculation of the base resistance were developed [26,33,34] which include three-dimensional effects occurring in short transistors with an emitter length approaching the emitter width. The latter sizes are important for low-power designs. The introduction of self-aligning poly-silicon technologies as well as the extension of the model to high-frequency analog operation led to improvements [28,13] w.r.t. the first version, which were also verified for very fast large-signal digital-type applications [37].

HICUM is based on an extended and generalized Integral Charge-Control Relation (GICCR) [29,24,31,35]. However, in contrast to the (original) Gummel-Poon model (GPM) [1] as well as the SPICE-GPM (SGPM) [2] and its variants, in HICUM the (G)ICCR concept is applied consistently without inadequate simplifications and additional fitting parameters (such as the Early voltages). Since reliable design and optimization of high-speed circuits requires accurate modeling mainly of the dynamic transistor behavior, quantities like depletion capacitances and the transit time of mobile carriers as well as the associated charges, which determine the dynamic behaviour, are considered as basic quantities of the model. An accurate approximation of these basic quantities as a function of bias yields, thus, not only an accurate description of the small-signal and dynamic large-

signal behaviour but also - via the (G)ICCR [35] - of the d.c. behaviour. This coupling between static and dynamic description leads, moreover, to a reduction of "artificial" model parameters like Early voltages and knee currents. Furthermore, the above mentioned basic quantities can be easily and accurately determined by standard small-signal measurement methods.

The modularity and physics-based approach of HICUM allows the construction of a model hierarchy without additional effort in parameter extraction. Based on HICUM Level2 (HICUM/L2) and its corresponding set of specific electrical parameters, a simplified version HICUM Level0 (HICUM/L0) with the same equivalent circuit as the SGPM is being developed. In contrast to the latter though, HICUM/L0 eliminates many problems while maintaining similar overall simplicity. A detailed discussion of the simplified model version and the motivation behind will be given in Chapter 2.2, once the development has been completed. The HICUM/Level0 model is not yet available in commercial simulators.

The important physical and electrical effects taken into account by HICUM/L2, which is described in Chapter 2.1, are briefly summarized below:

- high-current effects (incl. quasi-saturation)
- distributed high-frequency model for the external base-collector region
- emitter periphery injection and associated charge storage
- emitter current crowding (through a bias dependent internal base resistance
- two- and three-dimensional collector current spreading
- parasitic (bias independent) capacitances between base-emitter and base-collector terminal
- vertical non-quasi-static (NQS) effects for transfer current *and* minority charge
- temperature dependence and self-heating
- weak avalanche breakdown at the base-collector junction
- tunneling in the base-emitter junction
- parasitic substrate transistor
- bandgap differences (occurring in HBTs)
- lateral scalability

Modelling of these effects is reflected not only in the model equations but also in the topology of the equivalent circuit. Although the above listed effects are taken into account, the standard HICUM/L2 equivalent circuit still corresponds to a one-transistor model (see Fig. 2.1.1/1), which has turned out as sufficiently accurate for the vast majority of circuit applications. HICUM/L2 contains elements for describing the internal transistor (index i), the emitter periphery (index p) and the external transistor regions (index x). The internal transistor is defined by the region under the

emitter which is assigned an effective emitter width [23,38] and area, respectively, in order to retain a one-transistor model with an as simple as possible equivalent circuit topology as well as a sound physical background. In contrast to MOS transistor models, the geometry dependent calculations have been implemented in a separate program (TRADICA, cf. [42]) for various reasons.

Due to its semi-physical nature HICUM/L2 possesses geometry scaling capabilities up to high current densities [38]. In order to make use of these scaling capabilities specific parameters have to be determined from measurements, for which instructions have been developed (e.g., [22,25,27,14, 15]. Parameter extraction as well as generation of model parameters for different transistor configurations will be addressed in Chapter 4.

Since HICUM has been developed for high-speed applications, in the public domain version described in this document only minimal effort has been made to *very* accurately describe the inverse (or reverse) operating region defined by VCE $<$ 0. The model formulations are extended in a simple way into that bias region in order to ensure numerical stability. Information on model availability in (commercial) circuit simulators is provided in Chapter 5.

As the experimental results in chapter 6 show, the accuracy and applicability of HICUM has been demonstrated for a variety of different technologies, ranging from a low-speed and relatively high-voltage process to present SiGe production processes, as well as for many different operating modes.

2 Model equations

In the following text all equations that are actually used in the implemented model code are marked by frame. The physical background of the equations is briefly discussed and references for more detailed explanations are provided. The model equations are discussed on the basis of a vertical npn transistor. The 2-transistor model can be easily applied to a vertical pnp transistor, but requires for most processes the addition of a second parasitic transistor (e.g. in a subcircuit).

The presently available version of HICUM (named HICUM/Level2) includes many physical effects that are relevant for today´s silicon-based processes (incl. SiGe technologies). As a consequence, its equivalent circuit is fairly complicated and not well-suited for rough analytical calculations often performed by circuit designers in the preliminary design phase. Therefore, a strongly simplified version of the model, called HICUM/Level0, is intended to be offered in near future. The combination of these different levels of complexity during circuit design is expected to also save computational effort and time.

2.1 HICUM/Level2

2.1.1 Equivalent circuit

Compared to the SGPM the equivalent circuit (EC) of HICUM/Level2 contains two additional circuit nodes, namely B* and S' in Fig. 2.1.1/1. The node B*, which separates the operating point dependent internal base resistance from the operating point independent external component, is required to take into account emitter periphery effects, which can play a significant role in modern transistors. This node is also employed for an improved modelling of the distributed nature of the external base-collector (BC) region by splitting the external BC capacitance C_{BCx} over r_{Bx} in form of a π-type equivalent circuit for the corresponding RC transmission line(s). As a further advantage of introducing the node B*, high-frequency small-signal emitter current crowding can be correctly taken into account by the capacitance C_{rBi}. An emitter-base isolation capacitance C_{Eox}, that becomes significant for advanced technologies with thin spacer or link regions, as well as a BC oxide capacitance C_{Cox}, which is included in the C_{BCx} element, are taken into account.

In contrast to other models, the influence of the internal collector series resistance is (partially) taken into account by the model equations for the transfer current i_T and the minority charge which is represented by the elements C_{dE} and C_{dC} in Fig. 2.1.1/1. As a consequence, the collector terminal C' of the internal transistor is (physically) located at the end of the epitaxial (or n-well) collector region. This approach not only avoids additional complicated and computationally expensive model equations for an "internal collector resistance" but also saves one node. The chosen approach has been demonstrated to be accurate for a wide range of existing bipolar technologies (cf. chapter 6)

The reliable design of high-speed circuits often requires the consideration of the coupling between the buried layer and the substrate terminal S. Since the substrate material consists of both a resistive and capacitive component, as a first (rough) approach a substrate network with a resistance r_{Su} and a capacitance C_{Su} is introduced, leading to the “internal” substrate node S*.

A possibly existing substrate transistor has been taken into account by using a simple transport model. Like in the SGPM, this can also be realized by a subcircuit (cf. Section 2.1.12) and setting r_{Su} and C_{jS} to zero in the HICUM equivalent circuit. In advanced bipolar processes, the emitter terminal of the substrate transistor (B*) moves towards the (npn) base contact (B) which makes the external realization of such a parasitic transistor by a subcircuit even easier. The substrate transistor

- if it is not avoided by proper layout measures - only might turn on for operation at very low CE voltages (“very” hard saturation).

The physical meaning and modelling of all EC elements in Fig. 2.1.1/1 is discussed below in more detail.

The description in the following text is given for a npn transistor, which is mostly used type of bipolar transistors. For vertical pnp transistors, the model can be applied by interchanging the signs of terminal voltages and currents. Lateral pnp transistors could be described by a composition of HICUM/L2 models but usually a subcircuit consisting of three simple transport models (e.g. HICUM/0) is considered to be more appropriate.

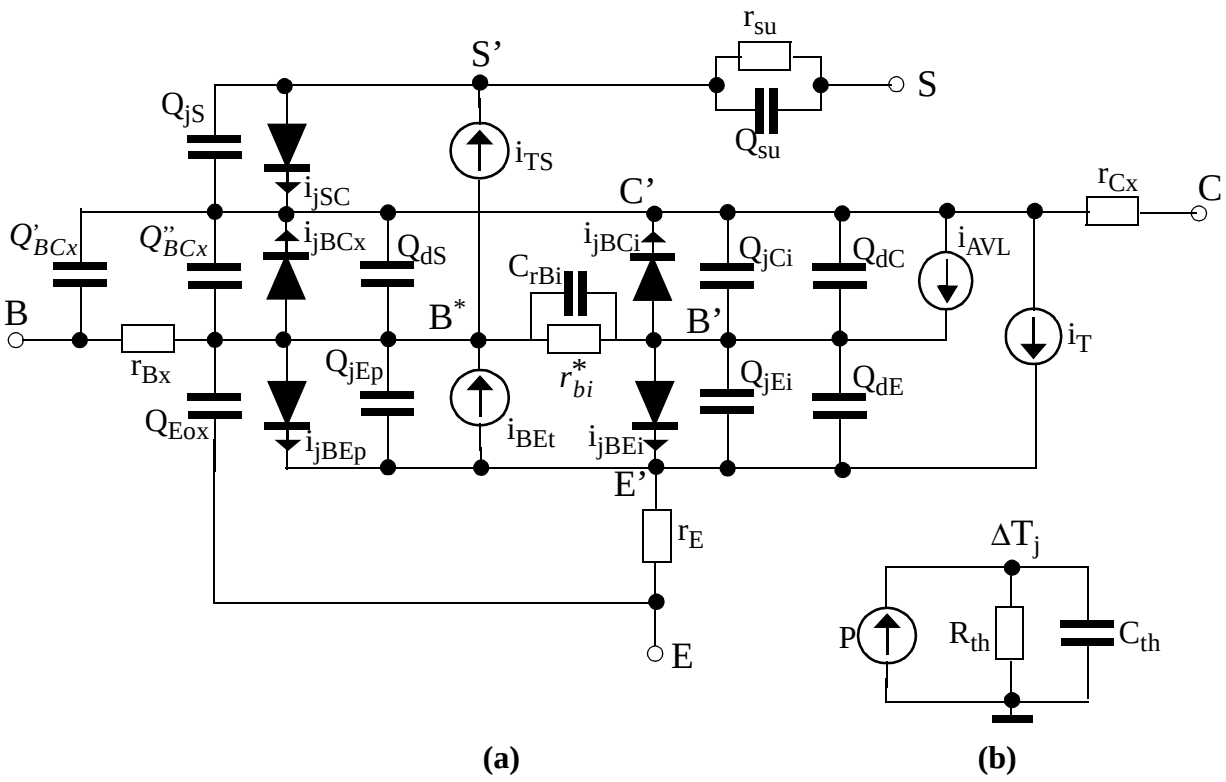


Fig. 2.1.1/1: (a) Large-signal HICUM/Level2 equivalent circuit. The external BC capacitance consists of a depletion and a bias independent (e.g., oxide) capacitance with the ratio C'_{BCx}/C''_{BCx} being adjusted with respect to proper modelling of the h.f. behavior.
(b) Thermal network used for self-heating calculation.

2.1.2 Quasi-static transfer current

The transfer current of a vertical homo- and hetero-junction transistor can be described by a generalized form of the ICCR that can also be extended to 2D and 3D transistor structures with narrow emitter stripes or very small contact windows. The various steps to arrive at the final equation for the transfer current i_T are outlined below, demonstrating the modular structure of the model equations.

A. Basic formulation

The result of the one-dimensional (1D) GICCR is

$$i_T = \frac{c_{10}}{Q_{p,T}}\left[\exp\left(\frac{v_{B'E'}}{V_T}\right) - \exp\left(\frac{v_{B'C'}}{V_T}\right)\right] \tag{2.1.2-1}$$

with the constant

$$c_{10} = (qA_E)^2 V_T \overline{\mu_{nB} n_{iB}^2} \quad . \tag{2.1.2-2}$$

As discussed in the Appendix, $v_{B'E'}$ and $v_{B'C'}$ are the (time dependent) terminal voltages of the 1D transistor if the integration leading to the modified hole charge, $Q_{p,T}$, is performed throughout the total 1D transistor, i.e. between its emitter and collector contact. $\overline{\mu_{nB} n_{iB}^2}$ is an average value for the base region.

$Q_{p,T}$ consists of a *weighted* sum of charges,

$$\boxed{Q_{p,T} = Q_{p0} + h_{jEi} Q_{jEi} + h_{jCi} Q_{jCi} + Q_{f,T} + Q_{r,T}}\,, \tag{2.1.2-3}$$

The charge formulations designated with the index “T” result when the transfer current is derived from the transport equation and hetero-junctions as well as current spreading are included. The hole charge at thermal equilibrium, Q_{p0}, is a model parameter. Q_{jEi} and Q_{jCi} are the depletion charges stored within the BE and BC junction. $Q_{f,T}$ and $Q_{r,T}$ are (weighted) minority charges stored in the total (1D) transistor [35]. The various components in the minority charges and the weighting factors will be discussed in more detail later.

The correspondence to the conventional model formulation can be maintained by realizing that the usual collector saturation current is simply given by

$$I_S = \frac{c_{10}}{Q_{p0}} \quad , \tag{2.1.2-4}$$

so that (2.1.2-1) can also be written in normalized form

$$i_T = \frac{I_S}{Q_{p,T}/Q_{p0}}\left[\exp\left(\frac{v_{B'E'}}{V_T}\right) - \exp\left(\frac{v_{B'C'}}{V_T}\right)\right] . \tag{2.1.2-5}$$

Mathematically, i_T in (2.1.2-1) equation can be split into a "forward" component,

$$i_{Tf} = \frac{c_{10}}{Q_{p,T}}\exp\left(\frac{v_{B'E'}}{V_T}\right) \tag{2.1.2-6}$$

and a "reverse" (better: inverse) component,

$$i_{Tr} = \frac{c_{10}}{Q_{p,T}}\exp\left(\frac{v_{B'C'}}{V_T}\right) , \tag{2.1.2-7}$$

which will be referred to in the discussion below. Physically, i_{Tf} represents the electron current flowing from emitter to collector at forward operation at $\exp(V_{C'E'}/V_T) >> 1$. Analogously, i_{Tr} represents the electron current flowing from collector to emitter at inverse operation with $\exp(-V_{C'E'}/V_T) >> 1$. This separation of i_T simplifies both the implementation of the solution of the non-linear transfer current formulation as well as the modelling of the minority charge components.

B. Extension to the 2D (3D) case and influence of internal base resistance

The 1D transistor structure can be transformed into a 2D or 3D structure by multiplying all area specific 1D model parameters with the emitter area of the transistor. This defines the internal transistor, i.e. the structure under the emitter window. As a result, the lateral voltage drop caused by the base current has to be taken into account for calculating $v_{B'E'}$ and $v_{B'C'}$ in (2.1.2-1). This requires an appropriate definition and model for the internal base resistance by which then $v_{B'E'}$ and $v_{B'C'}$

are becoming "averaged" terminal voltages to ensure a correct description of the electrical (terminal) characteristics of the internal transistor.

C. Emitter periphery injection

The carrier injection at the emitter periphery junction and the corresponding transfer current component through the external base can be taken into account by defining an effective electrical emitter width b_E and length l_E [23, 25, 38], which are usually larger than the emitter window dimensions. This results in an effective size for the internal transistor in the 2D and 3D case with the effective emitter area A_E. By multiplication of all area specific 1D model parameters with A_E (rather than A_{E0}) it was shown in [38], that (2.1.2-1) can then be directly applied without any loss of accuracy at low current densities. At high current densities, however, this approach can become less accurate, and another extension is usually required which will be discussed later. $v_{B'E'}$ and $v_{B'C'}$ are now the terminal voltages of the effective internal transistor (cf. Fig. 2.1.1/1), and the components Q_{jEi} and Q_{jCi} in the charge $Q_{p,T}$ are now defined for the effective internal transistor.

Besides lateral scalability of the model, the major advantages of this approach are that (i) a single equation can be used throughout the total operating region and (ii) a single transfer current source element can be used in the EC (Fig. 2.1.1/1) to describe even transistors with strong 2D and 3D effects.

D. Heterojunction bipolar transistors (HBTs)

The generalized ICCR [35] results in the following expression for the *weighted* minority charge

$$\boxed{Q_{f,T} = h_{fE}Q_{fE} + Q_{fB} + h_{fC}Q_{fC,T}} \qquad (2.1.2\text{-}8)$$

with Q_{fE}, Q_{fB} as the actual minority charges in the emitter and base, respectively. $Q_{fC,T}$ is a weigthed collector minority charge that can include a bias dependent weighting function due to lateral current spreading (see later). The weighing factors h_{fE} and h_{fC} as well as h_{jEi} and h_{jCi} in (2.1.2-3) are given by the differences and grading of the bandgap between the various transistor regions in a HBT. Note, that $Q_{f,T}$ is generally not equal to the stored minority charge Q_f used during dynamic operation.

Assuming a linearly graded bandgap in the base, the model parameter h_{jci} can be expressed analytically as a function of the grading coefficient a_G [47]

$$h_{jCi} \approx \exp\left(-\frac{a_G w_{B0}}{V_T}\right) \tag{2.1.2-9}$$

with w_{B0} as the neutral base width in equilibrium. The corresponding factor for the BE charge, h_{jEi}, can be set to 1 for present Si-based processes and is therefore omitted in the following text for the time being.

The weighting factors [35]

$$h_{fE} = \frac{\overline{\mu_{nB} n_{iB}^2}}{\overline{\mu_{nE} n_{iE}^2}} \qquad \text{and} \qquad h_{fC} = \frac{\overline{\mu_{nB} n_{iB}^2}}{\overline{\mu_{nC} n_{iC}^2}} \tag{2.1.2-10}$$

are model parameters that take into account the different values for effective intrinsic carrier concentration n_i and mobility μ_n of the neutral transistor regions. h_{jCi}, h_{fE}, and h_{fC} are considered to be model parameters in order to make the model applicable also in cases where the doping and physical values are unknown.

For SiGe heterojunction transistors, h_{fC} can be significantly larger than 1 while h_{jCi} is less than 1 explaining the larger Early voltages measured in those transistors. In contrast, for most homojunction transistors these parameters assume values close to 1 although they are becoming more relevant, too, in advanced homojunction transistors due to high-doping effects.

For HBTs, such as those fabricated in III-V semiconductors, that contain a significant energy difference in the conduction band, transport effects such as thermionic emission and tunneling may have to be accounted for. There are various ways of doing this which differ in complexity and, therefore, convergence rate and simulation time. For the present model, the most simple approach has been adopted by introducing a non-ideality coefficient m_{Cf} in the forward component of the transfer current:

$$i_{Tf} = \frac{c_{10}}{Q_{p,T}} \exp\left(\frac{v_{B'E'}}{m_{Cf} V_T}\right) . \tag{2.1.2-11}$$

This approach is believed to offer sufficient flexibility for practical purposes, while keeping down additional computational burden.

E. High current densities

Earlier investigations of a variety of doping profiles have shown that (2.1.2-1) becomes less accurate at high collector current densities due to current spreading in the (epitaxial) collector [31,25]. This 2D/3D effect can also be taken into account as a physics-based expression by using the GICCR and by applying the same methodology as described in [38].

The previously described version of HICUM [31] contains a simplified modelling of this effect by replacing the constant c_{10} with the empirical function $c_1 = c_{10}(1 + i_T/I_{Ch})$ in which I_{Ch} is a model parameter that is (roughly) proportional to the emitter area. In the presently implemented version, the simplified description is still maintained, but a numerically more stable expression is being used:

$$\boxed{c_1 = c_{10}\left(1 + \frac{i_{Tf1}}{I_{Ch}}\right)} \; . \tag{2.1.2-12}$$

with the 1D forward transfer current

$$\boxed{i_{Tf1} = \frac{c_{10}}{Q_{p,\,T}} \exp\left(\frac{v_{B'E'}}{m_{Cf} V_T}\right)} . \tag{2.1.2-13}$$

For $Q_{r,T}$ the actual charge Q_r is being used.

F. Final transfer current model formulation

The "forward" component defined in (2.1.2-6) is repeated here with the modifications in (2.1.2-11) and (2.1.2-12):

$$i_{Tf} = \frac{c_1}{Q_{p,\,T}} \exp\left(\frac{v_{B'E'}}{m_{Cf} V_T}\right) . \tag{2.1.2-14}$$

The "reverse" (better: inverse) component remains identical to (2.1.2-7); in the latter, the influence of collector current spreading at forward operation is not included, i.e. c_1=c_{10}. (2.1.2-14) can be rearranged to give an *explicit* expression for the forward transfer current,

$$\boxed{i_{Tf} = i_{Tf1}\left(1 + \frac{i_{Tf1}}{I_{Ch}}\right)}. \qquad (2.1.2\text{-}15)$$

The total transfer current is then

$$\boxed{i_T = i_{Tf} - i_{Tr}}. \qquad (2.1.2\text{-}16)$$

At high reverse bias across either junction, the respective space-charge region can extend throughout the whole base region (base punch-through effect). As a result, $Q_{p,T}$ would become zero or even less than zero which would cause numerical problems. This situation is most likely to occur at low current densities, where the (always positive) minority charge is negligible. Therefore, in HICUM the hole charge at low current densities,

$$\boxed{Q_{p,1} = Q_{p0} + Q_{jEi} + h_{jCi}Q_{jCi}}, \qquad (2.1.2\text{-}17)$$

is limited to a positive value $Q_{B,rt} = 0.05Q_{p0}$, using a smoothing function, and is replaced by

$$\boxed{Q_{p,low} = Q_{B,rt}\left(1 + \ln\left[1 + \exp\left(\frac{Q_{p,1}}{Q_{B,rt}} - 1\right)\right]\right)}. \qquad (2.1.2\text{-}18)$$

For the usual operating range with $Q_{p,1}/Q_{p0} > 1$, the difference $Q_{p,low}$-$Q_{p,1}$ is much smaller than $10^{-6}Q_{p0}$, so that the smoothing and the associated computational effort can then be skipped in the code.

In general, the GICCR is a non-linear implicit equation for either i_T or $Q_{p,T}$, respectively. Since $Q_{p,T}$ is the common variable in both current components i_{Tf} and i_{Tr}, the GICCR is solved in HICUM for $Q_{p,T}$ by employing Newton-Raphson iteration*. However, as long as $Q_{f,T}$ and Q_r are linearly varying functions of the respective current, i.e. the transit times are current *independent*, the GICCR reduces to a quadratic equation, with an explicit solution for $Q_{p,T}$ (assuming $c_1 = c_{10}$ at low current densities)

*.In the SGPM, the solution is obtained by significant simplifications of the minority charge terms, leading to an (explicit) quadratic equation. Such an approach is physically consistent only at low current densities.

$$Q_{p,\,T} = \frac{Q_{p,\,low}}{2} + \sqrt{\left(\frac{Q_{p,\,low}}{2}\right)^2 + \tau_{f0} c_{10} \exp\left(\frac{v_{B'E'}}{V_T}\right) + \tau_r c_{10} \exp\left(\frac{v_{B'C'}}{V_T}\right)} \qquad (2.1.2\text{-}19)$$

with $Q_{p,low}$ from (2.1.2-18). Inserting the above solution into i_{Tf} and i_{Tr} and adding the minority charge terms provides quite a useful *initial guess* for the Newton iteration at higher current densities:

$$Q_{p,T,initial} = Q_{p,low} + \tau_{f0}\, i_{Tf} + \tau_r\, i_{Tr} \ . \qquad (2.1.2\text{-}20)$$

2.1.3 Minority charge, transit times, and diffusion capacitances

The minority charge is divided into a "forward" and a "reverse" (or inverse) component. The forward component, Q_f, is considered to be dependent on the forward transfer current, i_{Tf}, while the reverse component, Q_r, is considered to be dependent on the reverse transfer current, i_{Tr}. The large-signal charge components can be determined by integrating the respective small-signal transit times, defined as

$$\tau = \frac{dQ}{dI} \tag{2.1.3-1}$$

rather than $\tau = Q/I$.

2.1.3.1 Minority charge component controlled by the forward transfer current

The operating point dependent minority charge stored in a forward biased (vertical) transistor can be determined from the transit time τ_f by simple integration,

$$Q_f = \int_0^{i_{Tf}} \tau_f \, di \quad . \tag{2.1.3-2}$$

τ_f can be extracted from the measured transit frequency vs. d.c. collector current I_C (=I_T) at forward operation for different voltages v_{CE} or v_{BC} as a parameter (cf. [22] and chapter 4). The current and voltage dependent transit time is modelled in HICUM by two components,

$$\boxed{\tau_f(v_{C'E'}, i_{Tf}) = \tau_f(v_{B'C'}) + \Delta\tau_f(v_{C'E'}, i_{Tf})}\,, \tag{2.1.3-3}$$

where τ_{f0} is the low-current transit time, and $\Delta\tau_f$ represents the increase of the transit time at high collector current densities. Fig. 2.1.3/1 shows the typically observed behavior of τ_f and its various components, for which physics-based equations will be given later in this chapter. It is important to note, that the sum of all physically (from carrier densities) calculated storage times, $\tau_{m\Sigma}$, equals the transit time τ_f, that is extracted from small-signal results using the measurement method.

The minority charge model in HICUM uses an “effective” collector voltage

$$v_{ceff} = V_T\left[\ln\left(1 + \exp\left(\frac{v_c - V_T}{V_T}\right)\right) + 1\right] \tag{2.1.3-4}$$

with

$$v_c = v_{C'E'} - V_{C'E's} \approx V_{DCi} - v_{B'C'} \ . \tag{2.1.3-5}$$

The internal CE saturation voltage $V_{C'E's}$ ($\approx V_{DEi}$-V_{DCi}) is a model parameter. The smoothing function for v_{ceff} has been implemented in order to provide a smooth behavior of the critical current (see later) and the forward minority charge for very small and negative values of v_c.

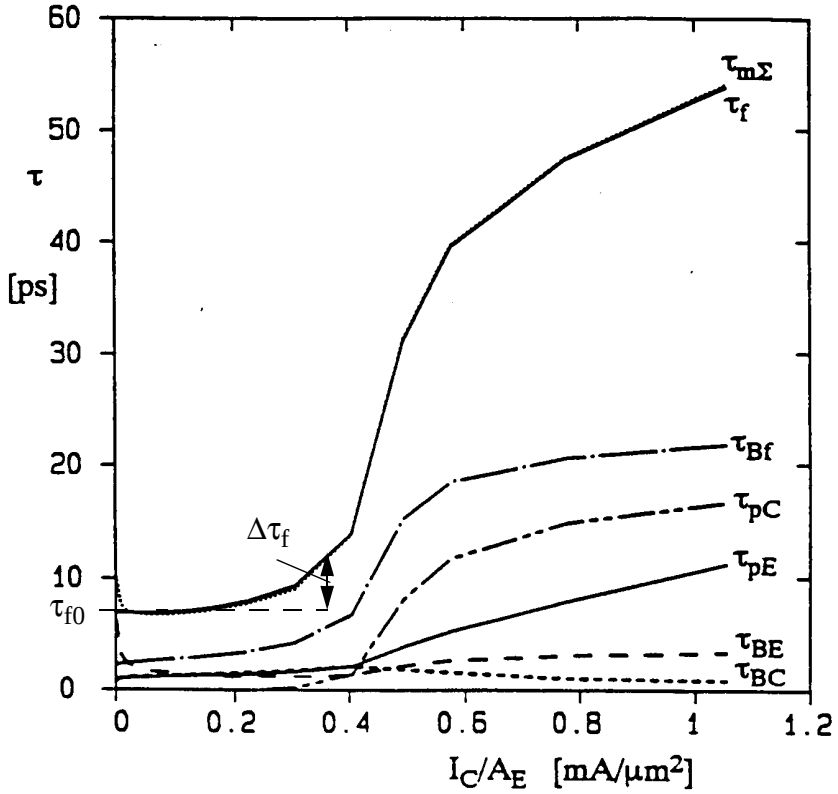


Fig. 2.1.3/1: Charge storage and transit time components vs. collector current density. The components τ_{Bf}, τ_{pC}, τ_{pE}, τ_{BE}, τ_{BC}, and $\tau_{m\Sigma}$ were calculated from 1D device simulation, while τ_B was extracted from small-signal simulations and f_T using the measurement method.

As Fig. 2.1.3/2 shows, v_{ceff} is equal to v_c for values larger than about $2V_{C'E's}$ and approaches the the thermal voltage V_T as the limit for negative values.

The transit time and minority charge model used in HICUM and its derivation are discussed in detail in [41]. In this text, the most important equations and their physical meaning are summarized.

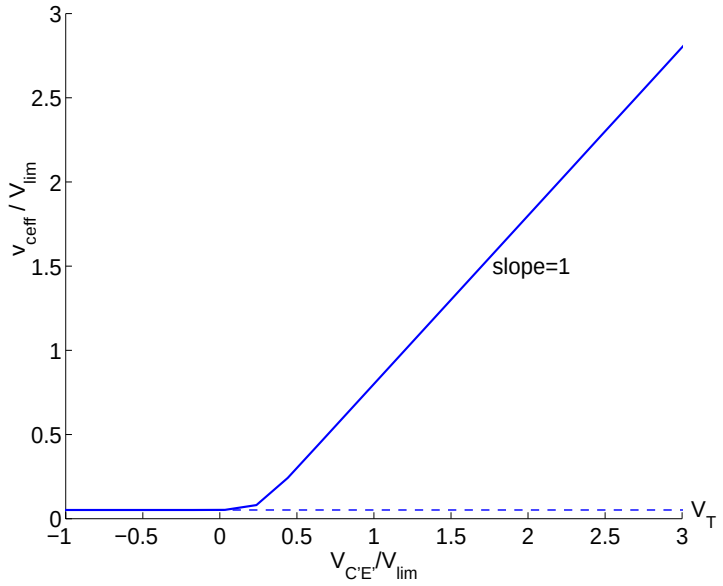


Fig. 2.1.3/2: Normalized effective collector voltage vs. normalized (internal) collector voltage showing the behaviour of the smoothing function.

A. Low-current densities

The low-current component τ_{f0} depends on the collector-base (or collector-emitter voltage) only,

$$\tau_{f0}(v_{B'C'}) = \tau_0 + \Delta\tau_{0h}(c-1) + \tau_{Bfvl}\left(\frac{1}{c}-1\right) \qquad (2.1.3\text{-}6)$$

with the (reciprocal) normalized internal BC depletion capacitance $c = C_{jCi0}/C_{jCi}(V_{B'C'})$. The first time constant, τ_0, represents the sum of voltage independent components of various transistor regions at $V_{B'C'} = 0$; this condition already defines how to extract its value. The second term represents the net voltage dependent change caused by the Early-effect and the transit time through the BC space charge region: for $\Delta\tau_{0h}<0$ the Early effect dominates while for $\Delta\tau_{0h}>0$ the transit time increase caused by the widening of the BC space charge region at large voltages dominates. The third term takes into account the finite carrier velocity in the BC space charge region resulting in a carrier jam at low voltages $V_{C'E'}$.

Fig. 2.1.3/3 shows two examples for the voltage dependence of the low-current transit time and its two voltage dependent components. The axis values have been normalized to the model parameters τ_0 and V_{DCi}, respectively. The upper figure (a) contains a behavior that is (more) typical for a relatively slow high-voltage transistor, which is characterized by a relatively wide and low-doped collector region under the emitter. In this case, τ_{f0} increases with increasing $V_{C'E'}$ ($=V_{B'E'}-V_{B'C'}$) due to the widening of the BC space charge region. Toward very low $V_{C'E'}$ the drift velocity within the BC space charge region decreases, and the respective (third) term in (2.1.3-6) dominates the voltage dependence, which leads again to an increase of τ_{f0} and to a minimum around $V_{B'C'}=0$.

The lower figure (b) shows the typical behaviour for a high-speed transistor with, e.g., a selectively implanted collector and a thin base. With increasing reverse bias, the BC space charge region does extend noticeably also into the base, resulting in a (slightly) negative value of $\Delta\tau_{0h}$ and a decrease of the respective component. Therefore, τ_{f0} decreases with increasing $V_{C'E'}$.

The respective low-current forward minority charge is simply given by

$$\boxed{Q_{f0} = \tau_{f0}\, i_{Tf}} \quad . \tag{2.1.3-7}$$

(a)

(b)

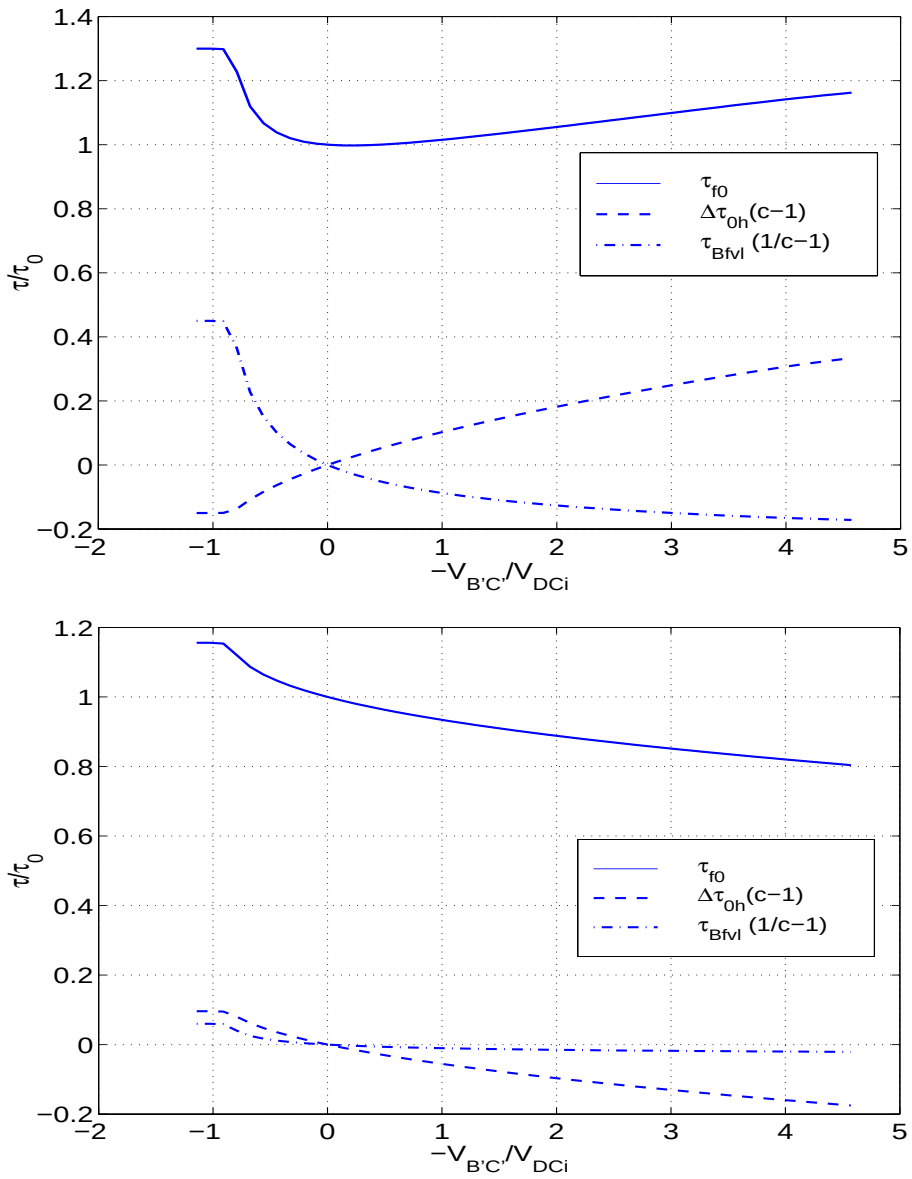


Fig. 2.1.3/3: Normalized low-current transit time and its components as a function of normalized (internal) BC voltage: (a) for a “high-voltage” transistor (τ_0=10ps, $\Delta\tau_{0h}$=2.5ps, τ_{Bfvl}=3ps), (b) for a “high-speed” transistor (τ_0=2.5ps, $\Delta\tau_{0h}$=-0.4ps, τ_{Bfvl}=0.1ps).

B. Medium and high current densities

At medium current densities, the electric field at the BC junction starts to decrease, and the BC junction region becomes quasi-neutral at high current densities. This is often called Kirk-effect [12]. In HICUM, the onset of high-current effects is characterized by the critical current [32]

$$I_{CK} = \frac{v_{ceff}}{r_{Ci0}} \frac{1}{\sqrt{1+\left(\frac{v_{ceff}}{V_{lim}}\right)^2}} \left[1 + \frac{x + \sqrt{x^2 + 10^{-3}}}{2}\right] \tag{2.1.3-8}$$

with $x = (v_{ceff}-V_{lim})/V_{PT}$ in the smoothing function that connects the cases of low and high electric fields in the collector. The other (model) parameters are the internal collector resistance at low electric fields,

$$r_{Ci0} = \frac{w_C}{q\mu_{nC0}N_{Ci}A_E} \frac{1}{f_{cs}} \quad , \tag{2.1.3-9}$$

the voltage defining the boundary between low and high electric fields in the collector,

$$V_{lim} = \frac{v_{sn}}{\mu_{nC0}} w_C \quad , \tag{2.1.3-10}$$

and the (collector) punch-through voltage

$$V_{PT} = \frac{qN_{Ci}}{2\varepsilon} w_C^2 \quad . \tag{2.1.3-11}$$

As the above relations show, I_{CK} depends on the electron saturation drift velocity, v_{sn}, and the electron low-field mobility, μ_{nC0}, as well as on width w_C and (average) doping N_{Ci} of the internal collector. The current spreading factor f_{cs}, which is discussed in chapter 2.1.17, facilitates lateral scaling [38] and is calculated by TRADICA (or any parameter generation or extraction program). Despite their physical relationship r_{Ci0}, V_{lim} and V_{PT} are considered to be model parameters in order to offer a more flexible parameter extraction and broader application of the model. However, their physics-based relationship is very useful for temperature and statistical modelling.

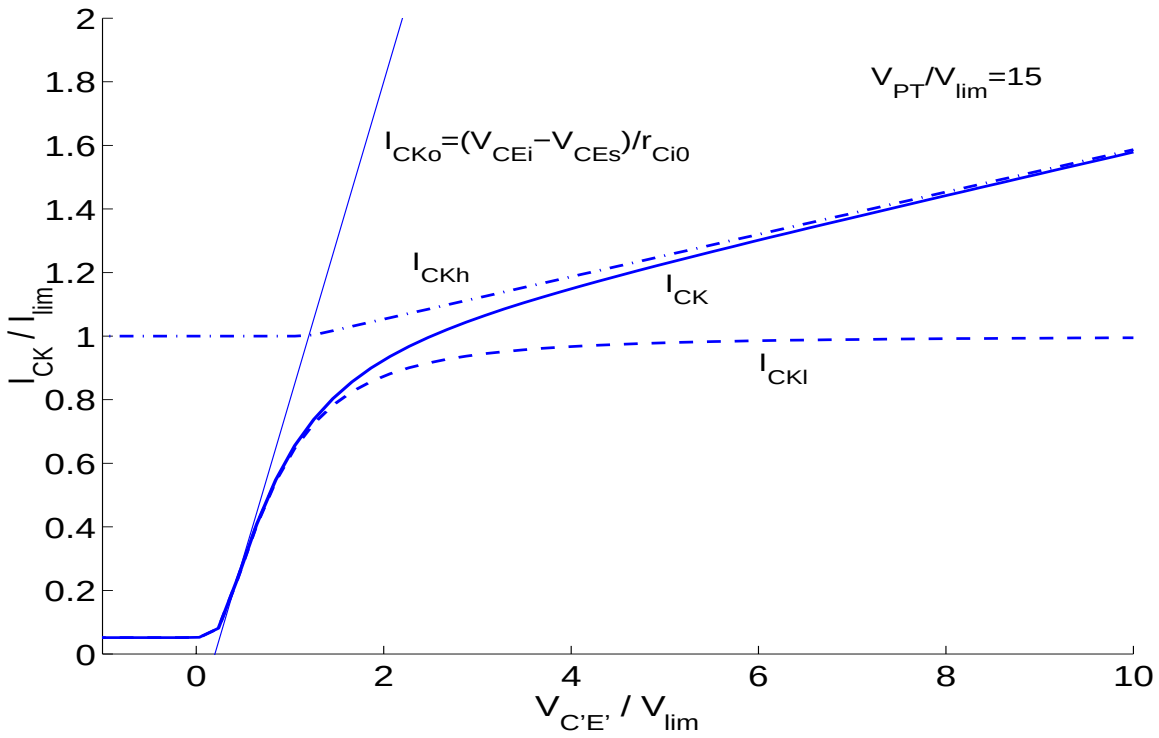


Fig. 2.1.3/4: Normalized critical current I_{CK} vs. normalized internal CE voltage and related single components: $I_{CKl} = (v_{ceff}/r_{Ci0})/\sqrt{1+(v_{ceff}/V_{lim})^2}$ from low-voltage theory; $I_{CKh} = I_{lim}\,[1+(v_{ceff}-V_{lim})/V_{PT}]$ from high-voltage theory with $I_{lim}=V_{lim}/r_{Ci0}$.

The consequence of the changing electric field in the BC junction at medium current densities is, first of all, an increase in the neutral base width and, therefore, in the base component of the transit time; second, also the transit time through the BC space charge region may increase, depending on how large the electric field is. Third, the corresponding decrease of the small-signal current gain leads to an increase of the emitter component. Since the current independent part of this component has already been taken into account in τ_{f0} only the change (increase) has to be modelled,

$$\Delta\tau_{Ef} = \tau_{Ef0}\left(\frac{i_{Tf}}{I_{CK}}\right)^{g_{\tau E}} \qquad (2.1.3\text{-}12)$$

with the model parameters $g_{\tau E}$ and the storage time

$$\tau_{Ef0} = \frac{\tau_{pE0}}{\beta_0} \approx \frac{1}{\beta_0}\left(\frac{w_E}{v_{Ke}} + \frac{w_E^2}{2\mu_{pE}V_T}\right) \tag{2.1.3-13}$$

which depends on the low-frequency common-emitter small-signal current gain β_0 and the hole transit time τ_{pE0} in which w_E, μ_{pE}, and v_{Ke} are the width, hole mobility and the effective hole contact recombination velocity of the neutral emitter, respectively. The corresponding charge stored in the neutral emitter is:

$$\boxed{\Delta Q_{Ef} = \Delta\tau_{Ef}\frac{i_{Tf}}{1+g_{\tau E}}} \; . \tag{2.1.3-14}$$

In the neutral collector, minority (hole) charge storage starts only at high current densities [31, 32]. Theferore, the charge difference to its negligible low-current contribution is equal to the total hole charge Q_{pC} in the collector:

$$\boxed{\Delta Q_{Cf} = Q_{Cf} = Q_{pC} = \tau_{pCs} i_{Tf} w^2} \tag{2.1.3-15}$$

with the saturation storage time of the neutral collector,

$$\tau_{pCs} = \frac{w_C^2}{4\mu_{nC0}V_T} \; . \tag{2.1.3-16}$$

The normalized injection width,

$$\boxed{w = \frac{w_i}{w_C} = \frac{i + \sqrt{i^2 + a_{hc}}}{1 + \sqrt{1 + a_{hc}}}} \tag{2.1.3-17}$$

is bias dependent via the variable

$$\boxed{i = 1 - \frac{I_{CK}}{i_{Tf}}} \tag{2.1.3-18}$$

while a_{hc} is considered to be a model parameter. By using a smoothing function for w rather than the original expression i in (2.1.3-17), the collector charge is made continuously differentiable over the whole bias region. The corresponding collector storage time is given by

$$\Delta\tau_{Cf} = \tau_{Cf} = \tau_{pC} = \frac{dQ_{pC}}{dI_{Tf}} = \tau_{pCs}\, w^2 \left[1 + \frac{2}{\frac{i_{Tf}}{I_{CK}} \sqrt{i^2 + a_{hc}}} \right] \tag{2.1.3-19}$$

Device simulations for many different processes have shown that the shape of the current dependence of the neutral base component τ_{Bf}, is very similar to that of the collector portion τ_{pC} due to the coupling of these regions by the carrier density at the BC junction. As a consequence, the bias dependent increase of the base charge at high-current densities is similarly expressed as

$$\boxed{\Delta Q_{Bf} = \tau_{Bfvs} i_{Tf}\, w^2} \tag{2.1.3-20}$$

with the saturation storage time reached at high current densities,

$$\tau_{Bfvs} = \frac{w_{Bm} w_C}{2 G_{\zeta i} \mu_{nC0} V_T} \quad . \tag{2.1.3-21}$$

w_{Bm} is the metallurgical base width, and $G_{\zeta i}$ (≥1) is a factor that depends on the drift field in the neutral base [41]. The corresponding additonal base transit time reads

$$\Delta\tau_{Bf} = \frac{d\Delta Q_{Bf}}{dI_{Tf}} = \tau_{Bfvs}\, w^2 \left[1 + \frac{2}{\frac{i_{Tf}}{I_{CK}} \sqrt{i^2 + a_{hc}}} \right] . \tag{2.1.3-22}$$

In HICUM, the total storage time constant,

$$\tau_{hcs} = \tau_{pCs} + \tau_{Bfvs} = \frac{w_C^2}{4 \mu_{nC0} V_T} + \frac{w_{Bm} w_C}{2 G_{\zeta i} \mu_{nC0} V_T} \quad , \tag{2.1.3-23}$$

is used as a model parameter to make the model application more flexible and easy to use. As discussed in chapter 2.1.17, the accurate and physics-based description of collector current spreading and associated lateral scaling at high current densities require a partitioning between base and collector component. For this, the partitioning constant

$$f_{\tau hc} = \frac{\tau_{pCs}}{\tau_{hcs}} = \frac{w_C}{w_C + 2w_{Bm}} \tag{2.1.3-24}$$

is introduced as model parameter. A value of $f_{\tau hc}$ between 0 and 1 allows a gradual partitioning, with the 1D expressions given above (i.e. no collector current spreading) being employed for $f_{\tau hc} = 0$, while a dominating influence of the colector term (including current spreading) can be taken into account by $f_{\tau hc} \rightarrow 1$.

Fig. 2.1.3/5 shows a sketch of the current dependence of the *additional* transit time $\Delta\tau_f$ and its various components, calculated with the equations given above and using model parameters that are typical for a high-speed process.

In the 1D case, the collector and base component can be lumped together ($f_{\tau hc} = 0$), leading to the expression for the additionally stored minority charge in the base and collector region at high current densities,

$$\boxed{\Delta Q_{fh} = \Delta Q_{Bf} + Q_{Cf} = \tau_{hcs} i_{Tf} w^2} \ . \tag{2.1.3-25}$$

The corresponding increase of the transit time at high-current densities is then given by

$$\boxed{\Delta\tau_{fh} = \Delta\tau_{Bf} + \tau_{Cf} = \tau_{hcs} w^2 \left[1 + \frac{2}{\frac{i_{Tf}}{I_{CK}}\sqrt{i^2 + a_{hc}}}\right]} \ . \tag{2.1.3-26}$$

The 1D case is detected by the model if the model parameters LATB and LATL (cf. chapter 2.1.17) are zero.

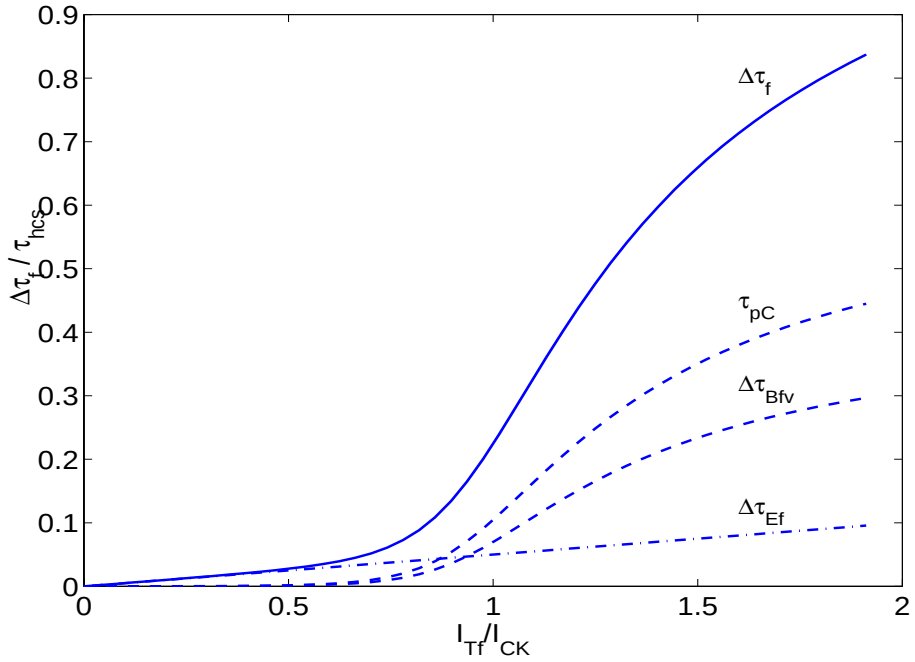


Fig. 2.1.3/5: Sketch of normalized transit time $\Delta\tau_f$ vs. normalized forward collector current I_{Tf}, including the various components: collector component τ_{pC}, additional base component $\Delta\tau_{Bf}$, and additional emitter contribution $\Delta\tau_{Ef}$.

The total minority charge in the various operating regions, that is used for transient or high-frequency analysis, is then calculated according to (2.1.3-1) and consists of the following contributions:

$$Q_f = Q_{f0} + \Delta Q_{Ef} + \Delta Q_{fh} \tag{2.1.3-27}$$

while the total forward transit time (or storage time) is given by

$$\tau_f = \tau_{f0} + \Delta\tau_{Ef} + \Delta\tau_{fh} \ . \tag{2.1.3-28}$$

If the lateral scaling capability is used, ΔQ_{fh} and $\Delta\tau_{fh}$ are composed of their separately calculated base and collector contribution (cf. chapter 2.1.17). The above equations contain physical and process parameters that facilitate predictions of the electrical characteristics as a function of process variations.

2.1.3.2 Minority charge component controlled by the inverse transfer current

For forward transistor operation in high-speed applications the portion of the minority charge which is exclusively controlled by the base-collector voltage is often negligible or only a small fraction of the total minority charge. Therefore, including this charge in Q_f causes only negligible error in transient operation of transistors in high-speed circuits. For small-signal high-frequency operation in the high-current region, which is a very unusual case, the base-collector voltage controlled charge may be taken into account by including its diffusion capacitance in the total internal base collector capacitance [13].

Alternatively, the BC diffusion charge can be modelled by the simple relation

$$Q_r = \tau_r \, i_{Tr} \tag{2.1.3-29}$$

with the inverse transit time τ_r as a model parameter.

2.1.4 Depletion charges and capacitances

Modelling of depletion charges (Q_j) and capacitances (C_j) as a function of the voltage v across the respective junction is partially based on classical theory that gives within a certain operating range

$$Q_j = \int_0^v C_j dv' = \frac{C_{j0} V_D}{1-z}\left[1-\left(1-\frac{v}{V_D}\right)^{(1-z)}\right] \qquad (2.1.4\text{-}1)$$

and

$$C_j = \frac{C_{j0}}{\left(1-\frac{v}{V_D}\right)^z} \quad . \qquad (2.1.4\text{-}2)$$

The zero bias capacitance C_{j0}, the diffusion (or built-in) voltage V_D as well as the exponent coefficient z are model parameters. Due to the pole at forward bias, i.e. $v=V_D$, however, the above formula is not yet suited for a compact model from both a numerical and physics-based point of view. The respective modification will be described for the BE depletion capacitance.

At high reverse voltages the epitaxial collector can become fully depleted up to the buried layer. This punch- (or reach-)through effect is also not included in the classical equation above (and in the SGPM). The corresponding extension will be discussed for the BC depletion capacitance

2.1.4.1 Base-emitter junction

Fig. 2.1.4/1 shows the voltage dependence of a BE depletion capacitance at forward bias. The symbols were obtained from 1D device simulation, with depletion and minority charge defined as in [36]. The depletion capacitance follows quite well the classical equation up to a certain voltage, which is close to the turn-on voltage of a transistor used for switching applications. In contrast to the classical equation, the capacitances then reaches a maximum within the “practical” operation range of a transistor. Towards very high forward bias, the capacitance even decreases to zero, since the total depletion charge has to be limited from a physical point of view.

The modified equation employed in HICUM is described below for the example of the internal BE depletion capacitance with the (classical) model parameters C_{jEi0}, V_{DEi}, z_{Ei}, and the additional

model parameter a_{jEi}. The latter is defined in Fig. 2.1.4/1 as the ratio of the maximum value to the zero-bias value and can directly be extracted from f_T measurements at low current densities (e.g. [2, 14]). As a consequence, C_{jEi} is kept at its maximum value in HICUM to maintain consistency between measurement and model. Keeping C_{jEi} constant is also justified, because at high forward bias, i.e. beyond the maximum, the diffusion capacitance becomes orders of magnitude larger than C_{jEi}. The reverse bias region of the BE depletion capacitance and charge is described by the classical equations.

For modeling the peripheral BE depletion capacitance, the corresponding model parameters C_{jEp0}, V_{DEp}, z_{Ep}, a_{jEp} as well as the voltage and $v_{B*E'}$ have to be inserted.

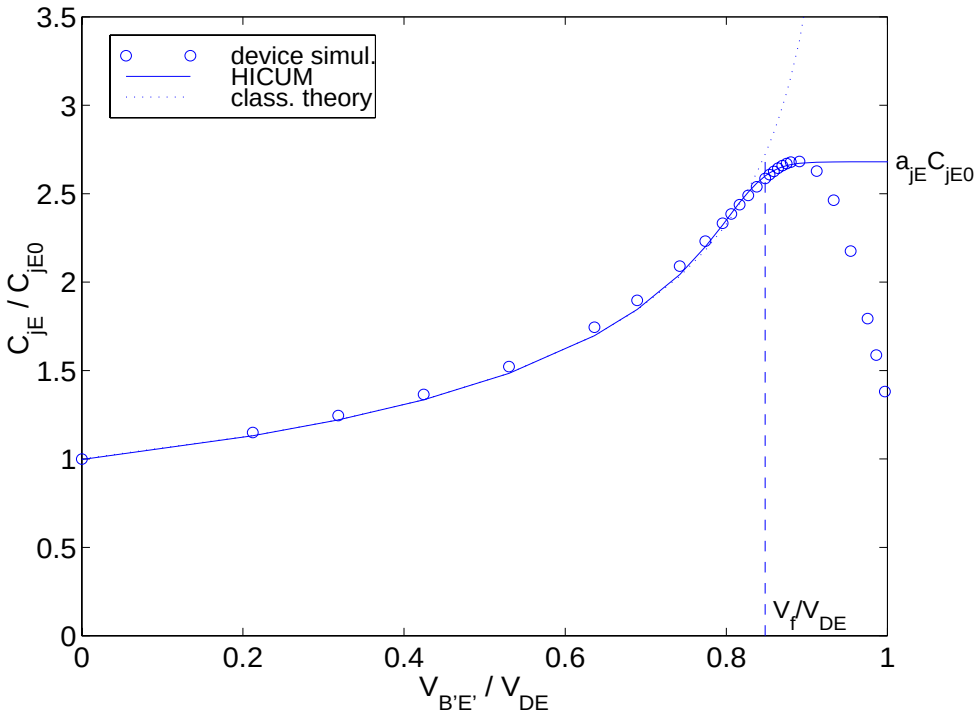


Fig. 2.1.4/1: Typical dependence of BE depletion capacitance on junction voltage at forward bias: comparison between 1D device simulation, HICUM, classical theory. In addition, characteristic variables used in the model equations have been inserted.

The forward bias depletion capacitance model consists of a classical portion and a component for medium and large forward bias (cf. Fig. 2.1.4/1):

$$C_{jEi} = \frac{C_{jEi0}}{(1 - v_j / V_{DEi})^{z_{Ei}}} \cdot \frac{e}{1+e} + a_{jEi} C_{jEi0} \frac{1}{1+e} \tag{2.1.4-3}$$

with

$$e = \exp\left(\frac{V_f - v_{B'E'}}{V_T}\right) \tag{2.1.4-4}$$

and the smoothing function for the auxiliary voltage

$$v_j = V_f - V_T \ln[1+e] < V_f \quad . \tag{2.1.4-5}$$

V_f is the voltage at which at large forward bias the capacitance of the classical expression intercepts the maximum constant value (cf. Fig. 2.1.4/1):

$$V_f = V_{DEi}[1 - a_{jEi}^{-(1/z_{Ei})}] \quad . \tag{2.1.4-6}$$

The corresponding charge equation reads

$$Q_{jEi} = \frac{C_{jEi0} V_{DEi}}{1 - z_{Ei}} \left[1 - \left(1 - \frac{v_j}{V_{DEi}}\right)^{(1-z_{Ei})}\right] + a_{jEi} C_{jEi0} (v_{B'E'} - v_j), \tag{2.1.4-7}$$

and Q_{jEp} is calculated similarly.

2.1.4.2 Internal base-collector junction

The BC junction is usually operated at reverse bias. If the internal voltage $-v_{B'C'}$ exceeds the effective punch-through voltage (see later), the epitaxial collector region becomes fully depleted. For an ideal step-like transition from the epitaxial collector to the buried-layer the corresponding capacitance would remain constant (like a plate capacitance). However, in reality the doping concentration increases with only a finite slope towards the maximum buried layer concentration. As a consequence, C_{jCi} still decreases even beyond punch-through, but with a weaker voltage dependence.

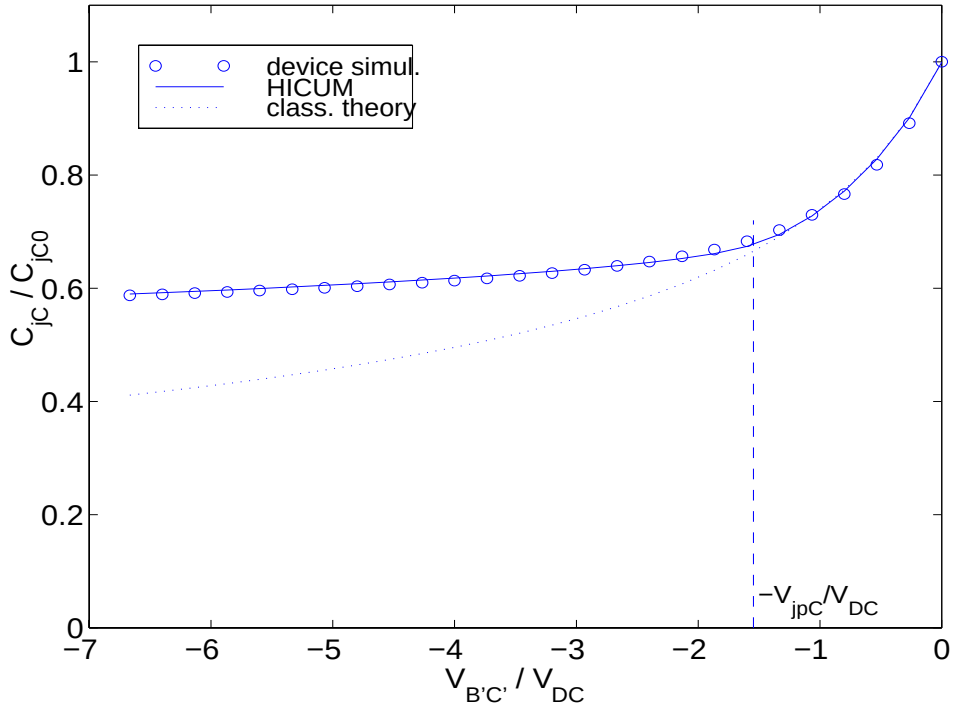


Fig. 2.1.4/2: Typical dependence of a BC depletion capacitance on junction voltage at reverse bias: comparison between 1D device simulation (symbols), HICUM (solid line), classical theory (dashed line). In addition, characteristic variables used in the model equations have been inserted.

Before the capacitance equation is explained in detail, it is helpful to define a number of variables that are needed in the equations. The effective punch-through voltage is given by

$$V_{jPCi} = V_{PTCi} - V_{DCi} = \frac{qN_{Ci}}{2\varepsilon} w_{Ci}^2 - V_{DCi} \quad , \tag{2.1.4-8}$$

which is shown in Fig. 2.1.4/2. For flexibility and accuracy reasons as well as in order to simplify and decouple parameter extraction, V_{PTCi} is considered as separate model parameter rather than using V_{PT} from the I_{CK} formulation. For predictive modeling V_{PTCi}=V_{PT} is certainly a good initial guess.

The voltage defining the boundary between the classical expression and the maximum (constant) value at large forward bias was already defined for the BE junction capacitance (cf. Fig. 2.1.4/1); in terms of the respective BC model parameters it reads here

$$\boxed{V_{fCi} = V_{DCi}[1 - a_{jCi}^{-(1/z_{Ci})}]} \quad . \tag{2.1.4-9}$$

The voltage at which the transition from medium to large reverse bias (slowly) starts, is defined as

$$\boxed{V_r = 0.1V_{jPCi} + 4V_T} \quad . \tag{2.1.4-10}$$

In the following, “large reverse” bias is defined as $V_{BCi} \leq -V_{jPCi}$, “medium” bias is defined as $V_{jPCi} < V_{BCi} < V_{fCi}$, and “large forward” bias is defined as $V_{BCi} \geq V_{fCi}$.

The depletion capacitance consists of three components,

$$\boxed{C_{jCi} = C_{jCi,cl} + C_{jCi,PT} + C_{jCi,fb}}, \tag{2.1.4-11}$$

which are discussed below in more detail.

$C_{jCi,cl}$ represents the contribution at medium bias,

$$\boxed{C_{jCi,cl} = \frac{C_{jCi0}}{(1 - v_{j,m}/V_{DCi})^{z_{Ci}}} \cdot \frac{e_{j,r}}{1 + e_{j,r}} \frac{e_{j,m}}{1 + e_{j,m}}} \tag{2.1.4-12}$$

which contains the classical equation as the first term. The last two product terms result from smoothing functions for the respective BC junction voltage, that enable a continuously differentiable transition to the two adjacent bias regions. Like for the BE depletion capacitance, the numerical overflow at large forward bias is avoided by replacing $V_{B'C'}$ with the auxiliary (smoothed) voltage

$$\boxed{v_{j,r} = V_{fCi} - V_T \ln[1 + e_{j,r}]} \quad \text{with} \quad \boxed{e_{j,r} = \exp\left(\frac{V_{fCi} - v_{B'C'}}{V_T}\right)} \tag{2.1.4-13}$$

which contains the actual junction voltage. Analogously to C_{jE}, the forward bias value (for $e(v_{j,r}) = 0$) is limited to a maximum,

$$\boxed{C_{jCi,fb} = a_{jCi} C_{jCi0} \frac{1}{1 + e_{j,r}}} \quad , \tag{2.1.4-14}$$

with a_{jCi} as model parameter. The last term is again a continuously differentiable function that enables a smooth transition between large forward and medium bias.

Finally, $C_{jCi,PT}$ represents the large reverse bias region around and beyond punch-through,

$$C_{jCi,PT} = \frac{C_{jCi0,r}}{(1 - v_{j,r}/V_{DCi})^{z_{Ci,r}}} \cdot \frac{1}{1 + e_{j,m}} \quad . \tag{2.1.4-15}$$

Here, the first term contains the classical voltage dependence, but now with different parameters $C_{jCi0,r}$ and $z_{Ci,r}$, which model the weak bias dependence under punch-through conditions and will be discussed later. In this case, the auxiliary voltage is given by the smoothing function

$$v_{j,m} = -V_{jPCi} + V_r \ln[1 + e(v_{j,m})] \quad \text{with} \quad e_{j,m} = \exp\left(\frac{V_{jPCi} + v_{j,r}}{V_r}\right) \tag{2.1.4-16}$$

which now depends on the auxiliary voltage $v_{j,r}$ in order to enable a smooth capacitance and charge behavior over all bias regions. Note, that $v_{j,r}$ equals $v_{B'C'}$ at large reverse bias.

The corresponding depletion charge is then obtained by integration of C_{jCi},

$$Q_{jCi} = \underbrace{Q_{jCi,m}}_{\text{medi-}} + \underbrace{Q_{jCi,r}}_{\text{reverse}} - \underbrace{Q_{jCi,c}}_{\text{correc-}} + \underbrace{a_{jCi} C_{jCi0}(v_{B'C'} - v_{j,r})}_{\text{large forward}} \tag{2.1.4-17}$$

with the component at medium bias,

$$Q_{jCi,m} = \frac{C_{jCi0} V_{DCi}}{1 - z_{Ci}} \left[1 - \left(1 - \frac{v_{j,m}}{V_{DCi}}\right)^{1 - z_{Ci}}\right] , \tag{2.1.4-18}$$

the component at large reverse bias,

$$Q_{jCi,r} = \frac{C_{jCi0,r} V_{DCi}}{1 - z_{Ci,r}} \left[1 - \left(1 - \frac{v_{j,r}}{V_{DCi}}\right)^{1 - z_{Ci,r}}\right] , \tag{2.1.4-19}$$

and a “correction” component,

$$Q_{jCi,c} = \frac{C_{jCi0,r} V_{DCi}}{1 - z_{Ci,r}} \left[1 - \left(1 - \frac{v_{j,m}}{V_{DCi}} \right)^{1 - z_{Ci,r}} \right] , \qquad (2.1.4\text{-}20)$$

that results from the integration process. The parameters $C_{jCi0,r}$ and $z_{Ci,r}$ in the last two components are required to model the weaker voltage dependence under punch-through conditions, compared to the voltage dependence at medium bias. $C_{jCi0,r}$ can be calculated from the punch-through voltage as

$$C_{jCi0,r} = C_{jCi0} \cdot \left(\frac{V_{DCi}}{V_{PTCi}} \right)^{(z_{Ci} - z_{Ci,r})} , \qquad (2.1.4\text{-}21)$$

while $z_{Ci,r}$ is internally set to $z_{Ci}/4$. The latter turned out to be a good compromise for the investigated cases. As consequence, both $C_{jCi0,r}$ and $z_{Ci,r}$ are only internal parameters and do not have to be extracted and externally specified. If required, however, it would be sufficient to make $z_{Ci,r}$ a user model parameter.

At high current densities C_{jCi} becomes also current dependent as discussed, e.g., in [31]. The respective (smooth) expressions for both capacitance and charge require complicated expressions which can increase simulation time significantly. As discussed in [13] for small-signal applications, a pure voltage dependent model for C_{jCi} proved to be sufficient, since transistors in (small-signal) analog circuits are not operated at high current densities. For large-signal transient applications, however, the influence of a current dependent C_{jCi} is negligible, especially at higher current densities. Therefore, the current dependence of C_{jCi} is neglected in the present HICUM version.

2.1.4.3 External base-collector junction

The external base-collector depletion capacitance consists of a bottom and a peripheral part. TRADICA merges these portions, that may have different model parameters, first into a single element (with a single set of model parameters), which is then partitioned into two capacitance elements across the external base resistance r_{Bx} (cf. Fig. 2.1.1/1), according to a first-order high-frequency approximation of the RC transmission line behaviour of the external base. The merging procedure, which is also required for simpler equivalent circuit structures, reduces the number of model parameters to be specified for the circuit simulator.

A possible alternative is to determine the partitioning from measurements of, e.g., high-frequency S-parameters. However, it was found that such a partitioning factor (strongly) depends on the measurement method and conditions used and, therefore, can assume non-physical values.

The partitioning of the total capacitance $C_{BCx} = C_{jCx}(v) + C_{Cox}$ (see also Section 2.1.7) across r_{Bx} requires the additional model parameter f_{BC}, which is dependent on geometry and technology specific parameters and which is calculated by TRADICA. According to f_{BC} the capacitances are split as follows in the present HICUM implementation (cf. Fig. 2.1.1/1):

$$C_{BCx} = C'_{BCx} + C''_{BCx} = (1\text{-}f_{BC})\, C_{BCx} + f_{BC}\, C_{BCx} \ . \qquad (2.1.4\text{-}22)$$

Depending on the values for f_{BC}, C_{Cox} and C_{jCx} as well as according to the nature of the capacitance components different cases have to be distinguished. For instance, if f_{BC} is larger than C_{Cox}/C_{jCx} then part of C_{Cox} has to be connected to node B* (i.e. *behind* r_{Bx}). Since C_{Cox} is closest to the base contact usually the major portion or even the total value has to be connected to the base terminal B. The various cases are taken into account based on the zero-bias depletion capacitance rather than the voltage dependent value in order to reduce arithmetic operation count. The implementation is as follows:

$C'_{BCx0} = (1\text{-}f_{BC})\, C_{BCx0}$

if($C'_{BCx0} \geq C_{Cox}$) then
  $C'_{Cox} = C_{Cox}$
  $C''_{Cox} = 0$
  $C'_{jCx0} = C'_{BCx0} - C_{Cox}$
  $C''_{jCx0} = C_{jCx0} - C'_{jCx0}$
else
  $C'_{Cox} = C'_{BCx0}$
  $C''_{Cox} = C_{Cox} - C'_{Cox}$
  $C'_{jCx0} = 0$
  $C''_{jCx0} = C_{jCx0}$
endif

Since the depletion charge of the external BC junction does not depend on the transfer current, the purely voltage dependent expressions given for C_{jCi} and Q_{jCi} can be employed for C_{jCx} and Q_{jCx} by simply inserting the model parameters C_{jCx0}, V_{DCx}, z_{Cx}, and V_{PTCx}. The punch-through voltage (and capacitance) of the external collector region is usually different from that of the inter-

nal region due to their different epi widths and - in case of a selectively implanted collector - the different doping concentrations in the internal and external region.

2.1.4.4 Collector-substrate junction

The CS depletion charge and capacitance are modelled by the same type of formula as employed for the bottom part of the external BC charge and capacitance. The corresponding model parameters are C_{jS0}, V_{jS}, z_S, and V_{PTS}. Taking into account the punch-through effect may be necessary for technologies containing a semi-insulating substrate (layer). For most technologies, however, there is no punch-through effect at the CS junction, and V_{PTS} can be set to "infinity".

Since the CS junction is modelled by a single element, C_{jS} contains - from a physical point of view - both the bottom and peripheral portion of that junction; i.e., the model parameters result from merging the corresponding voltage dependent portions [42] (see also Fig. 2.1.17/4).

For certain applications and processes, an additional substrate coupling network in series to C_{jS} as well as a substrate transistor may be necessary. These extensions are discussed later.

2.1.5 Static base current components

The base current flowing into the emitter can be separated into a bottom and peripheral component. The bottom portion models the current injected across the (*effective*) emitter area, and the peripheral component models the current injected across the peripheral BE junction. Each of these components contains the current contributions caused by volume (SRH and Auger) recombination, by surface recombination, by tunneling, and by an (effective) interface recombination velocity at the emitter "contact". The physical modelling of all these effects including the modulation of the neutral emitter width in advanced and heterojunction bipolar transistors would require a complicated and computationally time expensive description as well as a significantly increased effort in parameter determination. From a practical application point of view, however, a simpler approach does exist that is sufficiently accurate.

The following equations describe the d.c. and quasi-static component of the base current, which are applicable also at high frequencies. Note, that at high switching speeds or frequencies, the dynamic (capacitive) component of the base current becomes much larger than the d.c./quasi-static component, so that its correct modeling is of higher importance for those applications.

The quasi-static internal base current, which represents injection across the bottom emitter area, is modelled in HICUM as

$$\boxed{i_{jBEi} = I_{BEiS}\left[\exp\left(\frac{v_{B'E'}}{m_{BEi}V_T}\right)-1\right] + I_{REiS}\left[\exp\left(\frac{v_{B'E'}}{m_{REi}V_T}\right)-1\right]} \qquad (2.1.5\text{-}1)$$

The saturation currents I_{BEiS} and I_{REiS} as well as the non-ideality coefficients m_{BEi} and m_{REi} are model parameters. The first component in the above formula represents the current injected into the neutral emitter; a corresponding $m_{BEi}>1$ represents effects such as Auger recombination and the (very small) modulation of the width of the neutral emitter region. The second component represents the loss in the space charge region due to volume and surface recombination; the value of m_{REi} is usually in the range of 1.5 to 2 so that this component only plays a role at low injection. It is used to model the decrease of the current gain at low current densities.

Analogously, the quasi-static base current injected across the emitter periphery is given by

$$i_{jBEp} = I_{BEpS}\left[\exp\left(\frac{v_{B^*E'}}{m_{BEp}V_T}\right)-1\right] + I_{REpS}\left[\exp\left(\frac{v_{B^*E'}}{m_{REp}V_T}\right)-1\right] . \qquad (2.1.5\text{-}2)$$

The saturation currents I_{BEpS} and I_{REpS} as well as the non-ideality factors m_{BEp} and m_{REp} are model parameters.

Since the recombination at low forward bias is more pronounced at the emitter periphery compared to the bottom, its contribution (I_{REiS} ...) to the internal base current component may often be omitted in order to simplify the model and the parameter determination.

In hard-saturation or for inverse operation the current contributions across the base-collector junction become significant. The component of the internal BC junction is

$$i_{jBCi} = I_{BCiS}\left[\exp\left(\frac{v_{B'C'}}{m_{BCi}V_T}\right)-1\right] . \qquad (2.1.5\text{-}3)$$

The component for the external BC junction reads correspondingly

$$i_{jBCx} = I_{BCxS}\left[\exp\left(\frac{v_{B^*C'}}{m_{BCx}V_T}\right)-1\right] . \qquad (2.1.5\text{-}4)$$

In many practical cases, both components can be combined into one, i_{jBC}, between B* and C', without loss of accuracy (in, e.g., the output characteristics). This simplifies parameter extraction and reduces the number of model parameters.

2.1.6 Internal base resistance

In HICUM the internal and external base resistance are separately treated. The value of the internal base resistance r_{Bi} depends strongly on operating point, temperature, and mode of transistor operation (d.c., transient, h.f. small-signal). Especially the last mentioned dependence is a very complicated issue for high-speed large-signal switching processes.

The d.c. internal base resistance is modelled by

$$r_{Bi} = r_i \, \psi(\eta) \tag{2.1.6-1}$$

and is in HICUM/Level2 defined by the *effective* emitter dimensions b_E and l_E. Both the resistance r_i and the emitter current crowding function are bias and geometry dependent, and will be given below.

Conductivity modulation is described by the expression [25, 27]

$$\boxed{r_i = r_{Bi0}\frac{Q_0}{Q_0 + \Delta Q_p}}, \tag{2.1.6-2}$$

which is based on the bias dependent portion ΔQ_p of the stored hole charge,

$$\boxed{\Delta Q_p = \Delta Q_{jEi} + \Delta Q_{jCi} + Q_f + Q_r}\,. \tag{2.1.6-3}$$

Q_0 is a model parameter that is often close and physically related to the zero-bias hole charge Q_{p0} [25, 27]. Therefore, Q_0 is calculated from Q_{p0} as

$$\boxed{Q_0 = (1 + f_{DQr0})Q_{p0}} \tag{2.1.6-4}$$

with the factor f_{dQr0} as model parameter. The zero-bias internal base resistance r_{Bi0} is model parameters which is calculated by TRADICA as a function of emitter geometry and zero-bias internal base sheet resistance r_{SBi0}; Fig. 2.1.6/1 shows the typical bias dependence of the (normalized) internal base sheet resistance; the ratio r_{SBi}/r_{SBi0} is proportional to r_i/r_{Bi0}.

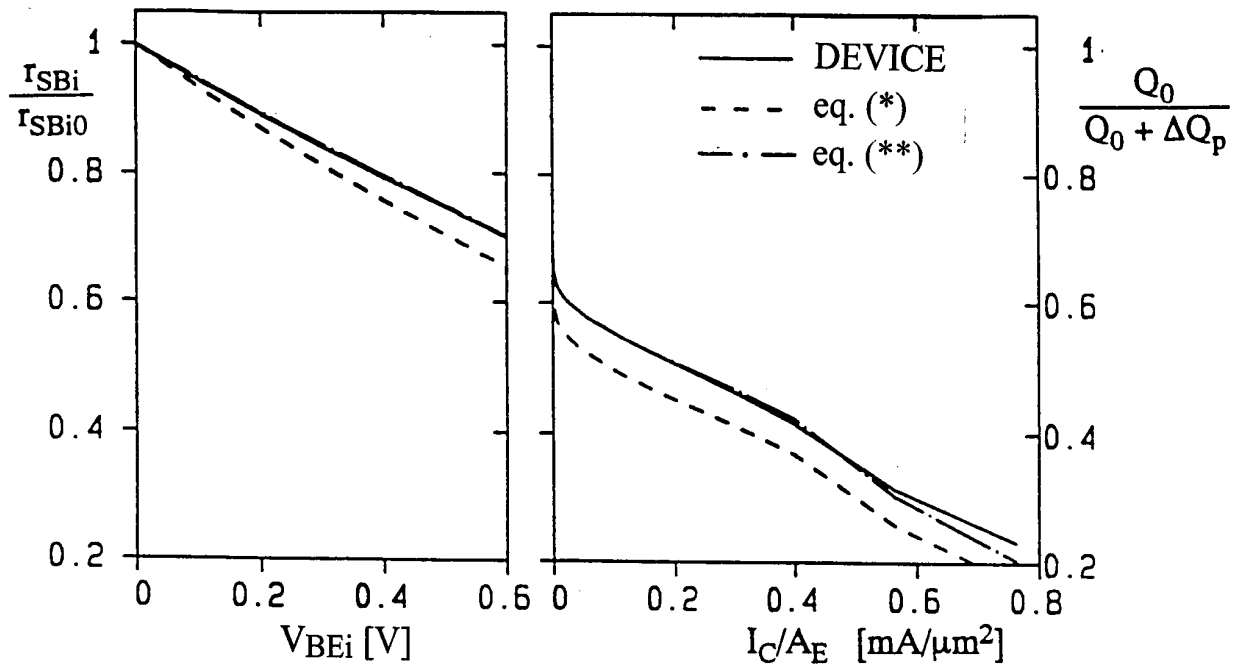


Fig. 2.1.6/1: Typical bias dependence of the normalized internal base sheet resistance and comparison to eq. (2.1.6-2) with $f_{dQr0}=0$ (labeled eq. (*)) and $f_{dQr0}>0$ (labeled eq. (**)) [27]. DEVICE corresponds to (1D) numerical device simulation; ($V_{BEi}=V_{B'E'}$).

For a transistor with n_E emitter contacts (or stripes) and arbitrary aspect ratio $l_E/b_E \geq 1$:

$$r_{Bi0} = r_{SBi0} \frac{b_E}{l_E n_E} g_i \tag{2.1.6-5}$$

with the geometry function [33, 34] for n_E+1 base contacts

$$g_i = \frac{1}{12} - \left(\frac{1}{12} - \frac{1}{28.6}\right)\frac{b_E}{l_E} \quad . \tag{2.1.6-6}$$

The effect of emitter current crowding is described for all aspect ratios $l_E/b_E \geq 1$ by the function [33, 34, 26]

$$\boxed{\psi(\eta) = \frac{\ln(1+\eta)}{\eta}} \tag{2.1.6-7}$$

with the current crowding factor

$$\boxed{\eta = f_{geo}\,\frac{r_i i_{jBEi}}{V_T}} \quad . \tag{2.1.6-8}$$

The factor f_{geo} is a model parameter which takes into account the geometry dependence of emitter current crowding (cf. Chapter 2.1.17).

For transistors with narrow emitter contacts (or stripes) the influence of the charge storage at the emitter periphery on the dynamic transistor behaviour can significantly increase. In order to obtain acceptable computation times and keep the extraction effort reasonable, the HICUM/LEVEL2 equivalent circuit does not contain a complete peripheral transistor element. Therefore, the peripheral charge has to be taken into account by modifying existing elements. The internal base impedance seen between the terminals B*-E' is decreased by the (effective) peripheral charge Q_{fp} to

$$\boxed{r_{Bi}^{*} = r_{Bi0}\frac{\Delta Q_i}{\Delta Q_p} = r_{Bi0}\frac{\Delta Q_i}{\Delta Q_i + Q_{fp}}} \quad . \tag{2.1.6-9}$$

ΔQ_i is the change of the hole charge in the internal transistor during a switching process. For model implementation, however, ΔQ_i is approximated by the change of only the major hole charge contributions w.r.t. equilibrium,

$$\boxed{\Delta Q_i = Q_{jEi} + Q_{fi}} \tag{2.1.6-10}$$

with Q_{fi} as the internal *minority* charge. The latter as well as the peripheral minority charge Q_{fp} can be calculated from the total minority charge Q_f, that is analytically described in the model, using the model parameter f_{Qi},

$$\boxed{Q_{fi} = f_{Qi} Q_f} \quad \text{and} \quad Q_{fp} = (1 - f_{Qi}) Q_f \tag{2.1.6-11}$$

f_{Qi} can be determined from the transit time of transistors with, e.g., different emitter widths. Note, the denominator of (2.1.6-9) contains Q_f directly so that Q_{fp} is not required to be explicitly known or calculated.

For the (high-frequency) small-signal case a similar expression can be derived [13],

$$\boxed{r_{Bi}^{*} = r_{Bi0}\frac{C_i}{C_i + C_{dEp}}} \tag{2.1.6-12}$$

with $C_{dEp} = C_{dE}(1\text{-}f_{Qi})$ as the peripheral diffusion capacitance and

$$\boxed{C_i = C_{jEi} + C_{dEi} + C_{dCi}} \tag{2.1.6-13}$$

as the total capacitance connected to the *internal* base node B'. The use of r_{Bi}^{*} from (2.1.6-9) gives for slow transients or low frequencies a (small) difference compared to the actual d.c. value of r_{Bi}. However, that deviation is usually insignificant because the influence of the peripheral charge or capacitance is large only for narrow emitter stripes where the d.c. internal base resistance is comparatively small. Note again, that for calculating the denominator of (2.1.6-12) C_{dEp} does not need to be known explicitely, but only C_{dE}.

2.1.7 External (parasitic) bias independent capacitances

In addition to junction and diffusion capacitances, that are both operating point dependent, there may exist constant oxide capacitances between base and emitter as well as base and collector. The base-emitter oxide capacitance C_{Eox} is caused by the overlap of emitter poly over base poly. The base collector oxide capacitance C_{Cox} is caused by the overlap of base poly and contact region over the buried layer (or the epi collector). The significance of theses capacitances depends on the technology considered. In order to make HICUM applicable for an as large as possible variety of technologies two "oxide" capacitances are included in the equivalent circuit of Fig. 2.1.1/1.

C_{Eox} takes into account the overlap of emitter and base connection, e.g., n^+ poly-silicon separated from p^+ poly-silicon by the thin spacer oxide in double self-aligned transistors (cf. Fig. 2.1.7/1).

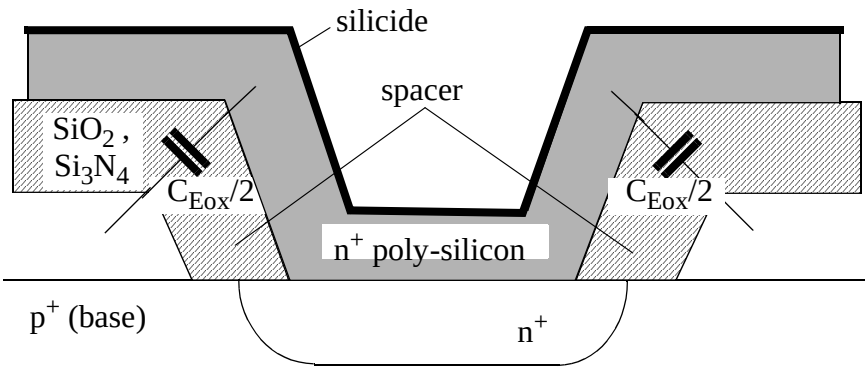


Fig. 2.1.7/1: Physical origin of the BE isolation capacitance C_{Eox}.

In many modern bipolar technologies the base contact is located on a field oxide and causes an additional isolation capacitance C_{Cox} between base and collector terminal (cf. Fig. 2.1.7/2). This capacitance is included in the equivalent circuit within C_{BCx} since its partitioning across r_{Bx} depends on the technology. The parameter f_{BC} determines the actual partitioning of C_{Cox}, too.

Both oxide capacitances are strongly geometry dependent and either have to be measured using proper test structures or can be calculated by TRADICA.

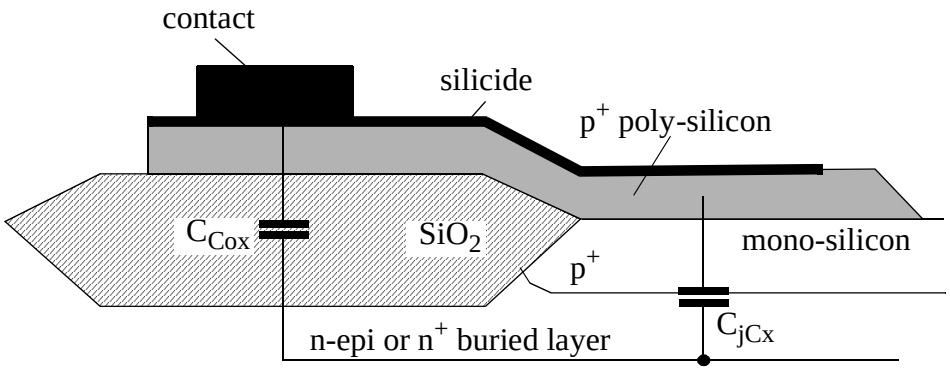


Fig. 2.1.7/2: Physical origin of the BC isolation (overlap) capacitance C_{Cox}.

2.1.8 External series resistances

The resistive regions of the external transistor and the emitter contact are represented in the equivalent circuit of Fig. 2.1.1/1 by bias independent series resistances. The reason for including a substrate resistance in the equivalent circuit will be discussed in Section 2.1.11.

A. External base resistance

Fig. 2.1.8/1 contains a cross section through the external base region of a double-poly self-aligned bipolar transistor. The external base resistance r_{Bx} consists of the following components:

- base contact resistance, r_{KB};
- resistance of the poly-silicon on the field oxide, r_{po};
- resistance of the poly-silicon on the mono-silicon, r_{pm};
- (link) resistance under the spacer, r_{sp}.

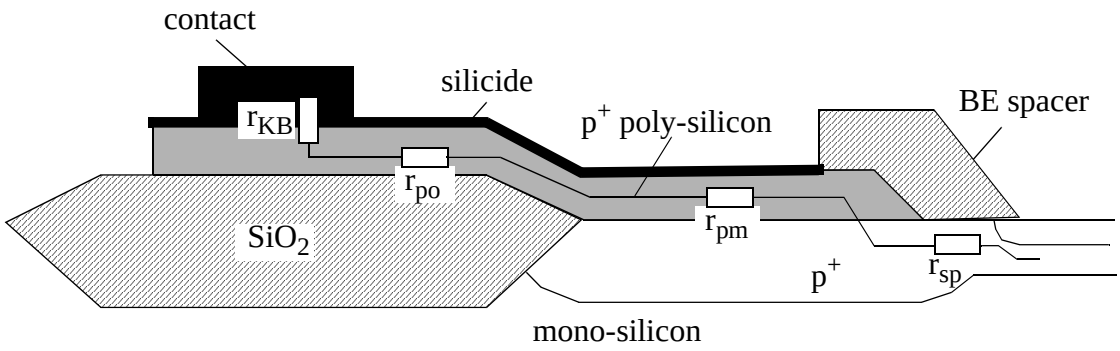


Fig. 2.1.8/1: The various components of the external base resistance.

The value of each of these components depends on the dimensions of the region and the corresponding sheet resistance or specific resistivity [33, 34]. The external base resistance is then given by:

$$r_{Bx} = r_{KB} + r_{po} + r_{pm} + r_{sp} \quad . \tag{2.1.8-1}$$

Many advanced processes use a silicide with a sheet resistance of typically 2...8 Ω/sq. As a consequence, r_{po} and a portion of r_{pm} are significantly reduced and become small compared to the contact and, especially, the link resistance.

For short emitters and transistors with a one-sided base contact only, 3D effects become important that are taken into account by TRADICA's resistance calculations according to [33, 34].

B. External collector resistance

Fig. 2.1.8/2 contains a cross section through the buried layer and collector region of a bipolar transistor. The external collector resistance r_{Cx} consists of the following components:

- collector contact resistance, r_{KC};
- resistance of the sinker region, r_{sink}, connecting contact and buried layer;
- resistance of the buried layer, r_{bl}.

The value of each of these components depends on the dimensions of the region and the corresponding sheet resistance or specific resistivity [42]. The external collector resistance is then given by:

$$r_{Cx} = r_{KC} + r_{sink} + r_{bl} \quad . \tag{2.1.8-2}$$

The external collector resistance does *not* contain any resistance component from the epitaxial layer under the emitter. If r_{KC} is determined by the poly-mono-silicon interface resistance it would be about the same as the emitter contact resistance.

The distributed collector current flow in multi-emitter transistors as well as a different number and location of collector stripes (or contacts) is taken into account in TRADICA by using special formulas. Also, for short emitter (and collector) stripes, current spreading in the buried layer is included in the resistance calculations.

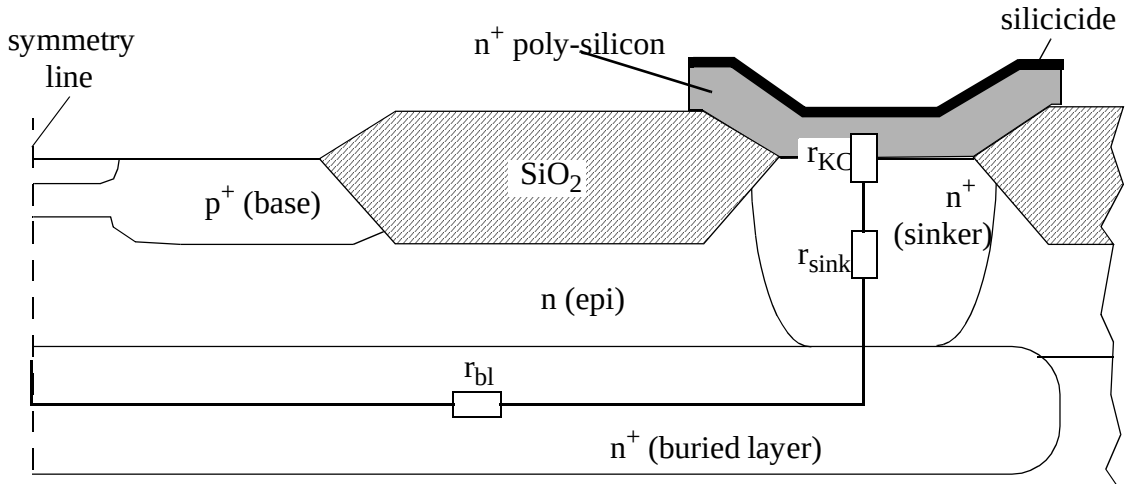


Fig. 2.1.8/2: The various components of the external collector resistance.

C. Emitter resistance

The emitter resistance r_E consists of the following (major) components:

- metallization resistance, r_{Em};
- poly-silicon resistance, r_{Ep};
- resistance of the interface between poly-silicon and mono-silicon, r_{Ei};
- resistance of the mono-silicon bulk region, r_{Eb}.

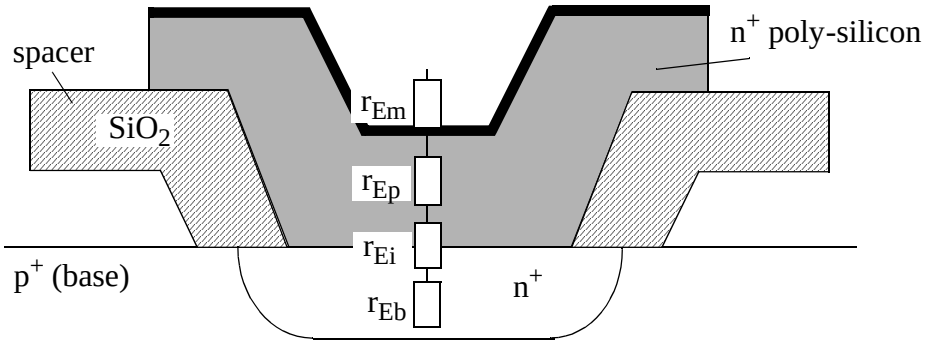


Fig. 2.1.8/3: The various components of the emitter resistance.

For many processes, measurements have been showing a direct proportionality of r_E with the reciprocal emitter window area. As a consequence, it is assumed that the emitter resistance for technologies with poly-silicon emitter is mainly determined by the resistance r_i at the interface between poly- and mono-silicon, and that contributions from the other regions are of minor importance. However, this has to be verified for each particular process.

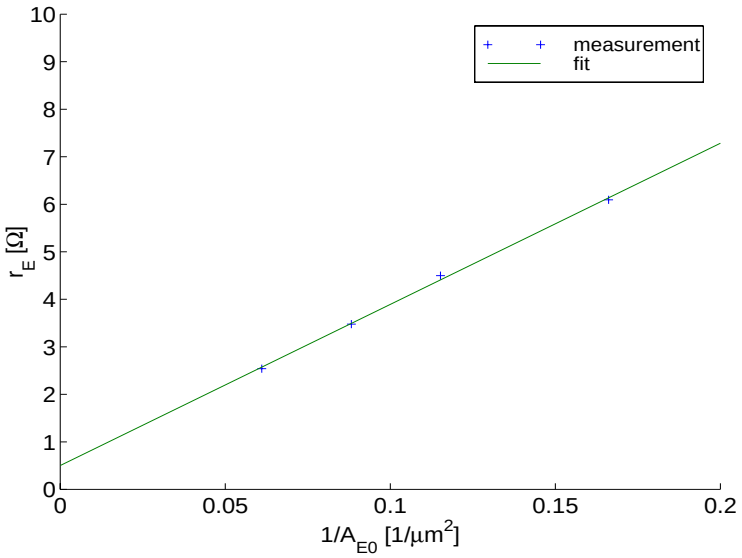


Fig. 2.1.8/4: Measured emitter resistance vs. reciprocal emitter window area and comparison to the scaling equation $r_E = \bar{r}_E / A_E + r_0$ with $\bar{r}_E$ as area specific emitter resistance in [Ωµm^2] and r_0 as residual (parasitic) probe resistance.

2.1.9 Non-quasi-static effects

Non-quasi-static (NQS) effects are occurring at high-frequencies or fast switching processes. Note, that the designation "high" or "fast" is relative and depends on the technology employed. NQS effects exist in both vertical and lateral spatial direction.

a) Vertical direction

It is well-known from “classical” transistor theory that at high frequencies the minority charge Q_f and the transfer current i_T are reacting delayed w.r.t. the voltages across both pn-junction (e.g. [50]). This effect is taken into account in HICUM by introducing additional delay times for both Q_f and I_{Tf}. These additional delay times are modelled as a function of bias by relating them to the transit time [13]:

$$\boxed{\tau_2 = \alpha_{Qf}\tau_f \qquad \text{and} \qquad \tau_m = \alpha_{iT}\tau_f} \ . \tag{2.1.9-1}$$

The factors α_{Qf} and α_{iT} are model parameters. The assumption of a stiff coupling between the additional delay times and the transit time has to be regarded as a first order approximation, especially at high current densities where a certain current dependence of α_{Qf} and α_{iT} has been observed [37]. However, it is questionable whether a more complicated modelling of τ_2 and τ_m is justified from an application point of view [13]. Note, that the SGPM only allows τ_m to be specified for *one* (fixed) operating point. Fig. 2.1.9/1 shows the NQS factors as a function of collector current density for a 15GHz process.

The additional time delay, which results in an excess phase in the frequency domain, is implemented in HICUM using a second order Bessel polynomial [49] for both time and frequency domain analysis in order to maintain consistency of the respective results. The ideal delay proposed in [50] would cause implementation problems in a circuit simulator for time domain analysis. The use of a Bessel polynomial avoids those problems and leads to the same results in the frequency range of practical interest.

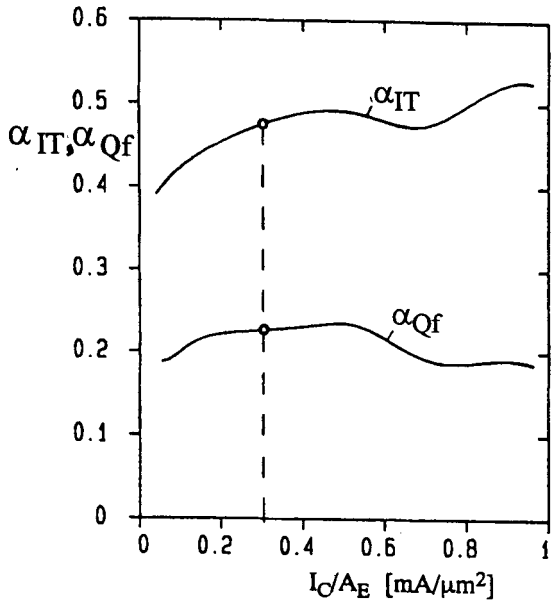


Fig. 2.1.9/1: NQS factors as a function of collector current density calculated from 1D device simulation; V_{CE} = 1.5V.

b) Lateral direction

Dynamic emitter current crowding causes at high frequencies (or fast transients) a reduction of the impedance seen into the internal base node compared to d.c. or low-frequency conditions.

For the small-signal case the distributed character of the internal base region can be modelled by shunting an adequate capacitance C_{rBi} in parallel to the d.c. resistance r_{Bi}. An analytical treatment of the small-signal input impedance of a stripe emitter transistor with $l_E/b_E >> 1$ results for not too high frequencies in

$$\boxed{C_{rBi} = f_{CrBi} C_i} \tag{2.1.9-2}$$

with C_i as the total capacitance connected to the internal base node B',

$$\boxed{C_i = C_{jEi} + C_{jci} + C_{dE} + C_{dC}} \tag{2.1.9-3}$$

From theory $f_{CrBi} = 0.2$ for a long rectangular emitter stripe [21]. In general though, f_{CrBi} depends on the emitter geometry; for instance, it increases (slightly) for smaller emitter aspect ratios. Therefore and to provide maximum flexibility, f_{CrBi} is considered as a model parameter.

Note, that for fast large-signal transient applications, the use of C_i is less justified since the transient current crowding violates the assumptions upon which the derivation of (2.1.9-2) is based.

2.1.10 Breakdown

2.1.10.1 Collector-Base Breakdown

HICUM contains a breakdown model for the base-collector junction that is valid for a weak avalanche effect and a planar breakdown occurring in the internal transistor, i.e. below the emitter. The latter is a reasonable assumption because published measurements for (self-aligned) poly-silicon emitter transistors show such a planar breakdown rather than a breakdown at the periphery of the external BC-junction. The model, which is described also in [39], is intended to indicate the onset of breakdown. In how far, however, it is suited for a simulation and design of circuits somewhat within the breakdown regime depends on the numerical robustness of the particular circuit simulator. Also, the present model does not include breakdown at high current densities, where the maximum electric field occurs at the buried layer rather than at the BC junction. The related instabilities (such as snap-back) would cause convergence problems for most circuit simulators.

The model equation for the element I_{AVL} in Fig. 2.1.1/1 is based on the well-known relationship

$$i_{AVL} = I_T \int_0^{w_{BC}} a_n \exp(-b_n/|E|)\,\mathrm{dx} \tag{2.1.10-1}$$

The ionization rate a_n and the field b_n are coefficients describing the Avalanche process, E is the electric field within the junction region, x is the ordinate in vertical direction, and w_{BC} is the width of the BC depletion region. From this, the avalanche generation current can be approximated by

$$i_{AVL} = i_T\, f_{AVL}(V_{DCi} - v_{B'C'}) \exp\left(-\frac{q_{AVL}}{C_{jCi}(V_{DCi} - v_{B'C'})}\right) \tag{2.1.10-2}$$

with the model parameters

$$f_{AVL} = 2a_n/b_n \quad , \tag{2.1.10-3}$$

$$q_{AVL} = b_n \varepsilon A_E/2 \, , \tag{2.1.10-4}$$

which depend on emitter area, physical data and temperature (via a_n and b_n).

The possible numerical instability in (2.1.10-2) at $v_{B'C'}=V_{DCi}$ can be avoided by replacing the term $(V_{DCi}-v_{B'C'})$ by the normalized depletion capacitance, $C_c=C_{jCi}(v_{B'C'})/C_{jCi0}$, leading to the expression

$$i_{AVL} = I_T \frac{f_{AVL} V_{DCi}}{C_c^{1/z_{Ci}}} \exp\left(-\frac{q_{AVL}}{C_{jCi0} V_{DCi}} C_c^{(1/z_{Ci}-1)}\right), \qquad (2.1.10\text{-}5)$$

which is continuously differentiable via C_c. From a computational point of view, however, i_{AVL} can also simply be set to zero for $v_{B'C'}\geq 0$. At large reverse bias $v_{B'C'}<-q_{AVL}/C_{jCi0}$, i_{AVL} is linearized to avoid convergence problems.

Fig. 2.1.10/1 shows the ratio i_{AVL}/I_T, which is proportional to the multiplication factor, as function of the normalized BC voltage for different values of the exponent coefficient $q_{AVL}/(C_{jCi0}V_{DCi})$.

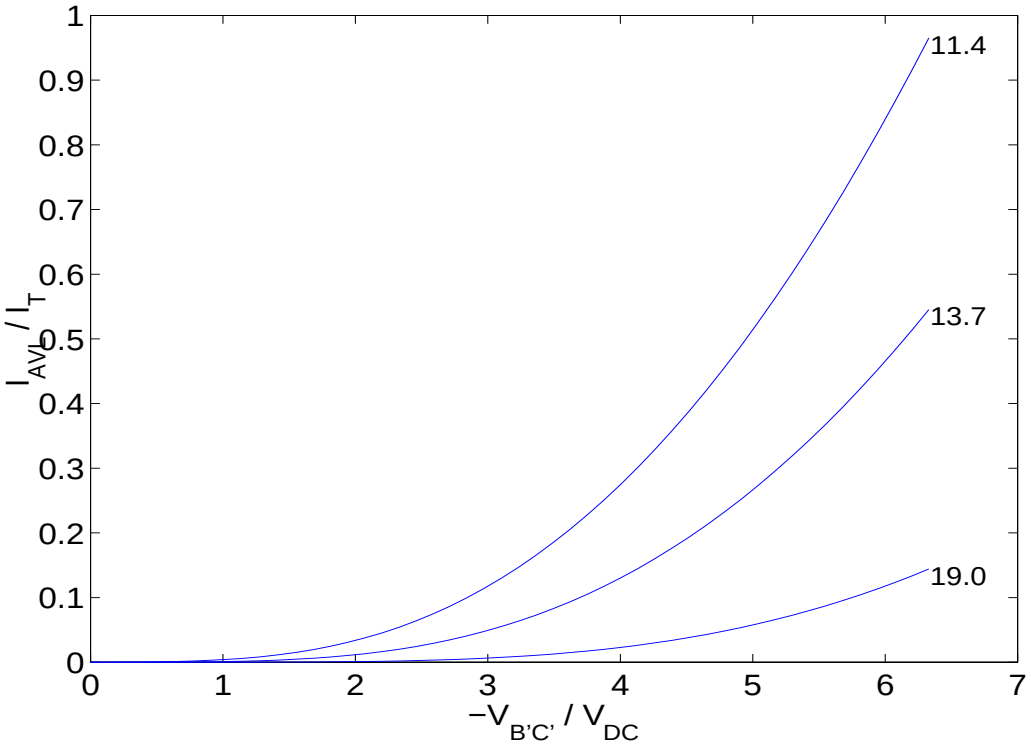


Fig. 2.1.10/1: Avalanche current i_{AVL} normalized to the transfer current I_T as a function of the normalized BC voltage for various values of the exponent coefficient $q_{AVL}/(C_{jCi0}V_{DCi})$ (see labels). Model parameter used: $C_{jCi0}=0.56\text{fF}/\mu\text{m}^2$, $V_{DCi}=0.79\text{V}$, $z_{Ci}=0.307$.

2.1.10.2 Emitter-base breakdown

In advanced bipolar transistors the EB breakdown voltage is usually around 1...3V due to the high doping concentrations. As a result, the breakdown effect in advanced (high-speed) transistors corresponds to a tunnelling mechanism.

The model equation employed in HICUM (cf. [39]) is based on the expression for the tunnelling current density [46]

$$J_{BEt} = \frac{\sqrt{2m^*/E_G}\, q^3(-V)}{h^2} E_{BEj} \exp\left[-\frac{8\pi\sqrt{2m^*E_G}E_G}{3qhE_{BEj}}\right] \quad . \tag{2.1.10-6}$$

E_G is the bandgap energy, m^* is the effective electron mass, h is the Planck constant, and V is the voltage across the respective BE junction; i.e. $V=V_{B'E'}$ for the bottom junction or $V=V_{B^*E'}$ for the perimeter junction. E_{BEj} is the electric field at the junction which - according to the theory of abrupt junctions - can be expressed as

$$E_{BEj} = 2\frac{V_{DE}-V}{w_{BE}} \tag{2.1.10-7}$$

with V_{DE} as built-in voltage of the respective junction. w_{BE} is the space charge region width of that junction and given by

$$w_{BE} = w_{BE0}(1-V/V_{DE})^{z_E} \tag{2.1.10-8}$$

with the zero-bias value

$$w_{BE0} = \begin{cases} \varepsilon_{Si}A_{E0}/C_{jEi0} & \text{, bottom junction} \\ \varepsilon_{Si}P_{E0}\left(0.8\frac{\pi}{2}x_{je}\right)/C_{jEp0} & \text{, perimeter junction} \end{cases} \tag{2.1.10-9}$$

P_{E0} and A_{E0} are the emitter window perimeter and area, respectively, and x_{je} is the vertical junction depth. C_{jEi0} and C_{jEp0} are the zero-bias depletion capacitance of the bottom and perimeter junction, respectively. The factor $0.8(\pi/2)x_{je}$ approximates the perimeter junction curvature caused by lateral

outdiffusion of the emitter doping. Inserting (2.1.10-7 to 2.1.10-9) back into (2.1.10-6), defining a normalized voltage $V_e=V/V_{DE}$, and multiplying with the respective area yields for the tunnelling current

$$i_{BEt} = I_{BEtS}(-V_e)(1-V_e)^{1-z_E}\exp[-a_{BEt}(1-V_e)^{z_E-1}] \quad . \tag{2.1.10-10}$$

Fig. 2.1.10/2 shows the normalized tunneling current as a function of normalized junction voltage.

For numerical reasons, the $1-V_e$ terms are converted to terms that contain the respective normalized bias dependent depletion capacitance $C_e=C_{jE}(v)/C_{jE0}$, which has been made numerically stable at $V_e=1$. Using the classical $C_{jE}(v)$ relationship which is valid at the reverse bias of interest,

$$(1-V_e)C_e = C_e^{1-1/z_E} \quad , \tag{2.1.10-11}$$

leads to the final formulation

$$\boxed{i_{BEt} = I_{BEtS}(-V_e)C_e^{1-1/z_E}\exp[-a_{BEt}C_e^{1/z_E-1}]} \quad . \tag{2.1.10-12}$$

The "saturation" current

$$I_{BEtS} = 2\frac{\sqrt{2m^*/E_G}\,q^3V_{DE}^2}{h^2\varepsilon_{Si}}C_{jE0} \tag{2.1.10-13}$$

and the coefficient

$$a_{BEt} = \frac{8\pi\sqrt{2m^*E_G}E_G}{3qh}\;\frac{w_{BE0}}{2V_{DE}} \tag{2.1.10-14}$$

are model parameters, that depend on physical and process data as well as on geometry. i_{BEt} is a continuously differentiable expression since the depletion capacitance is continuously differentiable.

In most processes, the breakdown effect occurs first at the peripheral emitter junction, because the doping concentrations are highest there, and due to the curvature of that junction which leads

to a narrower space-charge region and, thus, to a higher electric field. In this case, C_{jE0}, V_{DE}, z_E, and V_e in the above equations have to be replaced by C_{jEp0}, V_{DEp}, and z_{Ep} and $v_{B*E'}/V_{DEp}$.

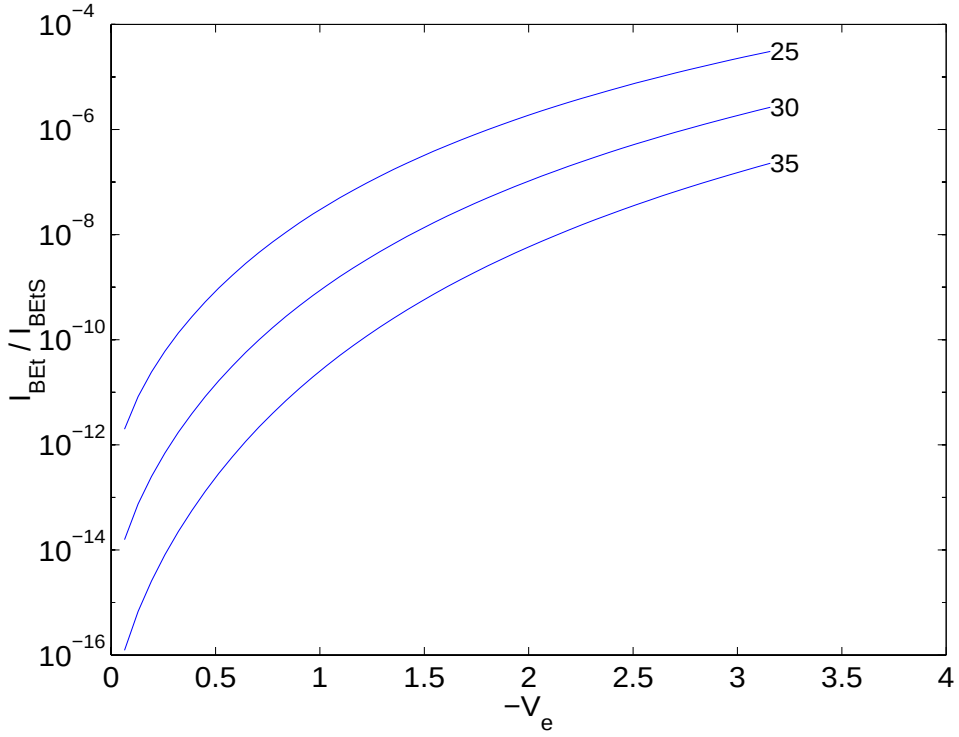


Fig. 2.1.10/2: Normalized tunneling current as a function of normalized junction voltage $V_e=V/V_{DE}$ for various values of a_{BEt}. Model parameters used: $V_{DE}=0.95V$, $z_E=0.5$.

2.1.11 Substrate network

The substrate contact of a transistor may be at the bottom of the wafer only or, more preferably, at the surface. But even the surface contact is usually located relatively far away from the CS junction, so that a significant resistance r_{Su} may exist in series to the CS depletion capacitance, due to the usually quite high substrate resistivity ρ_{Su}. In addition, the high permittivity of silicon, ε_{Si}, leads to a capacitance C_{Su} in parallel to r_{Su} that becomes important at high operating speed. Physically, the connection between the substrate contact and the CS depletion capacitance can be partitioned into a bulk (or bottom) and a periphery RC network [20] (cf. also Fig. 2.1.17/4), each of which having the time constant $\tau_{Si}=\rho_{Su}\varepsilon_{Si}$. For practical applications in a compact model, however, a simplified network is employed that combines bottom and periphery components into one RC equivalent circuit (cf. Fig. 2.1.1/1). The values of r_{Su} and C_{Su} are strongly geometry dependent.

Fig. 2.1.11/1 shows the impact of the substrate coupling on the frequency dependent output conductance of a 25GHz process (see also [15]).

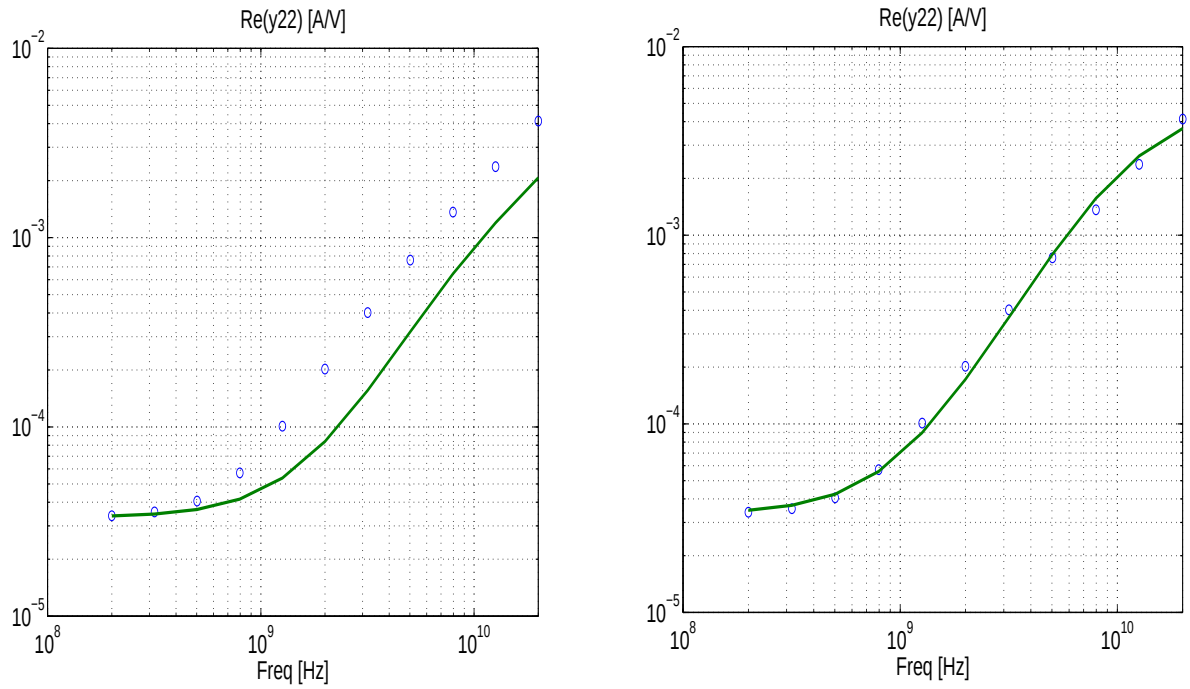


Fig. 2.1.11/1: Impact of intra-device substrate-coupling on transistor output conductance (real part of y_{22}) as function of frequency. Comparison of measurements (symbols) and HICUM (lines): (a) model without substrate network r_{su}, C_{su}; (b) model with substrate network. Emitter size: 0.4*14µm^2; bias point: I_C/A_E=0.22 mA/µm^2, V_{CE}=0.8V.

2.1.12 Parasitic substrate transistor

Under certain electrical circumstances, the parasitic substrate transistor can be turned on, depending also on the processes and layout of the transistor. First of all, one can distinguish between a bulk substrate transistor given by the buried layer area and - dependent on the process - a peripheral substrate transistor. The most likely electrical condition for turning on the substrate transistor is a forward-biased BC junction which occurs either at high current densities under the emitter (internal BC junction) or if the transistor is operated in hard saturation (external and internal BC junction). An example for this are power amplifiers, in which the transistor is operated in hard saturation with $V_{CE} \rightarrow V_{CEs}$ and strongly forward biased V_{BC}. Another condition for turning on the substrate transistor is a forward biased CS junction caused by voltage drops in the substrate (latch-up).

Since the bulk substrate transistor usually has a current gain of less than 1 due to the highly doped and wide buried layer, its influence is negligible and needs not to be considered at high collector current densities. Device simulations confirmed this for an advanced bipolar process. A peripheral substrate transistor action can be avoided by a surrounding collector sinker with high enough doping concentration at the buried layer depth. Also, this peripheral transistor does not exist at all in trench-isolated processes.

In (npn) transistors without surrounding collector sinker, however, the epitaxial collector acts as a lightly doped base between the external base (now the emitter) and the substrate (now the collector), resulting in a pnp transistor with considerable current gain that may be required to be modelled in addition to the vertical npn transistor. HICUM contains a simplified substrate transistor model in order to take the corresponding effects into account.

The parasitic substrate transistor consists of the elements i_{Ts}, i_{SC}, C_{jS}, i_{BCx} and C_{BCx} in the equivalent circuit of Fig. 2.1.1/1. While C_{jS}, i_{BCx} and C_{BCx} already belong to the standard HICUM equivalent circuit, a substrate *transistor* action requires the addition of a substrate transfer current source. Since substrate transistor action is considered as second order effect, a simplified model has been chosen for i_{Ts}:

$$\boxed{i_{TS} = I_{TSf} - I_{TSr} = I_{TSS}\left[\exp\left(\frac{v_{B*C'}}{m_{Sf}V_T}\right) - \exp\left(\frac{v_{S'C'}}{m_{Sr}V_T}\right)\right]} \qquad (2.1.12\text{-}1)$$

with the saturation current I_{TSS} and the emission coefficients m_{Sf} and m_{Sr} as model parameters. The second term is only relevant if the SC junction becomes forward biased which of little practical importance; therefore, to reduce the number of model parameters, $m_{Sf} = m_{Sf}$ is assumed.

In case of a forward biased SC junction, also a "base" current component exists, that is modelled by the diode equation:

$$\boxed{i_{SC} = I_{SCS}\left[\exp\left(\frac{v_{S'C'}}{m_{SC}V_T}\right) - 1\right]} \qquad (2.1.12\text{-}2)$$

with the saturation current I_{SCS} and the emission coefficient m_{SC} as model parameters. Although this current (and its derivative) are usually of little practical relevance it is generally useful for simulator convergence.

The minority charge storage in the epitaxial region under the external base is taken into account by a diffusion charge

$$\boxed{Q_{dS} = \tau_{Sf}\, i_{TSf}} \qquad (2.1.12\text{-}3)$$

with the forward transit time τ_{Sf} as a model parameter of the substrate transistor. τ_{Sf} depends on the average current path (neutral base width) under the external base and at the buried layer periphery. So far, the classical base transit time expression turned out to be a good approximation for estimating the value of τ_{Sf}. Also, device simulations have shown that for high-speed processes the stored charge represented by Q_{dS} has only negligible effect on transistor switching out of hard saturation.

Note, that in advanced bipolar processes the emitter terminal of the substrate transistor (B*) moves towards the (npn) base contact (B), which makes the external realization of such a parasitic transistor by a subcircuit even easier.

2.1.13 Small-signal Equivalent circuit

Fig. 2.1.13/1 shows the small-signal EC, that can be derived from the large-signal EC in Fig. 2.1.1/1. Nonlinear elements that depend on their branch voltage only, such as diodes, have been replaced by their conductances. Nonlinear elements that are controlled by other than their branch voltage, such as transfer current sources and the avalanche current source, are replaced by the respective controlled source and a possible conductance. The latter contains the direct dependence of the nonlinear current source on the branch voltage while the controlled source is designated by a complex current symbol. The respective most important derivatives for the nonlinear elements are given below and can be calculated once the currents and charges are available.

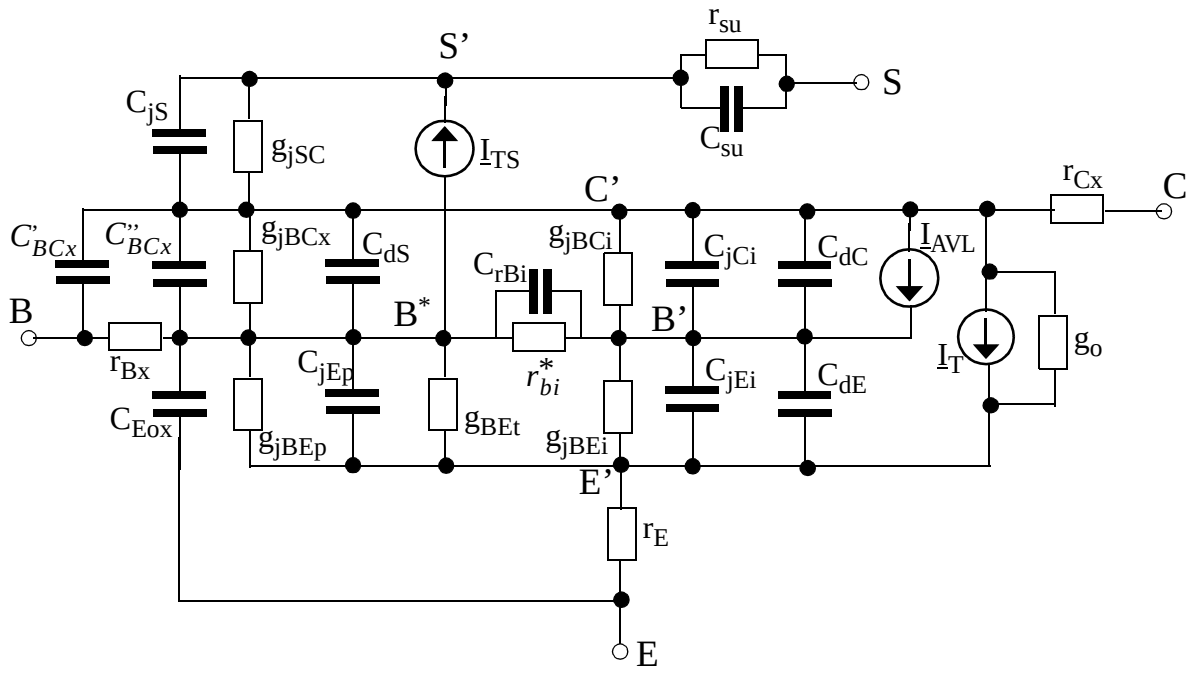


Fig. 2.1.13/1: Small-signal HICUM/Level2 equivalent circuit. The external BC capacitance consists of a depletion and a bias independent (e.g., oxide) capacitance with the ratio C'_{BCx}/C''_{BCx} being adjusted with respect to proper modelling of the h.f. behavior. The elements associated with the derivatives caused by self-heating are not shown.

The capacitances C_{BCx}, C_{jEp}, C_{jEi}, C_{jCi} and C_{jS}, the parasitic isolation capacitances, and the (bias independent) series resistances have already been defined in the previous sections. The diode element current equations are linearized as usual to give the respective conductances g_{jBEp}, g_{jBEi}, g_{jBCi}, g_{jBCx}, g_{jSC}, which read in general

$$g_{jn} = \frac{I_{nS}}{m_n V_T}\exp\left(\frac{V}{m_n V_T}\right) = \frac{I_{jn} + I_{nS}}{m_n V_T} \tag{2.1.13-1}$$

with n={BEp, BEi, BCi, BCx, SC} and V as the respective branch voltage.

The conductance of the tunneling current element follows directly from eq. (2.1.10-10),

$$g_{BEt} = \frac{dI_{BEt}}{dV} = \frac{I_{BEtS}}{V_{DE}}\exp\left[-\frac{a_{BEt}}{(1-V_e)^{1-z_E}}\right]\left[1-\frac{V_e(1-z_E)}{1-V_e}[(1-V_e)^{1-z_E}+a_{BEt}]\right]$$

in which $1\text{-}V_e$ can be converted into the continuously differentiable capacitance ratio:

$$g_{BEt} = \frac{I_{BEtS}}{V_{DE}}\exp(-a_{BEt}C_e^{1/z_E-1})[1-V_e(1-z_E)C_e^{1/z_E}(C_e^{1/z_E-1}+a_{BEt})] \tag{2.1.13-2}$$

The forward transfer I_{Tf} current depends on $V_{B'E'}$ and $V_{B'C'}$ (or $V_{C'E'}$) and, therefore, leads to a voltage controlled current source $g_{mf}\underline{V}_{B'E'}$ and the output conductance element g_o. The various conductances of the transfer current that are required for the small-signal equivalent circuit are calculated in HICUM/L2 as follows:

$$S_{fb} = \left.\frac{dI_{Tf}}{dV_{B'E'}}\right|_{V_{B'C'}} = \frac{I_{Tf1}}{V_{Tf}}\cdot\frac{Q_{p,T}+\tau_r I_{Tr}-h_{jei}C_{jEi}V_{Tf}}{Q_{p,T}+\tau_r I_{Tr}+\tau_{f,T}I_{Tf1}d_{ch}}d_{ch} \tag{2.1.13-3}$$

with I_{Tf1} from (2.1.2-13), $Q_{p,T}$ from (2.1.2-3), $V_{Tf} = m_{Cf}V_T$,

$$d_{ch} = 1 + 2I_{Tf1}/I_{ch} \tag{2.1.13-4}$$

and

$$\tau_{f,T} = \left.\frac{dQ_{f,T}}{dI_{Tf}}\right|_{V_{B'C'}} . \tag{2.1.13-5}$$

The latter is calculated for the simple (1D) case analytically from the already known transit time contributions and weighting factors (model parameters). If collector current spreading is included (LATB and/or LATL greater than zero), $\tau_{f,T}$ is calculated numerically due to the smaller number of arithmetic operations compared to the corresponding full analytical expression.

The forward component of the output conductance reads

$$S_{fc} = \left.\frac{dI_{Tf}}{dV_{C'E'}}\right|_{V_{B'E'}} = \frac{I_{Tf1}}{V_{Af}} \cdot \frac{d}{1 + d\ \tau_{f,T} I_{Tf1} / Q_{p,T}} \tag{2.1.13-6}$$

with a bias dependent “Early” voltage

$$V_{Af} = \frac{Q_{p,T}}{h_{jci} C_{jCi} - \left.\frac{dQ_f}{dV_{C'E'}}\right|_{V_{B'E'}}} \tag{2.1.13-7}$$

and the (bias dependent) factors

$$d = d_{ch}\frac{e}{1+e} \quad \text{and} \quad e = \exp\left(\frac{v_c}{V_T} - 1\right) . \tag{2.1.13-8}$$

The latter factor results from the smoothing function for I_{CK}.

The corresponding inverse conductances are

$$S_{rb} = \left.\frac{dI_{Tr}}{dV_{B'E'}}\right|_{V_{B'C}} = \frac{I_{Tr}}{V_T} \cdot \frac{Q_{p,T} - (h_{jei} C_{jEi} + h_{jci} C_{jCi} + \tau_{f,T} S_{fb}) V_T}{Q_{p,T} + \tau_r I_{Tr}} \tag{2.1.13-9}$$

and

$$S_{rc} = \left.\frac{dI_{Tr}}{dV_{C'E'}}\right|_{V_{B'E'}} = -\frac{I_{Tr}}{V_T} \cdot \frac{Q_{p,T} + (\tau_{f,T} S_{fc} - h_{jci} C_{jCi}) V_T}{Q_{p,T} + \tau_r I_{Tr}} \tag{2.1.13-10}$$

From these derivatives follows the transconductance in common-emitter configuration ($dV_{B'E'}=dV_{B'C'}$)

$$g_m = \left.\frac{dI_T}{dV_{B'E'}}\right|_{V_{C'E'}} = y_{21}(\omega{=}0) = S_{fb} + S_{rb} \tag{2.1.13-11}$$

and the output conductance in common-emitter configuration

$$g_o = \left.\frac{dI_T}{dV_{C'E'}}\right|_{V_{B'E''}} = y_{22}(\omega=0) = -(S_{fc} + S_{rc}) \quad . \tag{2.1.13-12}$$

The resulting small-signal transfer current is then given by

$$\boxed{\underline{I}_T = S_{fb}\underline{V}_{B'E'} - S_{rb}\underline{V}_{B'C'}} \quad . \tag{2.1.13-13}$$

If non-quasi-static effects are included, the transconductance S_{fb} becomes complex.

Outside of the high-current region, the forward conductances reduce to

$$g_m \approx g_{mf} = \frac{I_{Tf1}}{V_T} f \cdot \frac{Q_p - h_{jei} C_{jEi} V_{Tf}}{Q_{p,T} + \tau_f I_{Tf}} \tag{2.1.13-14}$$

and

$$g_o \approx I_{Tf} \frac{h_{jci} C_{jCi}}{Q_p + \tau_f I_{Tf}} \approx \frac{I_{Tf1}}{V_{Af}} \quad . \tag{2.1.13-15}$$

Since $h_{jCi}<1$ for a (positive) bandgap grading in the base, an HBT has a higher Early voltage and lower output conductance than a homojunction transistor. For experimental examples of the bias and frequency dependence of the above conductances see chapter 6.

The conductances of the avalanche current element read

$$\boxed{g_{AVL,b} = \left.\frac{dI_{AVL}}{dV_{B'E'}}\right|_{V_{B'C'}} = k_{AVL} S_{fb} - g_a} \tag{2.1.13-16}$$

and

$$\boxed{g_{AVL,c} = \left.\frac{dI_{AVL}}{dV_{B'C'}}\right|_{V_{B'E'}} = k_{AVL} S_{fc} + g_a} \tag{2.1.13-17}$$

with the “multiplication” factor (cf. eq. (2.1.10-5))

$$\boxed{k_{AVL} = \frac{f_{AVL} V_{DCi}}{C_c^{1/z_{Ci}}} \exp\left(-\frac{q_{AVL}}{C_{jCi0} V_{DCi}} C_c^{(1/z_{Ci}-1)}\right)} \qquad (2.1.13\text{-}18)$$

and the conductance

$$\boxed{g_a = \frac{I_{AVL}}{V_{DCi}} C_c^{1/z_{Ci}} \left[1 + \frac{q_{AVL}}{C_{jCi0} V_{DCi}} C_c^{(1/z_{Ci}-1)} (1 - z_{ci})\right]} \; . \qquad (2.1.13\text{-}19)$$

The transconductances of the parasitic substrate transistor, which is described by a simple transport model, are given by

$$\boxed{S_{Tsu,\,b} = \frac{I_{TsS}}{m_{Sf} V_T} \exp\left(\frac{v_{B*C'}}{m_{Sf} V_T}\right)} \quad \text{and} \quad \boxed{S_{Tsu,\,s} = -\frac{I_{TsS}}{m_{Sr} V_T} \exp\left(\frac{v_{S'C'}}{m_{Sr} V_T}\right)}, \qquad (2.1.13\text{-}20)$$

resulting in the corresponding small-signal transfer current

$$\boxed{\underline{I}_{Ts} = S_{Tsu,\,b} \underline{V}_{B'C'} - S_{Tsu,\,s} \underline{V}_{S'C'}} \; . \qquad (2.1.13\text{-}21)$$

The BE diffusion capacitance is given by

$$\boxed{C_{dE} = \tau_f S_{fb}} \; , \qquad (2.1.13\text{-}22)$$

while the BC diffusion capacitance is approximated by

$$\boxed{C_{dC} = \tau_r S_{rc} + \tau_f S_{fc}} \; . \qquad (2.1.13\text{-}23)$$

The diffusion capacitance of the parasitic substrate transistors reads

$$\boxed{C_{dS} = \tau_{Sf} S_{Tsu,\,b}} \qquad (2.1.13\text{-}24)$$

and is connected in parallel to C''_{BCx}.

Although the base resistance is bias dependent, the d.c. value is used also for the small-signal case,

$$\boxed{r_{bi}^{*} = r_{Bi}^{*}} \tag{2.1.13-25}$$

which so far turned out to be a reasonable approximation, while at the same time simplifying the implementation significantly.

If self-heating is turned on, the derivatives of the relevant equivalent circuit element variables with respect to the temperature caused by the dissipated power P are also taken into account. The most important derivatives are given below; justified simplifications have been made regarding the derivatives of certain components in order to obtain the fairly compact expression.

The derivatives below are defined for constant voltages at the nodes of the electrical equivalent circuit:

$$\boxed{\left.\frac{dI_{Tf}}{dT}\right|_{V} = S_{fT} \cong \frac{I_{Tf1}}{T}\frac{\left[3 + \dfrac{V_{Gb} - V_{B'E'}}{m_{Cf}V_T}\right]}{1 + \dfrac{\tau_{f,T}I_{Tf1}}{Q_{p,T}}}}, \tag{2.1.13-26}$$

$$\boxed{\left.\frac{dI_{AVL}}{dT}\right|_{V} = S_{fTav} \cong k_{AVL}S_{fT}}, \tag{2.1.13-27}$$

$$\boxed{\left.\frac{dP}{dT}\right|_{V} = S_{pT} = V_{C'E'}S_{fT} - V_{B'C'}S_{fTav} + \ldots}. \tag{2.1.13-28}$$

In addition, the dissipated power requires derivatives with respect to node voltages, assuming a constant temperature (= voltage at the thermal node):

$$\boxed{\left.\frac{dP}{dV_{B'}}\right|_{V,\Delta T} = V_{C'E'}(S_{fb} - S_{fr}) - [V_{B'C'}S_{fbav} + I_{AVL}]}, \tag{2.1.13-29}$$

$$\boxed{\left.\frac{dP}{dV_{C'}}\right|_{V,\Delta T} = [V_{C'E'}(S_{fc} - S_{rc}) + I_T] - [V_{B'C'}S_{fbav} - I_{AVL}]}. \tag{2.1.13-30}$$

2.1.14 Noise model

The noise behaviour is modelled by employing the small-signal equivalent circuit in Fig. 2.1.13/1 and adding to all series resistances, diodes, and to the transfer current source their corresponding equivalent noise current sources. Compared to the SGPM, the more sophisticated equivalent circuit and more accurate model equations of HICUM/L2 allow a more accurate overall description of the noise behaviour, especially at high frequencies (e.g. [40]).

In ohmic resistances thermal noise is taken into account by an equivalent noise current source

$$\boxed{\overline{I_r^2} = \frac{4k_B T \Delta f}{r}} \qquad (2.1.14\text{-}1)$$

with r = r_E, r_{Cx}, r_{Bx}, or $r_{Bi,n}$ (cf. below). k_B is the Boltzmann constant, T the temperature, and Δf is the frequency interval. Investigations have shown that for certain processes a distributed model of the internal base yields an improved description of the high-frequency noise behaviour. However, in order to avoid either swapping transistor models as a function of simulation mode or larger simulation time in general by using a two- or multi-transistor model, a factor k_{rBi} is available as an additional model parameter. Therefore, for noise calculations, a modified internal base resistance can be used:

$$r_{Bi,n} = k_{rBi}\, r_{Bi}^{*} \quad . \qquad (2.1.14\text{-}2)$$

Shot noise is assumed for transfer currents, such as

$$\boxed{\overline{I_T^2} = 2qI_T\, \Delta f}, \qquad (2.1.14\text{-}3)$$

as well as for the avalanche current I_{AVL} and for currents across junctions (diode currents),

$$\boxed{\overline{I_{j\,diode}^2} = 2qI_{jdiode}\, \Delta f} \ , \qquad (2.1.14\text{-}4)$$

with the index *diode* = {BEi, BCi, BEp, BCx, CS}.

The base current components injected across the BE junction also contain flicker noise, which depends inversely on the frequency f. Investigations of flicker noise in polysilicon-emitter bipolar transistors seem to indicate that the flicker noise is generated at the poly-silicon to mono-silicon

interface [6,7,8]. This corresponds to a strong correlation between the bottom and perimeter component. As a consequence, and for simplification of the noise model and its implementation, the present version contains only one flicker noise source in parallel to g_{jBEi} that combines the bottom and perimeter current,

$$\boxed{\overline{I_{BE}^2} = k_F \left(I_{jBEi} + I_{jBEp}\right)^{a_F} \frac{\Delta f}{f}} \quad , \tag{2.1.14-5}$$

with k_F and a_F as model parameters. Deviations from the 1/f behaviour, which can be caused by, e.g., random telegraph noise, cannot be taken into account by the employed model.

2.1.15 Temperature dependence

Temperature dependence is described in HICUM via those model parameters that are related to physical quantities like intrinsic carrier density or mobility. In the following formulas, T_0 is the reference temperature for which the model parameters have been determined. The formulas are valid for a temperature range between about 250K and 400K, assuming that the model parameters are determined around T_0 = 300K. The validity range depends somewhat on the technology considered. A more detailed description of the physical background of certain formulas employed in HICUM is given in [31, 32].

For all quantities that contain the bandgap energy or its equivalent bandgap voltage V_G, respectively, the assumption of a linear dependence of bandgap with temperature is sufficient in the temperature range specified above. In most circuit simulators, though, this is assumed only for the saturation currents, which are most sensitive to temperature changes, while for the built-in voltages often a more complicated function $V_G(T)$ is used (e.g. [46]) which is valid down to quite low temperatures. However, since effects such as freeze-out are usually not taken into account by compact models, it is not recommended to use a model below about 250K unless its parameters have been extracted or at least verified especially for that temperature range.

For numerical reasons (over- or underflow), some of the original equations have to be modified, mostly towards very temperatures. The respective smoothing functions to be used for circuit simulator implementation are also given below. It is assumed that every circuit simulator prevents negative or zero temperature.

Temperature coefficients (TCs) are designated by the symbol α.

2.1.15.1 Transfer current

The transfer current is strongly temperature dependent via the intrinsic carrier density n_i. Since the square of n_i is contained in the ICCR constant c_{10}, this leads to

$$\boxed{c_{10}(T) = c_{10}(T_0)\left(\frac{T}{T_0}\right)^3 \exp\left[\frac{V_{Gb}}{V_T(T)}\left(\frac{T}{T_0}-1\right)\right]} \quad . \tag{2.1.15-1}$$

The (over the base region) *averaged* bandgap voltage V_{Gb} is a model parameter and

$$V_T(T) = k_B\, T / q \tag{2.1.15-2}$$

is the temperature dependent value of the thermal voltage. Note, that according to the assumption of a linear temperature dependence of the bandgap, V_{Gb} corresponds to the versus T=0 extrapolated value.

The zero-bias hole charge Q_{p0} is only weakly temperature dependent via the influence of base width change with temperature, that is mainly caused by the change in depletion width of the BE junction:

$$\boxed{Q_{p0}(T) \;=\; Q_{p0}(T_0)\left[1 + \frac{z_{Ei}}{2}\left\{1 - \frac{V_{DEi}(T)}{V_{DEi}(T_0)}\right\}\right]} \;. \tag{2.1.15-3}$$

No additional model parameters are required here. Also, for typical values of V_{DEi} in the order of V_{Gb} the value of Q_{p0} will remain positive up to extremely high temperatures. Therefore, a smoothing function is omitted here to keep the computational effort minimal, particularly during self-heating calculations.

2.1.15.2 Base currents and current gain

The forward current gain B_f can be modelled as a simple linear function of T,

$$\boxed{B_f(T) \;=\; B_f(T_0)[1 + \alpha_{Bf}\Delta T]}\,, \tag{2.1.15-4}$$

with the relative temperature coefficient

$$\alpha_{Bf} \;=\; \frac{1}{B_f(T_0)}\frac{dB_f}{dT}\bigg|_{T_0,\, I_C(low)} \tag{2.1.15-5}$$

as a model parameter, which can be easily measured (at low current densities). Since in HICUM not the current gain but the physically independent base current is described, the respective saturation currents are modelled as a function of temperature and current gain TC

$$\boxed{I_{BS}(T) \;=\; I_{BS}(T_0)\left(\frac{T}{T_0}\right)^3 \exp\left[\frac{V_{Gb}}{m_B V_T(T)}\left(\frac{T}{T_0} - 1\right) - \alpha_{Bf}\Delta T\right]}\,, \tag{2.1.15-6}$$

with I_{BS} (= I_{BEiS}, I_{REiS}, I_{BEpS}, I_{REpS}, resp.) and m_B (= m_{BEi}, m_{REi}, m_{BEp}, m_{REp}, resp.). Like the transfer current the main contribution to the temperature dependence is caused by the intrinsic carrier density. However, the relevant bandgap is given by the emitter region and, thus, the V_{Gb} term is corrected here by the term $\alpha_{Bf}\Delta T$ with $\Delta T=T-T_0$, which takes into account the difference between the bandgap in the emitter and base region. In addition, the ideality factor m_B, which is assumed to be temperature independent, occurs as a factor for V_T.

A similar relation, but without the term $\alpha_{Bf}\Delta T$, is used for the saturation currents of the base current components across the BC and CS junction after inserting the respective model parameters. For completeness, an additional parameter α_{Br} could be introduced for instance, but at the expense of an increased number of model parameters for an operation region that is of very little importance for practical applications of bipolar transistors.

2.1.15.3 Transit time and minority charge

The critical current density I_{CK}/A_E depends on temperature via physical parameters like mobility of the epitaxial collector and saturation velocity. The internal collector resistance contains the low-field electron mobility and reads

$$\boxed{r_{Ci}(T) = r_{Ci}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{Ci}}} \quad . \tag{2.1.15-7}$$

The model parameter ζ_{Ci} is a function of the collector doping concentration (e.g., [31, 41]). The voltage V_{lim} contains both mobility and saturation velocity, resulting in

$$\boxed{V_{lim}(T) = V_{lim}(T_0)(1-\alpha_{vs}\Delta T)\left(\frac{T}{T_0}\right)^{\zeta_{Ci}}} \tag{2.1.15-8}$$

with the relative temperature coefficient α_{vs} of the (electron) saturation velocity as model parameter. Designating the above original voltage as V_{lim}^{o}, numerical problems due to negative values of V_{lim} in I_{CK} at very high temperatures are avoided by using the smoothing function

$$V_{lim} = V_T + V_T \ln\left[1 + \exp\left(\frac{V_{lim}^o - V_T}{V_T}\right)\right]. \qquad (2.1.15\text{-}9)$$

The CE saturation voltage can be modelled as a linear function of temperature,

$$V_{C'E's}(T) = V_{C'E's}(T_0)[1 + \alpha_{CEs}\Delta T] \ , \qquad (2.1.15\text{-}10)$$

with α_{CEs} as a model parameter. Its value can be estimated from the difference between the respective relative temperature coefficients of the built-in voltages V_{DEi} and V_{DCi}.

The temperature dependence of the transit time model is given in [41]. Except for the low-current transit time, no additional model parameters are required. The low-current portion of the transit time, τ_{f0}, as a function of temperature is mainly determined by the quadratic temperature dependence of the parameter τ_0:

$$\tau_0(T) = \tau_0(T_0)[1 + \alpha_{\tau 0}\Delta T + k_{\tau 0}\Delta T^2] \ . \qquad (2.1.15\text{-}11)$$

The model parameters $\alpha_{\tau 0}$ and $k_{\tau 0}$ can be expressed by physical quantities.

The time constants τ_{Bfvs} and τ_{pCs} depend on temperature via the same diffusivity (of the collector) and, therefore, the temperature dependence of the composite parameter τ_{hcs} can be expressed as

$$\tau_{hcs}(T) = \tau_{hcs}(T_0)\left(\frac{T}{T_0}\right)^{(\zeta_{Ci}-1)} \ . \qquad (2.1.15\text{-}12)$$

The emitter time constant τ_{Ef0} depend on temperature via mainly the hole diffusivity in the neutral emitter and the current gain. Assuming a large emitter concentration with a negligible temperature dependence of the mobility, the following expression can be obtained:

$$\tau_{Ef0}(T) = \tau_{Ef0}(T_0)\,\frac{T/T_0}{1 + \alpha_B\Delta T} \qquad (2.1.15\text{-}13)$$

which does not require an additional model parameter. Possible numerical problems at extreme temperatures (very high or very low, dependent on the sign of α_B) have to be avoided though; for this, instead of the original denominator $a_o = (1+\alpha_B\Delta T)$ the following denominator is used:

$$\boxed{a = \frac{a_o + \sqrt{a_o^2 + 0.01}}{2}}. \qquad (2.1.15\text{-}14)$$

The temperature dependence of the minority charge and of the additional delay times, that model vertical NQS effects, follows automatically from that of the transit time using (2.1.3-2) and (2.1.9-1), respectively.

2.1.15.4 Depletion charges and capacitances

The key parameter for the temperature dependence of the depletion charges and capacitances is the diffusion (or built-in) voltage. From its proportionality to the bandgap follows

$$\boxed{V_D(T) = V_D(T_0)\frac{T}{T_0} - V_{Gj}\left(\frac{T}{T_0} - 1\right) - 3V_T \ln\left(\frac{T}{T_0}\right)}. \qquad (2.1.15\text{-}15)$$

The bandgap voltage V_{Gj} corresponds to the vs. T=0 extrapolated bandgap voltage including (possible) high doping effects occurring at the respective pn-junction. For simplification, V_{Gj} can be set equal to V_{Gb}, but this depends on whether the junction related bandgap voltage is available as parameter in the particular circuit simulator. Designating the above original voltage as V_D^o, numerical problems due to negative values at (very) high temperatures are avoided by using the smoothing function

$$\boxed{V_D = V_{D\alpha} + V_T \ln\left[1 + \exp\left(\frac{V_D^o - V_{D\alpha}}{V_T}\right)\right]} \quad \text{with} \quad \boxed{V_{D\alpha} = 0.1V_D(T_0)}. \qquad (2.1.15\text{-}16)$$

In ELDO and SPICE-like simulators, the built-in temperature dependence of the depletion charge parameters is used, which is the same as for the SGPM and so far proved to be sufficiently accurate for silicon-based applications.

The zero-bias junction capacitance can be expressed generally as $C_{j0} \sim V_D^{-z}$ so that its temperature dependence can be directly calculated from that of V_D:

$$C_{j0}(T) = C_{j0}(T_0)\left(\frac{V_D(T_0)}{V_D(T)}\right)^z \quad . \tag{2.1.15-17}$$

The temperature dependence of the depletion charge follows automatically from (2.1.4-1a) by applying the above formulas and assuming that the exponent-factor z does not depend on temperature.

The parameter α_j determining the maximum value of a depletion capacitance at forward bias is (empirically) modified as follows:

$$\alpha_j(T) = \alpha_j(T_0)\frac{V_D(T)}{V_D(T_0)} \quad . \tag{2.1.15-18}$$

As can be seen in Fig. 2.1.15/1, the zero-bias capacitance increases, while the voltage at the maximum and the maximum itself decrease with increasing temperature.

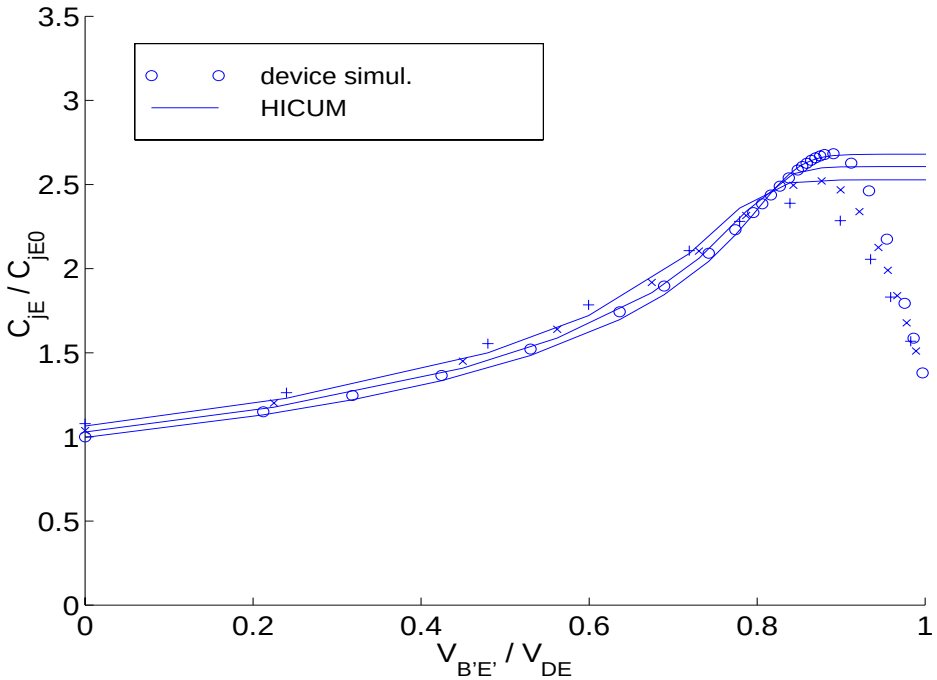


Fig. 2.1.15/1: Temperature dependence of the base-emitter depletion capacitance, normalized to its zero-bias value at 300K, vs. normalized applied voltage: comparison between 1D device simulation (symbols) and model equation (lines). The curves are for the temperatures T/K = 300 (o), 350 (*), 400 (+).

The parameter f_{BC} does not depend on temperature.

2.1.15.5 Series resistances

The internal base resistance depends on temperature mainly via the mobility in the neutral base region, which is contained in the internal base sheet resistance. Thus, the zero-bias resistance is described as

$$r_{Bi0}(T) = r_{Bi0}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{rBi}} \quad . \tag{2.1.15-19}$$

The model parameter ζ_{rBi} is a function of the (average) base doping concentration (cf. $r_{Ci0}(T)$). Conductivity modulation and emitter current crowding in r_{Bi} are automatically described as a function of T by the corresponding charges and currents. The shunt capacitance C_{rBi} is temperature dependent via the capacitances of the internal transistor.

External base resistance r_{Bx}, external collector resistance r_{Cx}, and emitter series resistance follow a similar relationship as r_{Bi0}. This requires the model parameters ζ_{rBx}, ζ_{rCx} and ζ_{rE} which are a function of the (average) doping concentrations within the corresponding regions.

Fig. 2.1.15/2 shows the various types of temperature dependence that can be modelled with the above equation.

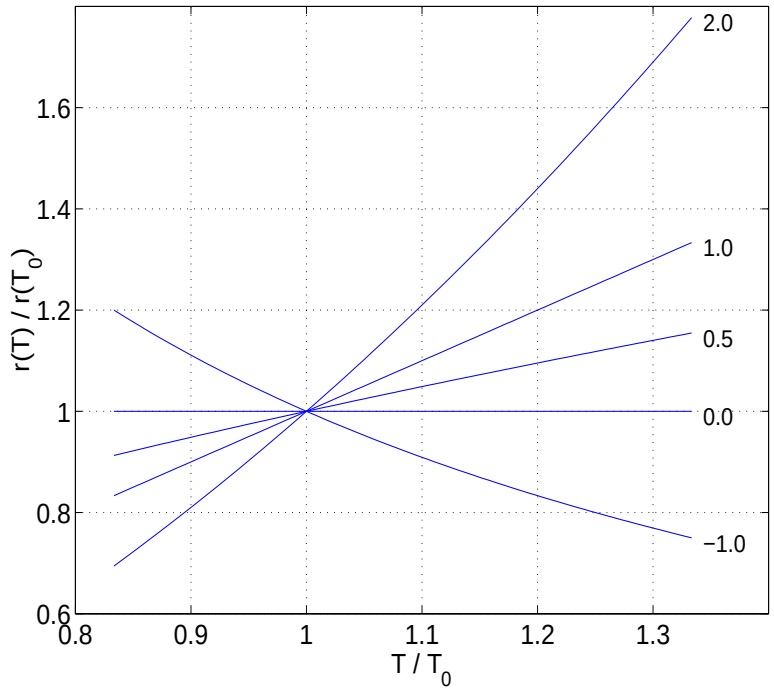


Fig. 2.1.15/2: Normalized resistance as a function of temperature according to eq. (2.1.15-19) for different values of ζ (= ζ_{Ci}, ζ_{rBi}, ζ_{rBx}, ζ_{rCx} or ζ_{rE}) as parameter.

2.1.15.6 Breakdown

A. Base-collector junction (avalanche effect)

The temperature dependence of the coefficients describing avalanche breakdown can be described as [18]

$$a_n(T) = a_n(T_0)\ \exp(\alpha_{na}\,\Delta T)\ , \qquad (2.1.15\text{-}20)$$

$$b_n(T) = b_n(T_0)\ \exp(\alpha_{nb}\,\Delta T) \qquad (2.1.15\text{-}21)$$

with $\Delta T = T - T_0$ and the temperature coefficients α_{na} and α_{nb}. Insertion of these equations into (2.1.10-3,4) gives for the model parameters

$$\boxed{f_{AVL}(T) = f_{AVL}(T_0)\exp(\alpha_{fav}\Delta T)} \quad \text{and} \quad \boxed{q_{AVL}(T) = q_{AVL}(T_0)\exp(\alpha_{qav}\Delta T)} \qquad (2.1.15\text{-}22)$$

with the temperature coefficients $\alpha_{fav} = \alpha_{na} - \alpha_{nb}$ and $\alpha_{qav} = \alpha_{nb}$ which are considered as model parameters. According to a more recent study in [16], the temperature dependence of the parameter

a_n is negligible while only b_n varies slightly with temperature. Therefore, the exp-function reduces to (or can be approximated by) its first series terms, i.e. $\exp(\alpha_{nb}\Delta T) \approx 1 + \alpha_{nb}\Delta T$.

B. Base-emitter junction (tunnelling effect)

The temperature dependence of the parameters describing BE tunnelling is mainly determined by the bandgap's temperature dependence. The saturation current is then given by [39]

$$I_{BEtS}(T) = I_{BEtS}(T_0)\sqrt{\frac{V_G(T_0)}{V_G(T)}}\left(\frac{V_{DEp}(T)}{V_{DEp}(T_0)}\right)^2\frac{C_{jEp0}(T)}{C_{jEp0}(T_0)} \quad . \tag{2.1.15-23}$$

The exponent-coefficient as a function of temperature reads:

$$a_{BEt}(T) = a_{BEt}(T_0)\left(\frac{V_G(T)}{V_G(T_0)}\right)^{3/2}\frac{V_{DEp}(T)}{V_{DEp}(T_0)} \approx a_{BEt}(T_0) \quad . \tag{2.1.15-24}$$

No additional model parameters are required if either the simulator internal band-gap voltage is used or V_G=V_{Gb} is inserted which is a reasonable approximation.

2.1.16 Self-heating

The increase of the transistor's "junction" temperature T_j caused by self-heating is calculated using a thermal network as shown in Fig. 2.1.1/1b. The current source corresponds to the power dissipated in the device, and the node voltage corresponds to the junction temperature. The calculation requires the thermal resistance, R_{th}, and thermal capacitance, C_{th}, (of the particular transistor) as model parameters. The thermal network is solved together with each transistor model (provided $R_{th}>0$) for d.c. and transient operation. The node voltage is passed on to the model routine in order to calculate the temperature dependent model parameters.

The power is calculated from all relevant dissipative elements in the equivalent circuit, excluding any energy storage elements,

$$P = |I_T V_{C'E'}| + \sum |I_{jd} V_{diode}| + |I_{AVL} V_{B'C'}| + \sum \Delta V_n^2 / r_n \qquad (2.1.16\text{-}1)$$

with d={BEp, BCx, BEi, BCi, SC}, V_{diode} as respective diode voltage, r_n as (non-zero) series resistances (n={Bx, E, Cx, Bi}), and ΔV_n as the corresponding voltage drop across those resistances.

Note that only *self*-heating is presently taken into account but not the thermal coupling between different devices on the chip, which is a much more complicated topic and does not directly belong to a transistor model. However, the already existing temperature node of the model can be used for modelling thermal coupling in a circuit.

2.1.17 Lateral scaling

This chapter contains a brief description of the geometry scaling used for HICUM in order to explain the general idea. The scaling formulas - as far as they are bias independent - are implemented in the program TRADICA [42] which is used to generate model parameters for a given transistor configuration (cf. chapter 5). The description of the full set of lateral scaling equations would go beyond the scope of this text. Note, that due to the many different processes the geometry scaling of bipolar transistors is often more complicated than for MOS transistors. However, during TRADICA's use over more than 15 years, a quite general way of geometry scaling has been developed, that has proved to be applicable to a large variety of processes.

2.1.17.1 Transfer current

The geometry dependence of the parameters of the transfer current is given by the proportionalities

$$c_{10} \sim A_E^2 \ , \qquad Q_{p0} \sim A_E \ , \qquad I_{Ch} \sim A_E$$

with A_E as the effective emitter area which is defined in [23, 38].

2.1.17.2 Base current components

The base current components can be split into a bottom and a periphery contribution. For the BE junction, the bottom component is scaled proportional to the effective emitter area. As a consequence, the periphery component has to be corrected by the amount of current already taken into account by widening the emitter to an effective area in order to keep the total BE base current the same.

The base current across the internal base collector junction is scaled with the effective emitter area, while the current across the external BC junction is scaled with the external BC area minus the effective emitter area.

2.1.17.3 Minority charge and transit times

The formulas given in Chapter 2.1.3 for τ_{f0}, $\Delta\tau_{fh}$ and the corresponding charge Q_f were derived from one-dimensional (1D) considerations and can be employed if transistors with a fixed emitter width b_E are used, which is assumed to be much smaller than the emitter length l_E. However, for

narrow or short emitter stripes, 2D and 3D effects occur that will result in less physical values for some of the parameters (such as r_{Ci0}) as well as in different "shapes" of the bias dependence of the transit time. Furthermore, if variable emitter widths and lengths down to the minimum allowed dimensions have to be modelled, the 1D equations would require a different set of model parameters for every size or at least for a certain set of sizes ("binning"). As a consequence, a scalable transit time model is preferred which is given below [38].

A. Low current densities

The transit time at low current densities can be expressed as a function of emitter dimensions through its model parameter

$$\tau_0 = \tau_{f0i}\frac{1 + (\tau_{f0p}/\tau_{f0i})\gamma_C P_E/A_{E0}}{1 + \gamma_C P_E/A_{E0}} \qquad (2.1.17\text{-}1)$$

with $P_E=P_{E0}+4\gamma_C$ and $A_{E0}=b_{E0}l_{E0}$ (cf. List of Symbols). The transit time τ_{f0i} of the bottom transistor as well as the ratio of the transit time of the peripheral transistor to that of the bottom transistor, τ_{f0p}/τ_{f0i}, are TRADICA input parameters.

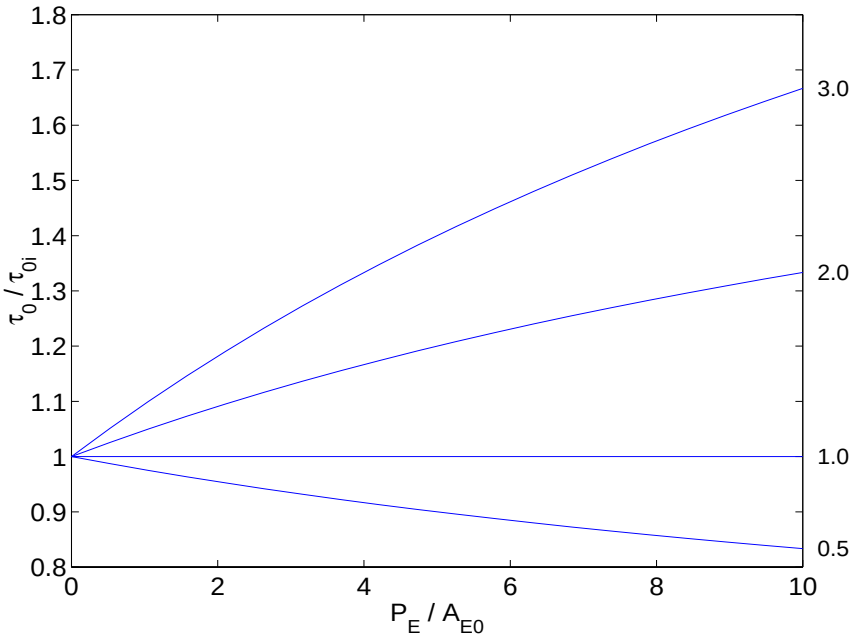


Fig. 2.1.17/1: Normalized low-current transit time as a function of emitter geometry for various ratios of τ_{f0p}/τ_{f0i}. Model parameter used: γ_C=0.05µm.

B. Critical current (density)

Collector current spreading leads to a lower effective current density and, as a result, a larger critical current density than the one scaled by the emitter area only. This can be described by

$$I_{CK} = I_{CK,\,1D}\, f_{cs} \tag{2.1.17-2}$$

with the collector current spreading factor

$$f_{cs} = \begin{cases} \dfrac{\zeta_b - \zeta_l}{\ln[(1+\zeta_b)/(1+\zeta_l)]} & , \quad l_{E0} > b_{E0} \\ 1 + \zeta_b & , \quad l_{E0} = b_{E0} \end{cases} \tag{2.1.17-3}$$

which becomes larger than 1 if current spreading occurs. The new model parameters that also determine the bias dependent lateral scaling (see below) are

$$\zeta_b = 2\frac{w_C}{b_E}\tan\delta_C \qquad \text{and} \qquad \zeta_l = 2\frac{w_C}{l_E}\tan\delta_C \ . \tag{2.1.17-4}$$

They depend on the collector current spreading angle δ_C which is a TRADICA parameter. The corresponding HICUM model parameters names are LATB (= ζ_b) and LATL (= ζ_l). Since the factor f_{cs} can be incorporated into the model parameter r_{Ci0} (cf. eq. (2.1.3-9)), it does not appear as additional parameter for HICUM. Fig. 2.1.17/2 shows the factor f_{cs} as a function of various parameters.

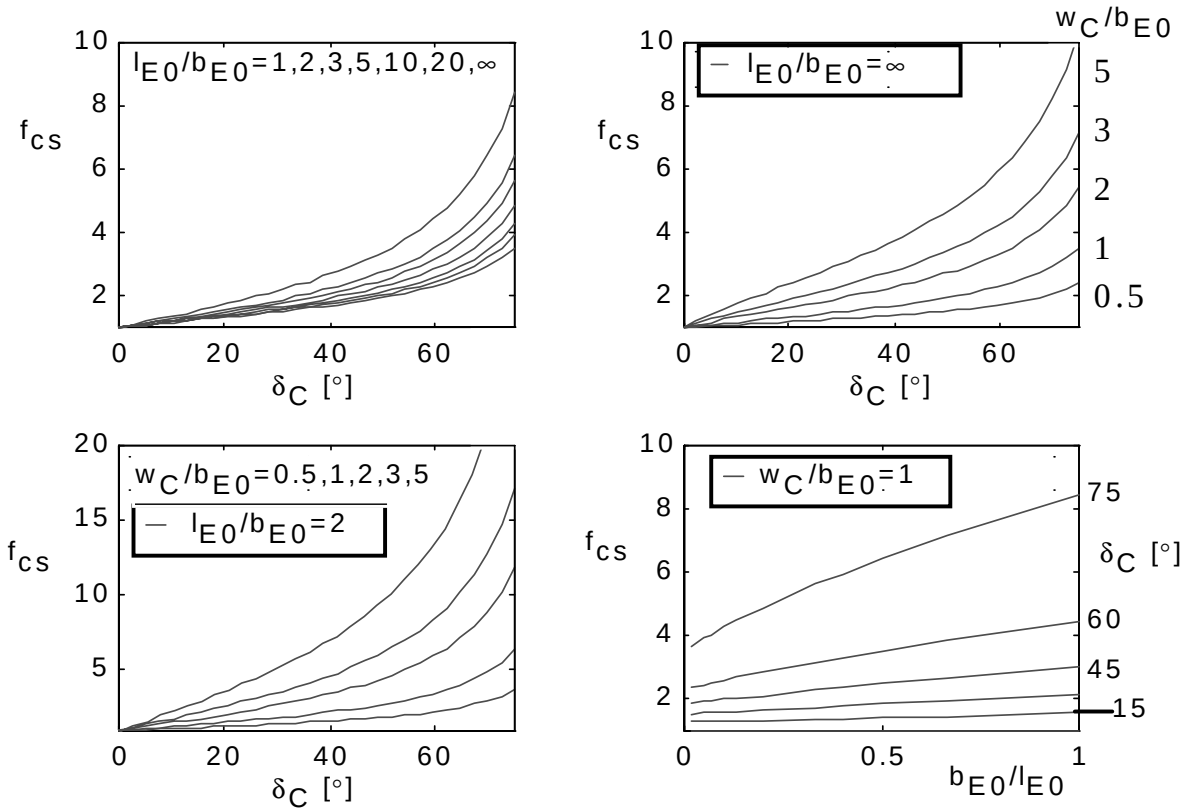


Fig. 2.1.17/2: Collector current spreading factor vs current spreading angle and ratio of emitter width to length, respectively, for a variety of parameters; upper left: emitter aspect ratio variation; upper right: variation of epi to emitter width for a long stripe transistor; lower left: same a before, but for a short transistor; lower right: variation of angle (in degrees).

C. High current densities

If the transistor enters the high-current region, minority charge is stored in the collector within the injection zone w_i which is strongly bias dependent. This width also depends on the collector current spreading angle and can be calculated in normalized from as

$$\frac{w_i}{w_C} = \begin{cases} \dfrac{\kappa - 1}{\zeta_l - \kappa\zeta_b} & , \quad l_{E0} > b_{E0} \\ \dfrac{1}{\zeta_b}\left[\dfrac{1+\zeta_b}{1+i_{ck}\zeta_b} - 1\right] & , \quad l_{E0} = b_{E0} \end{cases} \tag{2.1.17-5}$$

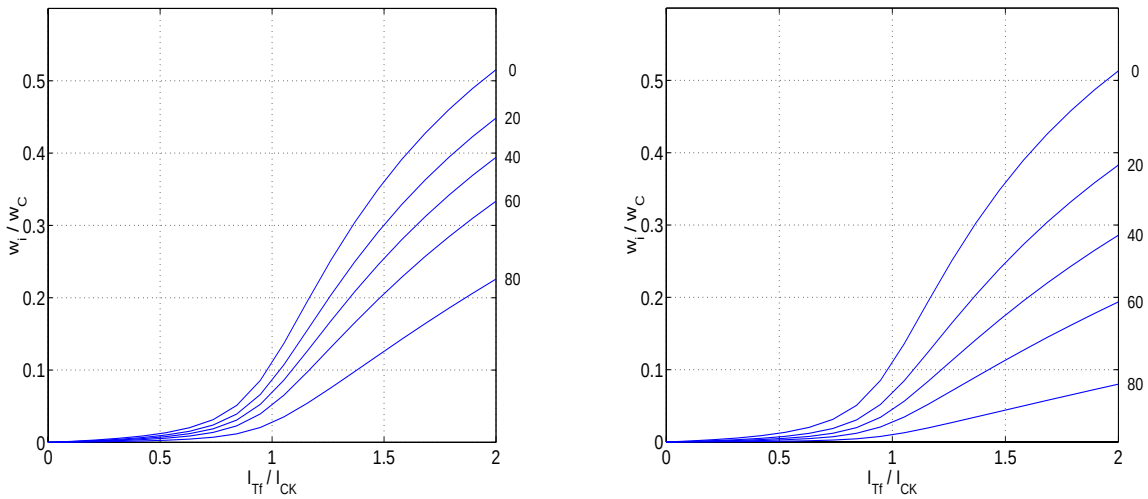
with

$$\kappa = \frac{1+\zeta_l}{1+\zeta_b}\exp\left[i_{ck}\ln\left(\frac{1+\zeta_b}{1+\zeta_l}\right)\right] = \left(\frac{1+\zeta_b}{1+\zeta_l}\right)^{i_{ck}-1} \qquad (2.1.17\text{-}6)$$

and the normalized current

$$i_{ck} = 1 - \frac{i+\sqrt{i^2+a_{hc}}}{1+\sqrt{1+a_{hc}}} \quad \text{with} \quad i = 1 - \frac{I_{CK}}{I_{Tf}} \qquad (2.1.17\text{-}7)$$

Fig. 2.1.17/3 shows the normalized injection width as a function of normalized (forward) collector current with the current spreading angle δ_C as a parameter. δ_C=0 corresponds to the 1D case; with increasing spreading angle, the current density in the collector is reduced and, therefore, the extension of the injection width decreases relative to the 1D case. Compared to long transistors (Fig. (a)), which correspond to the 2D case with $l_E >> b_E$, the impact of current spreading is smaller than for a square-emitter transistor (Fig. (b)), since in the latter current spreading in all four lateral directions becomes significant.



(a) (b)

Fig. 2.1.17/3: Normalized injection width as a function of normalized (forward) collector current for various current spreading angles δ_C: (a) long emitter $l_E >> b_E$; (b) square-emitter $l_E = b_E$. Parameters: $w_C/b_E = 1$, a_{hc}=0.05, $w_C/l_E = 0.01$ for (a) and $w_C/l_E = 1$ for (b).

Also, the equations for τ_{fC} and Q_{fC} have to be extended in order to be able to describe the bias dependence of the occurring 2D and 3D current spreading effects [38]:

$$Q_{Cf} = \tau_{pCS}\, I_{Tf} \begin{cases} 2\,\dfrac{f_{Ci}\ln\left(\dfrac{1+\zeta_b w}{1+\zeta_l w}\right) - f_{Cb} + f_{Cl}}{\zeta_b - \zeta_l} & , \quad l_{E0} > b_{E0} \\ \dfrac{1+\zeta_b w/3}{1+\zeta_b w} w^2 & , \quad l_{E0} = b_{E0} \end{cases} \tag{2.1.17-8}$$

with $\tau_{pCS} = f_{\tau hc}\tau_{hcs}$, and the auxiliary (bias dependent) functions

$$f_{Ci} = w + \frac{\zeta_b + \zeta_l}{2} w^2 + \frac{\zeta_b \zeta_l}{3} w^3 \;, \tag{2.1.17-9}$$

$$f_{Cb} = \frac{1}{\zeta_b}\left(1 - \frac{\zeta_l}{\zeta_b}\right)\left[\frac{x^2[2\ln x - 1] + 1}{4}\right] + \frac{1}{\zeta_b}\frac{\zeta_l}{\zeta_b}\left[\frac{x^3[3\ln x - 1] + 1}{9}\right] \tag{2.1.17-10}$$

with $x = 1 + \zeta_b w$ and

$$f_{Cl} = f_{Cb}(\zeta_b \leftrightarrow \zeta_l) \;, \tag{2.1.17-11}$$

i.e. f_{Cl} has the same form as f_{Cb} but with ζ_b and ζ_l interchanged.

In the implementation of these equations, potential divisions by zero, that could occur for $\zeta_b = 0$ or $\zeta_l = 0$ or $\zeta_b = \zeta_l = 0$ (1D case), have been taken into account by appropriate series expansions, which then also include the 1D theory described before. For the 2D/3D case discussed above, the transit time is calculated numerically

$$\tau_{Cf} = \frac{dQ_{Cf}}{dI_{Tf}} . \tag{2.1.17-12}$$

The base charge component at high current densities, ΔQ_{Bf}, is still calculated without current spreading, using the saturation storage time $\tau_{BfvS} = \tau_{hcs}(1\text{-}f_{\tau hc})$ and the analytical expression of the corresponding transit time $\Delta\tau_{Bf}$.

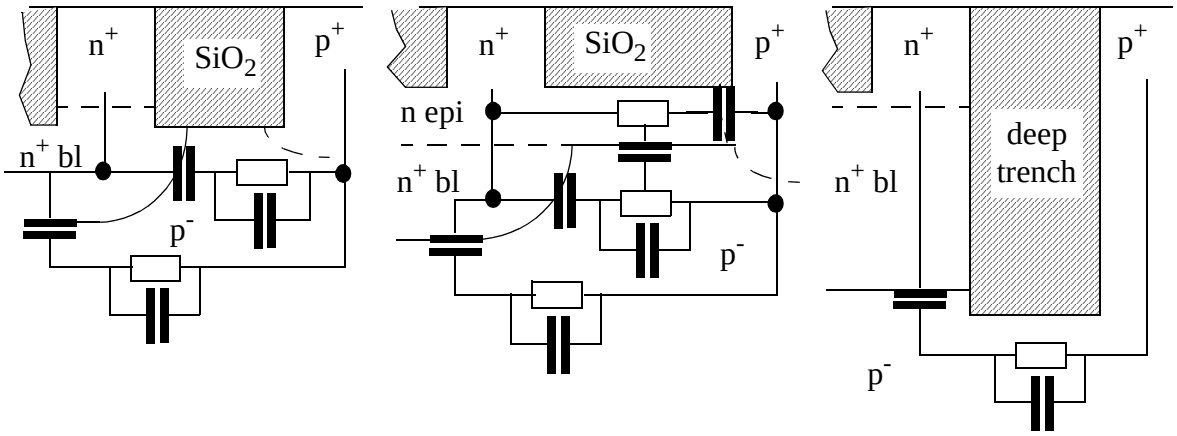
2.1.17.4 Depletion charges and capacitances

Internal capacitances and charges are scaled with the effective emitter area.

Scaling of external capacitances and charges depends on their physical origin:

- The geometry dependent peripheral BE depletion capacitance is calculated from the difference between the total and “effective” internal BE capacitance.
- The various components of the external BC depletion capacitance are calculated from the corresponding capacitance per area or perimeter (“specific” values) times the respective area or perimeter, with the latter one including corner contributions as well.
- The CS capacitance components are calculated from their respective specific values and the buried layer bottom area as well as from the dimensions of the peripheral substrate junction. Fig. 2.1.17/4 shows the various components that contribute to the peripheral CS depletion capacitance of a junction isolated bipolar transistor.

Also, BC and CS capacitance values can be predicted by TRADICA based on collector doping and specific substrate resistance.



thick (field) oxide | thin (field) oxide / shallow trench | deep trench

Fig. 2.1.17/4: Process variants of the CS junction, including components for modelling the depletion capacitance and intra-device substrate coupling.

2.1.17.5 Series resistances

The series resistances of a bipolar transistor depend strongly on geometry and contact configuration of the respective transistor. The geometry scaling of the internal and external base resistance

is described in [26, 33, 34]. The model parameter f_{geo} occurring in the current crowding factor is given by

$$f_{geo} = \frac{1}{g_i \, g_\eta} \tag{2.1.17-13}$$

in which the geometry functions

$$g_\eta = 18.3 - \left[12.2\frac{b_E}{l_E} - 19.6\left(\frac{b_E}{l_E}\right)^2\right] \quad \text{and} \quad g_i = \frac{1}{12} - \left(\frac{1}{12} - \frac{1}{28.6}\right)\frac{b_E}{l_E} \tag{2.1.17-14}$$

depend on the emitter dimensions only and describe a smooth transition from long to short emitter windows.

The external series resistances r_E and r_{Cx} can be calculated by TRADICA from specific resistances, sheet resistances and design rules, taking into account various transistor configurations. This method, which allows an independent determination of series resistances, is believed to be more accurate and flexible than ("direct") extraction from measurements since reliable methods for measuring these resistances do not exist. Most measurement methods are either applicable to a particular process, a certain bias range, or a certain transistor operation (d.c. or small-signal), and validity limits are often unknown or difficult to assess.

2.1.17.6 Breakdown

The avalanche effect formulation contains only q_{AVL} as directly area dependent parameter, besides variables such as transfer current and internal BC capacitance, the scaling of which is already being taken care of.

Under the assumption that in a modern bipolar transistor tunnelling occurs at the emitter periphery junction, the geometry dependence is given by the perimeter P_E of the emitter.

2.1.17.7 Parasitic substrate transistor

Since it is assumed that for most bipolar processes the substrate transistor is determined by its peripheral component, all current related parameters are presently scaled by the CS perimeter

length. The CS depletion capacitance was already discussed before. The transit time scales vertically with the distance between the epi-substrate and the BC junction.

2.1.17.8 Self-heating

Presently, R_{th} and C_{th} are scaled as follows with the effective emitter dimensions,

$$R_{th} = r_{th}\, f_{th} \qquad \text{and} \qquad C_{th} = c_{th} / f_{th} \quad , \tag{2.1.17-15}$$

with the geometry function [11]

$$f_{th} = \frac{\ln(4 l_E / b_E)}{l_E} \quad . \tag{2.1.17-16}$$

r_{th} and c_{th} are TRADICA parameters, that are defined for a *reference* structure with $b_{E,ref}$ and $l_{E,ref}$. This scaling rule is certainly a rough approximation and has to be verified for a given processes.

Fig. 2.1.17/5 shows the dependence of the thermal resistance on emitter width for constant emitter length. The variation is quite small and could also be described by a simple linear function. More measurement results are needed to establish a reliable geometry scaling rule for the thermal elements.

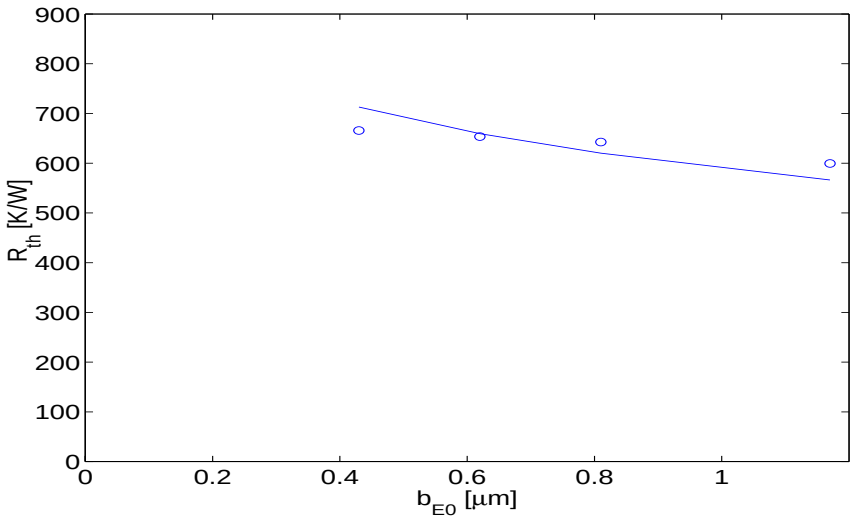


Fig. 2.1.17/5: Thermal resistance as a function of emitter width at constant emitter length: comparison between measurements (symbols) and analytical equation (line).

2.2 HICUM/Level0

Model not available yet.

3 Parameters

This chapter contains a reference list of model parameters with a brief description. The provided default values should be used for model implementation in a circuit simulator; with these values, all but the absolutely necessary functions, that define a bipolar transistor, are turned off. This way, the user only needs to specify the parameters for those effects that are desired to be taken into account. In addition to the default values, a second set of parameter values is provided for exercising the model with most of the physical effects being turned on. This set can be used for, e.g. model testing.

Finally, in the most right column, a multiplication factor is given, which represents the scaling of the respective parameter in case of M identical devices connected in parallel. Note though, that this scaling becomes inaccurate at high frequencies due to the missing interconnect elements that need to be accounted for separately for such device structures.

3.1 Parameter list for HICUM/Level2

Conventionally, the complete set of model parameters has to be specified by a so-called ".model card". The corresponding list of parameters is given in Section I below and is supposed to be available in all (commercial) implementations of the model. From a designer's point of view, however, it is more convenient and flexible to specify just the transistor configuration, defined by emitter width and length as well as number of stripes or contacts. A suggestion for such a (much shorter) list of parameters is given in Section II.

I. Conventional parameter list

The following list is divided into groups of parameters according to the elements in the HICUM equivalent circuit shown in Fig. 2.1.1/1 as well as those for additional physical effects such as noise and temperature dependence. Although the total number of model parameters appears to be large, less time and effort needs to be spent for model parameter extraction - assuming the same physical effects are considered as in the SGPM - due to (a) the physical nature and modularity of the model formulation and (b) the reliable and clearly defined extraction procedure. Note, that not every parameter always needs to be specified for a particular process or application in order to achieve the required accuracy. For example, certain parameters are related to HBTs only and, therefore, can be left at their default values for homojunction transistors.

Many HICUM parameters have been chosen as simple factors, that are related to physically meaningful basic parameters like a capacitance, charge or transit time. This choice significantly reduces changes (and the probability of errors) in the parameter list if the basic parameters are changed for, e.g., statistical simulation, because the factors often assume very similar values even for different process technologies.

Input for the factor M in the last column is interpreted as follows: multiplication of the parameter value is indicated by M while division is indicated by 1/M and no reaction by leaving the entry blank. Caution is required if the factor is applied to r_{su}, C_{su}, R_{th} and C_{th}, in which no interaction between parallel devices is assumed.

As reference temperature, 27C has been chosen to remain compatible with other simulators and models. The value for “∞“ may be dependent on the simulator system. Therefore, the user is referred to the manual of the respective simulator.

3.1.1 Transfer current

no	name	description	default	test	unit	factor
1	**IS (C10)**	Saturation current (GICCR constant) (C10=IS*QP0)	1E-16 (2E-30)	1.35E-18 (3.76e-32)	A (AC)	M (M^2)
2	**QP0**	Zero-bias hole charge	2E-14	2.78e-14	C	M
3	**ICH**	High-current correction for 2D and 3D effects	∞	2.09e-02	A	M
4	**HFE**	Emitter minority charge weighting factor in HBTs	1	1.0	-	
5	**HFC**	Collector minority charge weighting factor in HBTs	1	1.0	-	
6	**HJEI**	B-E depletion charge weighting factor in HBTs	1	1.0	-	
7	**HJCI**	B-C depletion charge weighting factor in HBTs	1	1.0	-	

3.1.2 Base-Emitter Currents

no	name	description	default	test	unit	factor
1	**IBEIS**	Internal B-E saturation current	1E-18	1.16e-20	A	M
2	**MBEI**	Internal B-E current ideality factor	1	1.0150	-	
3	**IREIS**	Internal B-E recombination saturation current	0	1.16e-16	A	M
4	**MREI**	Internal B-E recombination current ideality factor	2	2.0	-	
5	**IBEPS**	Peripheral B-E saturation current	0	3.72e-21	A	M
6	**MBEP**	Peripheral B-E current ideality factor	1	1.0150	-	
7	**IREPS**	Peripheral B-E recombination saturation current	0	1.0e-30	A	M
8	**MREP**	Peripheral B-E recombination current ideality factor	2	2.0	-	

3.1.3 Base-Collector Currents

no	name	description	default	test	unit	factor
1	**IBCIS**	Internal B-C saturation current	1E-16	1.16e-20	A	M
2	**MBCI**	Internal B-C current ideality factor	1	1.0150	-	
3	**IBCXS**	External B-C saturation current	0	4.39e-20	A	M
4	**MBCX**	External B-C current ideality factor	1	1.03	-	

3.1.4 Base-Emitter Tunnelling Current

no	name	description	default	test	unit	factor
1	**IBETS**	B-E tunnelling saturation current	0	0.0	A	M
2	**ABET**	Exponent factor for tunnelling current	40	40	-	

3.1.5 Base-Collector Avalanche Current

no	name	description	default	test	unit	factor
1	**FAVL**	Avalanche current factor	0	1.186	1/V	
2	**QAVL**	Exponent factor for avalanche current	0	11.1e-5	C	M

3.1.6 Series Resistances

no	name	description	default	test	unit	factor
1	**RBI0**	Zero-bias internal base resistance	0	71.76	Ω	1/M
2	**RBX**	External base series resistance	0	8.83	Ω	1/M
3	**FGEO**	Factor for geometry dependence of emitter current crowding	0.6557	0.73	-	
4	**FDQR0**	Correction factor for modulation by B-E and B-C Space charge layer	0	0.2	-	
5	**FCRBI**	Ratio of HF shunt to total internal capacitance	0	0.0	-	

no	name	description	default	test	unit	factor
6	**FQI**	Ratio of internal to total minority charge	1.0	0.9055	-	
7	**RE**	Emitter series resistance	0	12.534	Ω	1/M
8	**RCX**	External collector series resistance	0	9.165	Ω	1/M

3.1.7 Substrate Transistor

no	name	description	default	test	unit	factor
1	**ITSS**	Saturation current of substrate transistor transfer current	0	1.0e-16	A	M
2	**MSF**	Forward ideality factor of substrate transfer current	1	1.05	-	
3	**MSR**	Reverse ideality factor of substrate transfer current	1		-	
4	**ISCS**	Saturation current of C-S diode	0	1e-17	A	M
5	**MSC**	Ideality factor of C-S diode	1	1.0	-	
6	**TSF**	Transit time (forward operation)	0	1.05	s	

3.1.8 Intra-Device substrate coupling

Note: using the M factor is dangerous in this case, unless the transistor cell is exactly replicated and no coupling exists between cells.

no	name	description	default	test	unit	factor
1	**RSU**	Substrate series resistance	0	0	Ω	1/M
2	**CSU**	Shunt capacitance (caused by substrate permittivity)	0	0	F	M

3.1.9 Depletion Capacitances

no	name	description	default	test	unit	factor
1	**CJEI0**	Internal B-E zero-bias depletion capacitance	0	8.11e-15	F	M
2	**VDEI**	Internal B-E built-in potential	0.9	0.95	V	
3	**ZEI**	Internal B-E grading coefficient	0.5	0.5	-	
4	**ALJEI**	Ratio of maximum to zero-bias value of internal B-E capacitance	2.5	1.8	-	
5	**CJEP0**	Peripheral B-E zero-bias depletion capacitance	0	2.07e-15	F	M
6	**VDEP**	Peripheral B-E built-in potential	0.9	1.05	V	
7	**ZEP**	Peripheral B-E grading coefficient	0.5	0.4	-	
8	**ALJEP**	Ratio of maximum to zero-bias value of peripheral B-E capacitance	2.5	2.4	-	
9	**CJCI0**	Internal B-C zero-bias depletion capacitance	0	1.16e-15	F	M
10	**VDCI**	Internal B-C built-in potential	0.7	0.8	V	
11	**ZCI**	Internal B-C grading coefficient	0.4	0.333	-	
12	**VPTCI**	Internal B-C punch-through voltage	∞	416	V	
13	**CJCX0**	External B-C zero-bias depletion capacitance	0	5.4e-15	F	M
14	**VDCX**	External B-C built-in potential	0.7	0.700	V	
15	**ZCX**	External B-C grading coefficient	0.4	0.333	-	
16	**VPTCX**	External B-C punch-through voltage	∞	100	V	
17	**FBC**	Partitioning factor for external B-C capacitance	0	0.1526	-	
18	**CJS0**	C-S zero-bias depletion capacitance	0	3.64e-14	F	M
19	**VDS**	C-S built-in potential	0.6	0.6	V	
20	**ZS**	C-S grading coefficient	0.5	0.447	-	
21	**VPTS**	C-S punch-through voltage	∞	1E20	V	

3.1.10 Diffusion Capacitances

no	name	description	default	test	unit	factor
1	**T0**	Low-current forward transit time at VBC=0V	0	4.75e-12	s	
2	**DT0H**	Time constant for base and B-C space charge layer width modulation	0	2.1e-12	s	
3	**TBVL**	Time constant for modelling carrier jam at low VCE	0	4.0e-12	s	
4	**TEF0**	neutral emitter storage time	0	1.8e-12	s	
5	**GTFE**	Exponent factor for current dependence of neutral emitter storage time	1	1.4	-	
6	**THCS**	Saturation time constant at high current densities	0	30e-12	s	
7	**ALHC**	Smoothing factor for current dependent of base and collector transit time	0.1	0.75	-	
8	**FTHC**	Partitioning factor for base and collector portion	0	0.6	-	
9	**RCI0**	Internal collector resistance at low electric field	150	127.8	Ω	1/M
10	**VLIM**	Voltage separating ohmic and saturation velocity regime	0.5	0.70	V	
11	**VCES**	Internal C-E saturation voltage	0.1	0.1	V	
12	**VPT**	Collector punch-through voltage	∞	5	V	
13	**TR**	Storage time for inverse operation	0	0	s	

3.1.11 Isolation Capacitances

no	name	description	default	test	unit	factor
1	**CEOX**	B-E isolation capacitance	0	1.13e-15	F	M
2	**CCOX**	B-C overlap capacitance	0	2.97e-15	F	M

3.1.12 Non-Quasi-Static Effects

no	name	description	default	test	unit	factor
1	**ALQF**	Factor for additional delay time of minority charge	0	0.225	-	
2	**ALIT**	Factor for additional delay time of transfer current	0	0.45	-	

3.1.13 Noise

no	name	description	default	test	unit	factor
1	**KF**	Flicker noise coefficient (no unit only for AF=2)	0	1.43e-8	-	M^{1-AF}
2	**AF**	Flicker noise exponent factor	2	2	-	
3	**KRBI**	Factor for internal base resistance	1	1	-	

3.1.14 Lateral Geometry Scaling (at high current densities)

no	name	description	default	test	unit	factor
1	**LATB**	Scaling factor for collector minority charge in direction of emitter width b_E	0	3.765	-	
2	**LATL**	Scaling factor for collector minority charge in direction of emitter length l_E	0	0.342	-	

3.1.15 Temperature Dependence

no	name	description	default	test	unit	factor
1	**VGB**	Bandgap-voltage extrapolated to 0K	1.17	1.17	V	
2	**ALB**	Relative temperature coefficient of forward current gain	5E-3	6.3e-3	1/K	
3	**ALT0**	First-order relative temperature coefficient of parameter T0	0	0	1/K	
4	**KT0**	Second-order relative temperature coefficient of parameter T0	0	0	$1/K^2$	
5	**ZETACI**	Temperature exponent for RCI0	0	1.6	-	
6	**ALVS**	Relative temperature coefficient of saturation drift velocity	0	1e-3	1/K	
7	**ALCES**	Relative temperature coefficient of VCES	0	0.4e-3	1/K	
8	**ZETARBI**	Temperature exponent of internal base resistance	0	0.588	-	
9	**ZETARBX**	Temperature exponent of external base resistance	0	0.206	-	
10	**ZETARCX**	Temperature exponent of external collector resistance	0	0.223	-	
11	**ZETARE**	Temperature exponent of emitter resistance	0	0	-	
12	**ALFAV**	Relative temperature coefficient for FAVL	0	8.25e-5	1/K	
13	**ALQAV**	Relative temperature coefficient for QAVL	0	1.96e-4	1/K	

3.1.16 Self-Heating

no	name	description	default	test	unit	factor
1	**RTH**	Thermal resistance	0	0.0	K/W	1/M
2	**CTH**	Thermal capacitance	0	0.0	Ws/K	M

3.1.17 Circuit simulator specific parameters

The parameter LEVEL, that identifies the HICUM model in a circuit simulator has a different name for each simulator. The parameters TNOM and DT are available in most simulators and are named the same.

no	name	description	default	unit
1	**LEVEL**	Model identifier	9 (ELDO) bht (SPECTRE)	-
2	**TNOM**	temperature at which parameters are specified	27	°C
3	**DT**	Temperature change w.r.t. chip temperature for particular transistor	0	°C

II. Specification of transistor configuration

Rather than having to specify the above list of model parameters, it would be preferable to use only the transistor configuration as input. The table below shows the respective information that needs to be passed on to a program module for geometry scaling to generate the above list of model parameters. TNOM and DT still have to be specified independently.

No	Symbol	Name	description	Default	Unit
1	b_{E0}	bE0	emitter window width	0.5	µm
2	l_{E0}	lE0	emitter window length	10	µm
3	n_E	nE	number of emitter contacts	1	-
4	n_B	nB	number of base contacts	2	-
5	n_C	nC	number of collector contacts	1	-
6		loc	location of collector contact(s)	side	-
7		seq	contact configuration (mostly relevant for distinguishing CEB or CBE configuration)	CBEB	-
8	n_{pas}	npas	number of transistor structures connected in parallel (corresponds to the SPICE M factor)	1	-
	T_{nom}	TNOM	temperature at which process data are valid	27	C
	ΔT	DT	temperature change for particular transistor	0	C

3.2 Parameter list for HICUM/Level0

Not available yet.

4 Parameter determination

HICUM/L2 has been developed to address modeling issues related to the design of *integrated* circuits. In this case, geometry and process information are generally available, that can be used to obtain as much as possible physics-based model parameters. Besides bias, frequency and temperature, the transistor geometry can be considered as an additional independent dimension for parameter extraction the use of which helps avoiding ambiguous values compared to just fitting the terminal characteristics of a *single* device. A discussion of the advantages of the multi-geometry-based parameter extraction recommended for HICUM (and being used in the MOS area for a long time) is given in, e.g., [42]. Therefore, the description below deals with the extracting sequence that is used for generating geometry scalable HICUM parameters. For additional information of the extraction procedure see also [14].

As described in [14], the extracted model parameters for HICUM (and also for the SPICE Gummel-Poon model) are converted into a geometry and layout independent form. These so-called specific data are then used in a special program (TRADICA) to generate model parameters for arbitrary transistor configurations.

For a given process, obtaining compact model parameters of a large variety of transistor configurations, using the recommended process-based scalable approach (PBSA), involves several major steps:

- wafer selection according to certain criteria;
- deriving the relevant transistor dimensions from design rules;
- measurement of the relevant characteristics of a certain set of test structures (incl. transistors) over bias, geometry, temperature and frequency;
- extraction of (geometry) specific model parameters;
- generation of the model parameters for desired transistor configurations (either as library or directly during the circuit design phase).

The various aspects related to the above steps are briefly discussed in this chapter. In addition, an overview on the recommended sequence of parameter extraction is given in a formal way in chapter 4.4 to provide the reader with basic information, such as measurement and data requirements as well as principle procedures employed. Another purpose of this overview is also to serve as a guide line for implementing the parameter extraction methodology.

4.1 Wafer selection

There are many criteria as to which wafer should be selected or which one rejected when it comes to model parameter extraction. Below, those criteria that proved to be useful for the process-based scalable approach pursued here are briefly discussed.

As already mentioned before, the PBSA relaxes the requirements for the wafer selection, since it allows to shift the (specific) parameters later on to their desired nominal values. However, the electrical performance of the transistors (and other parameters) should not be too far off from the target specifications. Also, it is important to evaluate the process regarding geometry scalability, since non-conventional scaling requires larger effort (and time) for parameter extraction. Therefore, before a wafer is accepted for parameter extraction purposes, the following tests are recommended to be performed and evaluated:

- Measurement of a tetrode structure (for each transistor type) at zero bias, yielding roughly the internal base sheet resistance r_{SBi0};
- Measurement of a large area BC diode (i.e. without SIC) at zero bias and beyond punch through, yielding epi doping N_C and thickness w_C;
- Measurement of the bias dependent S-parameters for a typical transistor (each type) at a single CE voltage and frequency, yielding the transit frequency f_T.

The first two measurements can be performed on PCM structures. The third one is more time consuming and can be done after the first two have been evaluated. In general, though, all of the above data are usually available during process development and evaluation.

It is recommended then to obtain a wafer map that shows the uniformity of the electrical parameters r_{SBi0}, w_C, N_C, and f_T. The correlation of the latter to the first three should be checked as well as, of course, the absolute values regarding their deviation with respect to the target values.

Next, an appropriate die for parameter extraction is selected as the centre of the area with the highest uniformity. As a consequence, the chance of deviations in electrical characteristics between different transistors of the selected die is likely to be minimized.

In addition to the electrical tests, it is highly recommended to obtain pictures of the cross-section and top view (SEM and TEM pictures) of the most important transistor configurations for both extractions and applications. These pictures are usually available during process development and not only provide an impression on the actual transistor structure but also serve for verifying the transistor dimensions assumed or calculated from design rules. In the experience of the author, the information obtained from the above pictures can avoid results, that appear to be non-physical, and geometry scaling problems, that cannot be explained otherwise just by electrical measurements.

4.2 Relevant transistor dimensions

Definitions of the relevant transistor dimensions used for calculating the area and perimeter length specific model parameters are given in Fig. 4.2.0/1 for a junction isolated silicon bipolar transistor fabricated in a self-aligning base-emitter process.

.

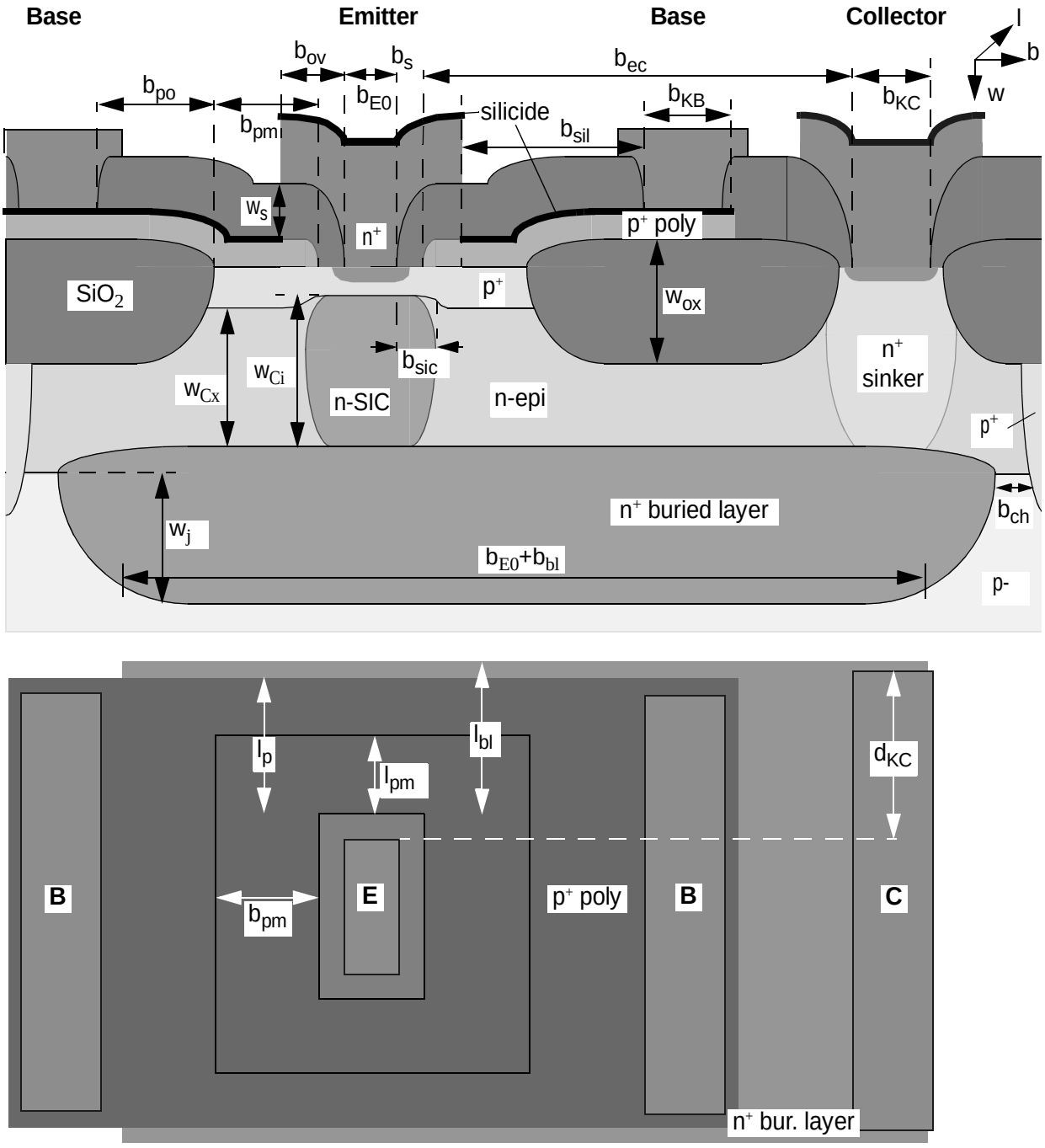


Fig. 4.2.0/1: Schematic cross-section and layout of a silicon bipolar transistor with junction isolation and self-aligned base-emitter formation.

The described parameter extraction procedure can also be applied to silicon epitaxial base transistors, including SiGe transistors. The corresponding schematic cross section and layout with the respective dimensions are shown in Fig. 4.2.0/2.

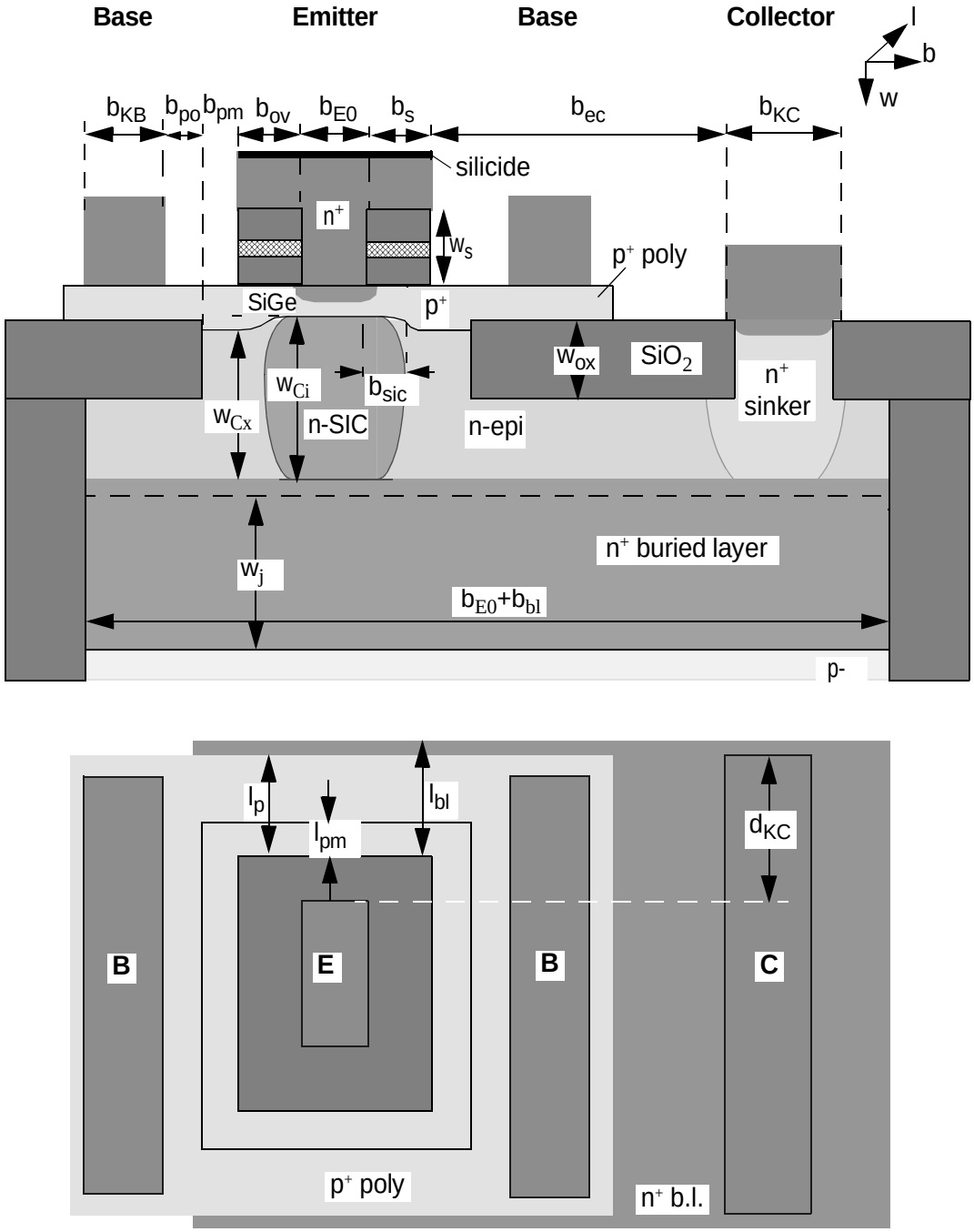


Fig. 4.2.0/2: Schematic cross-section and layout of a epitaxial base SiGe bipolar transistor with shallow and deep trench isolation.

4.3 Measurements

Parameter extraction for the PBSA relies on minimum requirements regarding measurement effort and equipment. While the set-up and detailed bias conditions (test plans) for a particular parameter determination procedure are given in the respective chapters, at this point a brief overview shall be provided on the basic and most important measurement methods, which are being employed for obtaining the data required for a variety of procedures. This chapter also serves for defining the "measurement" and "data" related terminology used throughout this documentation.

The measurements are taken on transistors and special test structures. Examples of the most important test structures suitable for PBSA are given in [14].

4.3.1 IV measurements and data

DC measurements taken, e.g., with a parameter analyser, on test structures and transistors are called IV measurements, resulting in the associated IV data. Examples are

- a forced current in a 3-terminal test structure for determining a sheet resistance and the corresponding measured voltage between the contacts or
- the collector and base current of a transistor as function of the applied voltage.

However, IV data also include the DC bias taken during S-parameter measurements (see below), while IV measurements always means a DC measurement and associated set up as defined above.

4.3.2 CV measurements and data

Capacitances with a sufficient large value can be measured with LCR or CV meters, thus the name CV measurements and CV data. This equipment usually operates at frequencies between 0.1...10 MHz. It is, therefore, only suited for measuring large size capacitances that are laid out as special test structures like in process monitors.

The designation CV data includes capacitance vs. voltage data from both CV measurements, as defined above, and from S-parameter measurements.

4.3.3 S-parameter measurements and data

Small-signal measurements at high frequencies are performed with a vector network analyser (VNA) and are taken as S-parameters, resulting in S-parameter data. Operating frequencies for obtaining accurate data are usually above 300 MHz, with an upper limit usually in the multi-10GHz range, dependent on the respective equipment. For parameter extraction purposes, two types of S-measurement are often distinguished: (a) "cold" measurements during which the transistor is operated at reverse and very low forward bias with negligible carrier injection and current across the junctions; (b) "hot" measurements during which the transistor is operated under usual forward-bias conditions with significant carrier injection and non-negligible current across junction. The corresponding data are designated as, e.g. cold S-parameters or hot Y-parameters.

Although the operating frequencies of high-performance transistors in some of the present Si-based processes already exceed 100GHz, the corresponding parameters for modeling the high-frequency transistor can be determined at frequencies well below 100 GHz under so-called quasi-static conditions. The lower frequency limit for parameter extraction related S-parameter measurements is approximately given by the 3dB corner frequency of the common-emitter (CE) small-signal current gain. At current gains between 50 and 200, this corresponds to the range around 1GHz. One of the most important quasi-static small-signal transistor parameters for extract-

ing model parameters is the transit frequency f_T. It has been shown in [9] that f_T can be obtained from a single frequency measurement of the small-signal CE current gain.

A typical set of data from a single-frequency bias sweep measurement includes the terminal voltages and current as well as the frequency and the four S-parameters in either magnitude and phase or real and imaginary part representation. The S-parameters can then be converted into Y-parameters at the same bias points. Next, the Y-parameters need to be de-embedded in order to eliminate the influence of parasitic elements and obtain the Y-parameters of the device under test only. From the de-embedded Y-parameters as a function of bias, a large number of HICUM model parameters can be extracted.

Generally, the bias dependence of the small-signal behavior and parameters is of great interest for parameter extraction. In many circuit design applications, the dependence of small-signal parameters on the collector current I_C at a given voltage V_{CE} is of major importance. Unfortunately, it is found very often, that S-parameters as a function of frequency are taken for bias points, that are defined by the terminal voltages V_{BE} and V_{CE}, while the terminal currents are not or cannot be monitored; the latter is often caused by, e.g., limitations of the data acquisition software or the equipment. Only with a separate DC measurement the terminal currents are then obtained, and the relationship between S-parameters and bias currents is attempted to be established. The great danger in this procedure is that the devices usually heat up differently (caused by self-heating) during the S-parameter and the pure DC measurement, leading to an incorrect relationship of the above mentioned variables. The consistent way of taking data is to monitor the current or, even better, to define the bias point by the collector current and V_{CE}. For some data acquisition software, the current can be monitored by reducing the small-signal measurements to a single frequency rather than a frequency sweep. Although in this case the "averaging" has to be increased, a somewhat shorter measurement time is often achieved (together with a large reduction in data) as well. Appropriate bias points for frequency sweep measurements can then be selected afterwards.

4.3.4 Sequence of measurements

In a production environment, measurement effort and time have to be minimized. This is done on one hand by using standard and established equipment set-ups and on the other hand by maximizing the equipment utilization in a given time frame.

Data acquisition for model parameter extraction starts at the reference temperature T_0 with simple and fast IV measurements of all special test structures used for determining sheet and contact resistances. Next, CV measurements are performed, followed by single-frequency cold and hot S-parameter measurements. The same device is probed for all bias conditions before moving the probes to the next device. These measurements provide already sufficient information for extracting more than 80% of the (specific) model parameters, the process of which can then start.

In the meantime, i.e. during parameter extraction, data acquisition continues with temperature dependent measurements, which are quite time consuming. By the time the latter measurements are completed, parameter extraction has provided an overview on the process and its actual performance, so that those bias range and points can be determined which are of interest for frequency sweeps. Frequency sweep measurements are usually required and taken only at the reference temperature. Based on the temperature and frequency dependent data, the remaining model parameters (except those for low-frequency 1/f noise) can be extracted, and model verification can already start.

Finally, special measurements, such as those for noise and distortion, can be performed at T_0.

4.4 A step by step procedure

The goal of this chapter is to give a "formal" overview on the sequence for extracting geometry scalable HICUM parameters. To keep this overview efficient, for each step only a brief description of the applied extraction procedure is provided, while for a detailed description (incl. equations) and the origin of the respective procedure, the reader is referred to one of the subsequent chapters of this documentation. One important boundary condition for developing HICUM was to enable a parameter extraction procedure in which as many as possible steps can be performed linearly independently or with only a weak interdependence, particularly for determining parameters describing first-order effects.

In modern bipolar technologies, often at least two types of transistors are offered: a high-performance (HP) transistor and a high-voltage (HV) transistor, that are defined by same process flow and with just one additional mask. The HP transistor is usually realized with a selectively implanted collector (SIC). It is recommended to extract first the parameters of the HV transistors and then the parameters of the HP transistors, since the HV transistor's collector is typically realized with the background doping that is also present under the external base of the HP device. If HV transistors are not available, those ones required for extraction can usually be easily realized and should be included on a test chip. If parameters for a HV transistor without SIC have to be extracted, no respective HP device is needed.

A couple of assumptions are being made in order to apply the procedures in practice:

- A suitable wafer with the appropriate test structures and transistors has been selected that has passed the recommended acceptance check mentioned in chapter 4.1.
- All measurements that are required for a particular extraction step are available and have been properly de-embedded. It is generally preferable to convert S-parameters to Y-parameters (to be done during de-embedding in any way) and use the latter data for parameter extraction.
- The design rules and dimensions of all test structures and transistors are known and have been verified, so that all necessary geometry calculations can be performed.
- The process is geometry scalable, i.e. the profile under the emitter does not depend on the emitter width. This can be checked by measuring the internal base sheet resistance as a function of emitter width (cf. [27,14]).

The information about each extraction step is contained in a small table. The meaning of the key words on the right-hand-side and the terminology used shall be briefly explained below.

- "Measurement data" characterizes the type of data required for the particular step. Acronyms such as CV, IV or cold measurements have already been defined in chapter 4.3.
- "Required model parameters" specify those ones that had to be extracted in an earlier step and are needed for the present step. They do not include dimensions, which are specified under "required geometry data".
- "Procedure" refers to the chapter where the extraction procedure and its background is described in more detail. Just a brief outline of the recommended method(s) is given under "quick info".
- Under "Extracted specific parameters" those parameters are listed that are geometry independent. These parameters are used in the program TRADICA to generate geometry scal-

able libraries for model parameters. Of course, certain HICUM parameters, such as ratios, are geometry independent in the first place and do not need to be scaled with geometry. However, since it is useful to determined a full set of (geometry) specific parameters first and keep the data in one place before subsequent parameter (library) generation, all extracted parameters are listed here.

- "Related HICUM parameters" are those that eventually occur in a library (model card) and are generated for a particular transistor configuration, employing a program like TRADICA.

Below, the extraction sequence is outlined. Linearly independent steps are indicated by the entry "none" under "Required model parameters".

4.4.1 BC depletion and isolation capacitance

Measurement data	• cold Y-parameters of different transistor configurations • CV data of large area HV structure (optional) • CV data of large area HP structure
Required model parameters	none (optional: C_{Cox} calculated from TRADICA for each transistor configuration)
Required geometry data	• area A_{BC} and perimeter P_{BC} of BC junction (HV transistor) • area A_{SIC} of SIC region (HP transistor)
Procedure:	• HV data: separation into bias dependent bottom and perimeter specific components of the depletion capacitance via different geometries; also, determination of specific isolation capacitance possible. • Extraction of parameters for modeling the bias dependence of above depletion capacitances. • HP CV data: extraction of SIC related parameters.
Extracted (specific) parameters	• HV data: $\overline{C}_{jCb0}$, V_{DCb}, z_{Cb}, V_{PTCb}; C'_{jCp0}, V_{DCp}, z_{Cp}, V_{PTCp}, $[C'_{Cox}]$ • HP data: $\overline{C}_{jCi0}$, V_{DCi}, z_{Ci},V_{PTCi}
Related HICUM parameters	C_{jCx0}, V_{DCx}, z_{Cx}, V_{PTCx}, C_{Cox}, f_{BC}; C_{jCi0}, V_{DCi}, z_{Ci},V_{PTCi}

4.4.2 BE depletion and isolation capacitance

Measurement data and test structures	• cold and hot Y-parameters of different transistor configurations • CV data of large area structure (optional)
Required model parameters	none (optional: C_{Eox} calculated from TRADICA for each transistor configuration)
Required geometry data	area A_{E0} and perimeter P_{E0} of emitter window
Procedure:	• Determination of C_{BE} from $1/(2\pi f_T)$ at a forward bias point. • Separation into bias dependent bottom and perimeter specific components of the depletion capacitance via different geometries; also, determination of specific isolation capacitance possible. • Extraction of parameters for modeling the bias dependence of above depletion capacitances
Extracted (specific) parameters	$\overline{C}_{jEi0}$, V_{DEi}, z_{Ei}, a_{jEi}; C'_{jEp0}, V_{DEp}, z_{Ep}, a_{jEp}, [C'_{Eox}]
Related HICUM parameters	C_{jEi0}, V_{DEi}, z_{Ei}, a_{jEi}; C_{jEp0}, V_{DEp}, z_{Ep}, a_{jEp}; C_{Eox}

4.4.3 CS depletion capacitance

Measurement data and test structures	• cold Y-parameters of different transistor configurations • CV data of large area structure (optional, but recommended)
Required model parameters	none
Required geometry data	area A_{CS} and perimeter P_{CS} of CS junction
Procedure:	• Separation into bias dependent bottom and perimeter specific components of the depletion capacitance via different geometries. • Extraction of parameters for modeling the bias dependence of above depletion capacitances.
Extracted (specific) parameters	$\overline{C}_{jSb0}$, V_{DSb}, z_{Sb}, V_{PTSb}; C'_{jSp0}, V_{DSp}, z_{Sp}, V_{PTSp}
Related HICUM parameters	C_{jS0}, V_{DS}, z_S, V_{PTS}

4.4.4 Internal base (sheet) resistance

Measurement data	IV data on transistor tetrodes with different emitter widths: • sweep of $V_{BE} = V_{BC}$ ($V_{CE} = 0$) • sweep of V_{BE} @ $V_{BC} = 0$
Required model parameters	C_{jEi0}, V_{DEi}, z_{Ei}; C_{jCi0}, V_{DCi}, z_{Ci} (or numerical integration of associated depletion charges)
Required geometry data	width b_{E0} and length l_{E0} of emitter windows
Procedure:	• Determine internal base sheet resistance $r_{SBi}(V_{BE},V_{BC})$ from corrected data. • Extraction of parameters for modeling the bias dependence of r_{SBi}. • Determination of the link and total external resistance (used for next step)
Extracted (specific) parameters	r_{SBi0}, $\overline{Q}_{p0}$, f_{dQr}, r_{Ss}
Related HICUM parameters	r_{Bi0}, Q_{p0}, f_{dQr}

Note, that the model parameter f_{geo} can be (and has been) directly calculated from the transistor configuration.

4.4.5 Components of external base resistance

Measurement data	• IV data of various resistance test structures • link and total external resistance from transistor tetrodes
Required model parameters	None
Required geometry data	dimensions of the relevant regions of the test structures
Procedure:	• Determine resistance(s) from IV data and perform current spreading correction (depending on resistance type). • Extract sheet or specific contact resistance from each structure
Extracted (specific) parameters	ρ_{KB}, r_{Spo}, r_{Spm}, r_{Ssil}
Related HICUM parameter	r_{Bx}

For single device extraction, this module has to be replaced by a procedure for extracting r_{Bx}.

4.4.6 Emitter resistance

Measurement data	open collector IV data from transistor structures with different emitter size
Required model parameters	None
Required geometry data	total emitter window width A_{E0} of each transistor
Procedure:	• for each transistor: fit modified open-collector model equation to measured data • extract specific contact resistance from $r_E(1/A_{E0})$
Extracted (specific) parameter	ρ_{KE}
Related HICUM parameter	r_E

4.4.7 Components of external collector resistance

Measurement data	IV data of special resistance test structure
Required model parameters	None
Required geometry data	dimensions of the relevant regions of the test structure
Procedure:	• Determine resistance from IV data and perform current spreading correction (if required). • Extract buried layer sheet and specific contact plus sinker resistance
Extracted (specific) parameters	ρ_{KC}, r_{Sbl}
Related HICUM parameter	r_{Cx}

4.4.8 Collector current at low bias

Measurement data	IV data from transistors with different emitter size
Required model parameters	most processes: C_{jEi0}, V_{DEi}, z_{Ei}, a_{jEi} (not for "real" HBTs) optional: Q_{p0}; [C_{jCi0}, V_{DCi}, z_{Ci}, if V_{CE} = const)
Required geometry data	emitter window area of the transistors
Procedure:	• Separation into bias dependent bottom and perimeter specific current components via different geometries. • Extraction of parameters related to bias dependence from least-squares fit of $\log(I_C/A_E)$ vs. V_{BE} @ V_{BC}=0 (procedure is partially dependent on process):
Extracted (specific) parameters	γ_C, $\overline{I}_S$, [$\overline{Q}_{p0}$, m_{Cf}]
Related HICUM parameters	I_S (or c_{10}), [Q_{p0}, m_{Cf}]

4.4.9 Current across BE junction at low bias

Measurement data	IV data from transistors with different emitter size
Required model parameters	none
Required geometry data	emitter window area of the transistors
Procedure:	• Separation into bias dependent bottom and perimeter specific current components via different geometries. • Extraction of saturation current (density) and non-ideality coefficient of each component from least-squares fit of log(I) vs. V_{BE} @ V_{BC}=0
Extracted (specific) parameters	γ_B; $\overline{I}_{BEiS}$, m_{BEi}, I'_{BEpS}, m_{BEp}; $\overline{I}_{REiS}$, m_{REi}, I'_{REpS}, m_{REp}
Related HICUM parameters	I_{BEiS}, m_{BEi}, I_{BEpS}, m_{BEp}; I_{REiS}, m_{REi}, I_{REpS}, m_{REp}

4.4.10 Current across BC junction at low bias

Measurement data	IV data from transistors with different size
Required model parameters	none
Required geometry data	collector-base junction area A_{BC} and emitter window area A_{E0} of the transistors
Procedure:	• Separation into bias dependent bottom and perimeter specific current components via different geometries. • Extraction of saturation current (density) and non-ideality coefficient for each component from least-squares fit of log(I) vs. V_{BC} @ V_{BE}=0
Extracted (specific) parameters	$\overline{I}_{BCxS}$, m_{BCx}; $\overline{I}_{BCiS}$, m_{BCi}
Related HICUM parameters	I_{BCxS}, m_{BCx}; I_{BCiS}, m_{BCi}

4.4.11 Thermal resistance

Measurement data	IV data of transistors used for extraction
Required model parameters	r_E, r_{Bx}, r_{Bi}
Required geometry data	emitter window area A_{E0} of the transistors
Procedure:	• Extraction of R_{th} of each transistor from I_B as a function of dissipated power according to [48], but with known r_E.
Extracted (specific) parameter	r_{th}
Related HICUM parameter	R_{th}

4.4.12 Forward transit time

Measurement data	hot Y-parameters of different transistor configurations
Required model parameters	C_{jCi0}, V_{DCi}, z_{Ci},V_{PTCi}; C_{jCx0}, V_{DCx}, z_{Cx}, V_{PTCx}, C_{Cox}; r_E, r_{Cx}; γ_C; [R_{th}]
Required geometry data	emitter window dimensions b_{E0} and l_{E0} of the transistors

Procedure:	• Determine transit frequency f_T from Y-parameters and determine transit time τ_f from $1/(2\pi f_T)$ vs $1/I_C$.
	• Low-current range:
	  • From $\tau_{f0}(V_{BC})$ data, extract parameters describing the bias dependence.
	  • Determine bottom and perimeter related component and associated geometry factor from $\tau_{f0}(V_{BC}=0)$ of transistors with different emitter size.
	• Medium current range
	  • From $I_{CK}(V_{CE}$ or $V_{BC})$ data, extract parameters describing the bias dependence
	  • Extract current spreading angle from $I_{CK}(V_{CE}=0.8V$ or $V_{BC}=0V)$
	• High-current region: extract relevant parameters describing the bias dependence.

Extracted (specific) parameters	τ_{f0i}, $f_{tpi} = \tau_{f0p}/\tau_{f0i}$, $\Delta\tau_{0h}$, τ_{Bfvl}; $\overline{r_{Ci0}}$, V_{lim}, V_{PT}, V_{CEs}; a_{hc}, τ_{hcs}, τ_{Ef0}, $g_{\tau E}$, $f_{\tau hc}$
Related HICUM parameters	τ_0, $\Delta\tau_{0h}$, τ_{Bfvl}; r_{Ci0}, V_{lim}, V_{PT}, V_{CEs}; a_{hc}, τ_{hcs}, τ_{Ef0}, $g_{\tau E}$, $f_{\tau hc}$

4.4.13 Collector current at high injection

Measurement data	IV data from transistors with different emitter size
Required model parameters	• those for I_T and I_{BE} extracted at low injection • depletion capacitances and transit time (to calculate $Q_{p,T}$) • r_E, r_{Bx}, r_{Bi}, r_{Cx} • R_{th}
Required geometry data	emitter window area of the transistors
Procedure:	• Extraction in high current region via non-linear optimization of $\log(I_C/A_E)$ vs. V_{BE} at sufficiently low V_{CE} (to minimize impact of self-heating). • Optimization can be performed simultaneously on transistors with different emitter sizes.
Extracted (specific) parameter	$\overline{I_{Ch}}$
Related HICUM parameter	I_{Ch}

4.4.14 Base-collector Breakdown

Measurement data	$I_B(V_{CB}$ or $V_{CE})$ data from transistors with different size
Required model parameters	C_{jCi0}, V_{DCi}, z_{Ci},V_{PTCi}; γ_C
Required geometry data	emitter window area A_{E0} of the transistors
Procedure:	• Determination of avalanche current $I_{AVL}(V_{CB})$ from measured $I_B(V_{CB})$ data at sufficiently low forward bias V_{BE}. • Extraction of parameters describing the bias dependence via non-linear optimization of $I_{AVL}(V_{CB})$.
Extracted (specific) parameters	f_{AVL}, $\bar{q}_{AVL}$
Related HICUM parameters	f_{AVL}, q_{AVL}

4.4.15 High-Frequency effects

4.4.15.1 Non-quasi-static effects

Measurement data	hot Y-parameters of a typical transistor configuration
Required model parameters	• those for I_T and I_{BE} extracted at low injection • all capacitances and transit time • r_E, r_{Bx}, r_{Bi}, r_{Cx}
Required geometry data	None
Procedure:	• Extraction of α_{iT} by fitting $Im\{y_{21}\}$at high frequencies for various bias points below peak f_T. • Extraction of α_{Qf} by fitting $Re\{y_{11}\}$at high frequencies for various bias points beyond peak f_T.
Extracted (specific) parameters	α_{iT}, α_{Qf}
Related HICUM parameters	α_{iT}, α_{Qf}

4.4.15.2 Partitioning of the external BC capacitance

Measurement data	None
Required model parameters	specific BC capacitances and sheet/contact resistances of the external base
Required geometry data	dimensions of the various regions of the external base
Procedure:	Calculation of the partitioning factor by TRADICA for each geometry during parameter (library) generation
Extracted (specific) parameter	
Related HICUM parameter	f_{BC}

Presently existing methods, that are based on experimental data, only allow to extract the partitioning factor for a single geometry, but do not offer a generic description for geometry scaling.

4.4.16 Intra-device substrate coupling

Measurement data	cold Y-parameters of relevant transistor configurations
Required model parameters	r_E (is of minor importance though)
Required geometry data	None
Procedure:	• Determine the impedance Z_{su} of the substrate coupling network and extract r_{su} and C_{su} from real and imaginary part of $1/Z_{su}$. • Alternative (also for parameter library generation): calculation from simulation after experimental calibration.
Extracted (specific) parameters	
Related HICUM parameters	r_{su}, C_{su}

Presently existing methods only allow to extract the substrate resistance for a single geometry, but do not offer a generic description for geometry scaling.

4.4.17 High-frequency emitter current crowding

Measurement data	hot Y-parameters of different transistor configurations
Required model parameters	• those of i_T and i_{BE} • all capacitances (incl. transit time) at the base node • r_E, r_{Bx}, r_{Bi}
Required geometry data	None
Procedure:	• f_{CrBi} can be determined from optimizing the model's y_{11} at high frequencies to the results of a transistor with the largest emitter width offered in a process. • Alternative (also for parameter library generation): use $f_{CrBi} = 0.2$
Extracted (specific) parameter	f_{CrBi}
Related HICUM parameter	f_{CrBi}

Presently existing methods only allow to extract f_{CrBi} from experimental data of a single geometry, but do not offer a generic description for geometry scaling. In addition, the modeling approach can only be applied to the small-signal case.

4.4.18 Parasitic substrate transistor elements

Geometry scaling of the substrate junction related currents depends on the process. For practical applications, the minimum effort is assumed to be spent on modeling and parameter extraction of the substrate transistor.

4.4.18.1 Transfer current

Measurement data	transistor configurations with different substrate size
Required model parameters	• if separate substrate pad is available: none • if in HF pads: base current components
Required geometry data	substrate perimeter length and/or area
Procedure:	• Separation into bias dependent bottom and/or perimeter specific current components via different geometries. • Extraction of parameters related to bias dependence from least-squares fit of $\log(I_{Ts})$ vs. V_{SC}.
Extracted (specific) parameters	I'_{TsS} or $\overline{I}_{TsS}$, m_{sf}
Related HICUM parameters	I_{TsS}, m_{sf}

4.4.18.2 Charge storage time

Measurement data	hot Y-parameters for a critical transistor configuration at (very) low V_{CE} (optional: different transistor configurations)
Required model parameters	transit time, C_{BE}, C_{BC}
Required geometry data	none
Procedure:	adjust τ_{sf} to fit f_T at low V_{CE}.
Extracted (specific) parameter	τ_{sf}
Related HICUM parameter	τ_{sf}

It is assumed that no separate substrate test transistor is available in HF pads to directly measure the S-parameters of the substrate transistor.

4.4.19 Temperature dependence

T_0 is the (reference) temperature at which the parameter extraction for modeling the bias and frequency dependent transistor behavior is performed. For extracting the relevant model parameters, the same measurements as for T_0 are repeated for different temperatures T.

4.4.19.1 Series resistances

Measurement data	IV data at different temperatures T
Required model parameters	series resistances and/or their components at T_0
Required geometry data	None
Procedure:	• determine the respective resistance r for each T • fitting of the ratio $\log[r(T)/r(T_0)]$ vs. (T/T_0) with the respective exponent factor ζ as parameter.
Extracted (specific) parameters	ζ_{Ci}, ζ_{rBi}, ζ_{rBx}, ζ_{rCx}, ζ_{rE}
Related HICUM parameters	ζ_{Ci}, ζ_{rBi}, ζ_{rBx}, ζ_{rCx}, ζ_{rE}

4.4.19.2 Bandgap voltage

Measurement data	$I_C(V_{BE})$ data at V_{BC}=0 for different temperatures T
Required model parameters	none
Required geometry data	none
Procedure:	• Determine the saturation current I_S and the non-ideality coefficient at various temperatures. • Extract V_{gB} from a least-squares fit based on $I_S(T)$
Extracted (specific) parameter	V_{gB}
Related HICUM parameter	V_{gB}

4.4.19.3 TC of the forward current gain

Measurement data	$I_C(V_{BE})$, $I_B(V_{BE})$ data at V_{BC}=0 for different temperatures T
Required model parameters	none
Required geometry data	none
Procedure:	• Determine $B(I_C)$ at various temperatures. • Extract α_{Bf} from $B(I_C$=const) vs. T-T_0 via least-squares fit
Extracted (specific) parameter	α_{Bf}
Related HICUM parameter	α_{Bf}

4.4.19.4 Transit time at low current densities

Measurement data	hot Y-parameters vs bias (at V_{BC}=0) for different temperatures T
Required model parameters	none
Required geometry data	none
Procedure:	• Determine the low-current transit time τ_{f0} for each T • Extract $\alpha_{\tau 0}$ and $k_{\tau 0}$ from $\tau_{f0}(T)$ via non-linear optimization
Extracted (specific) parameters	$\alpha_{\tau 0}$, $k_{\tau 0}$
Related HICUM parameters	$\alpha_{\tau 0}$, $k_{\tau 0}$

4.4.19.5 Critical current

Measurement data	hot Y-parameters vs bias (at V_{BC}=0) for different temperatures T
Required model parameters	none
Required geometry data	none
Procedure:	• Determine the transit time τ_f and the critical current I_{CK} for each T • Extract α_{CEs} from re-fitting I_{CK} at each T with V_{CEs}(T) as a parameter. • α_{vs} can be taken from literature
Extracted (specific) parameters	α_{vs} , α_{CEs}
Related HICUM parameters	α_{vs} , α_{CEs}

4.4.19.6 BC breakdown

Measurement data	I_B(V_{CB} or V_{CE}) data for different temperatures T
Required model parameters	none
Required geometry data	none
Procedure:	• Determine the avalanche current I_{AVL} from I_B for each T • With α_{fav} and α_{qav} as variables, perform a nonlinear optimization on the measured data for I_{AVL} by exercising the compact model with fixed values for f_{AVL} and q_{AVL}, that were determined at the reference temperature T_0.
Extracted (specific) parameters	α_{fav} , α_{qav}
Related HICUM parameters	α_{fav} , α_{qav}

4.5 Flowchart and comparison to SGPM

The PBSA allows to combine the parameter extraction of different compact models with a minimum of additional effort. Fig. 4.5.0/1 visualizes the overall extraction flow including the modules that are model independent ("general") and those that are specific to the SGPM and HICUM. This provides a rough overview on the effort required to add a new model such as HICUM to an existing parameter extraction for the SGPM and vice versa (i.e. keeping the SGPM in the loop as a backup). The program TRADICA allows to generate both types of models as well as a hierarchy of SGPMs with different complexity from a single set of extracted geometry specific parameters.

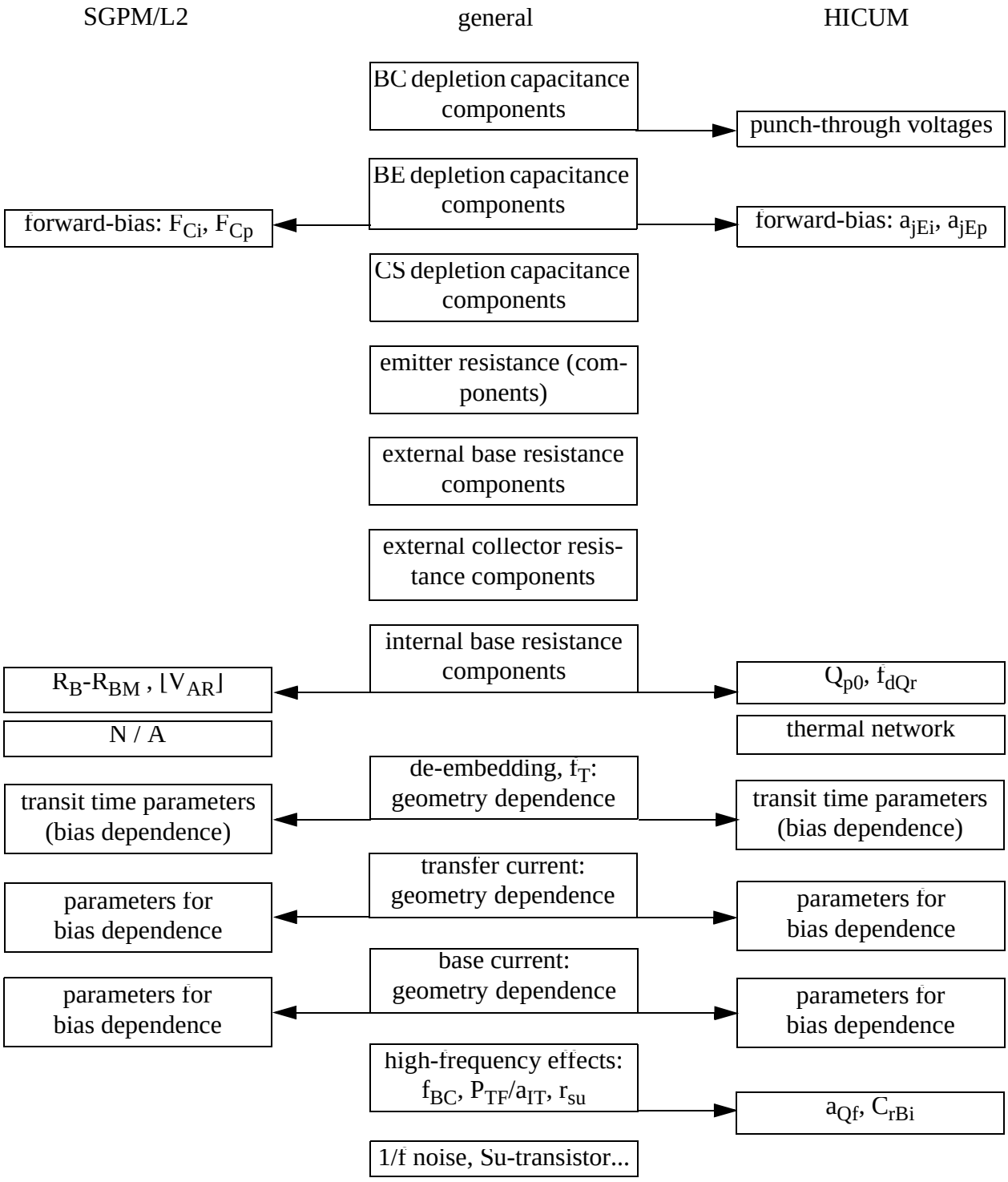


Fig. 4.5.0/1: Rough overview on the flow and modules for a combined geometry scalable parameter extraction for both SGPM and HICUM. SGPM/L2 corresponds to a similar equivalent circuit as HICUM, including, e.g., separate elements for the emitter perimeter injection and a partitioning of the base resistance and external BC capacitance.

4.6 Measurement conditions

The table below contains an overview on the most important measurements to be performed and the associated bias conditions. The values are examples and given for Si-based processes. Only a minimum number of measurements is specified (i.e. more data is always useful).

measurement type and bias conditions	data	result

• internal base pinch resistance data from at least 3 structures with different b_E;
  • V_{BE}=[-0.5,0.5]V @ V_{CE}=0, ΔV_{BE}=0.1V, ΔV_{BB}=0.01V
• sheet and contact resistances of ext. base region, buried layer, collector (sinker, contact)
  • ΔV=0.01...0.1V, depending on resistance value
	V_{BE} I_{B1} I_{B2}
	
	ΔV I (or r_S, r_{con} ...)
		base and collector series resistance components

• C-V on large area transistor
  • V_{BE}=[-0.5,0.5]V, V_{BC}=V_{SC}=0, ΔV_{BE}=0.1V
  • V_{BC}=[-BV_{CEO},0.5]V,V_{BE}=V_{SC}=0, ΔV_{BC}=0.1V
  • V_{SC}=[-BV_{CEO},0.5]V,V_{BE}=V_{BC}=0, ΔV_{SC}=0.1V
• C-V on large area BC diode (only for transistors with selectively implanted collector)
  • V_{BC}=[-BV_{CEO},0.5]V,V_{BE}=V_{SC}=0, ΔV_{BC}=0.1V
	V_{BE} C_{jE}
	V_{BC} C_{jC}
	V_{SC} C_{jS}
	
	V_{BC} C_{jC}(epi)
		depletion and isolation capacitance components

• cold S-parameters as a function of bias on ≥ 3 transistors with different b_E (<< l_E)
  • V_{BE}=[-0.5, 0.5]V, V_{BC}=0, ΔV_{BE}=0.1V
  • V_{BC}=[-BV_{CEO}, 0.5]V, V_{BE}=0, ΔV_{BC}=0.1V
	V_{BE} $\underline{S}$
	V_{BC} $\underline{S}$
		depletion and isolation capacitance components

• S-parameters as a function of bias on at least 3 transistors with different b_E (<<l_E) : • I_C/A_E=[0.01, 2]mA/μm^2 (depends on process) for at least 3 V_{CE}, e.g. V_{CE}/V=0.5, 1.5, BV_{CEO}	V_{BE} V_{CE} I_C I_B $\underline{S}$	f_T, τ_f, certain forward I-V parameters; verification

• d.c. output characteristics (reference transistor only)
  • V_{CE}=[0V, $V_{CE,max}$] @ I_B=const / V_{BE}=const ($V_{CE,max}$<BV_{CEO}(high I_C/A_E))
  • I_C/A_E=[0.01,2]mA/μm^2 (depends on process !!)
	V_{CE} I_C I_B V_{BE}	Avalanche, certain I_C parameters; verification

measurement type and bias conditions	data	result
• d.c. reverse characteristic (reference transistor only) • V_{BC}=[0.4, 0.7]V @ V_{BE}=0V	V_{BC} I_B [I_C]	BC diode current
• Temperature dependence: e.g. T=[-40, 75, 125] ^oC • repeat above measurements • shift V_{BE} bias according to temperature, assuming a TC of about -1.5mV/K	T, ...	TCs

5 Circuit simulators

5.1 Availability

Information on the availability of HICUM in commercial circuit simulators at the present time can be found on the same web-site as this document. HICUM has been implemented in a number of circuit simulators; early HICUM versions had been implemented also in SPICE2G5 and SPICE3F2. Due to the fact that every circuit simulator interface is different, the model code is forced to be arranged differently in every commercial simulator. As a result, a “generic” C or FTN source code of the model, that fits into any simulator and is sometimes requested, is not possible. Therefore, those existing codes that are embedded in the interfaces of the various simulators and cannot be released for legal reasons.

Model development takes place in MATLAB and the in-house mixed-mode device/circuit simulator DEVICE. The latter is, therefore, the reference simulator for model testing. Also, the source code of HICUM in DEVICE is available as “template” for model implementation into other (commmercial) simulators.

Although every officially released version of the model has been tested extensively, not every circuit and application can be tested, and the user is encouraged to report problems that are believed to be caused by the model.

The HICUM version described in this manual models currents and charges in a continuously differentiable way to ensure convergence in standard SPICE-type circuit simulators. Other types of simulators might behave differently.

5.2 Operating point information

Below is a list of those quantities that should be provided by the circuit simulator to the model user as “operating point information”. The voltages in the expressions are defined as follows:

$$V_{BEi} = V_{B'} - V_{E'}$$
$$V_{BEx} = V_{B*} - V_{E'}$$
$$V_{BCi} = V_{B'} - V_{C'}$$
$$V_{BCx} = V_{B*} - V_{C'}$$
$$V_{SCi} = V_{S'} - V_{C'}$$

Variable	Unit	Description	Definition
IB	A	Base terminal current	as calculated in the model
IC	A	Collector terminal current	as calculated in the model
IS	A	Substrate terminal current	as calculated in the model
VBE	V	External *BE* voltage	as calculated in the model
VBC	V	External *BC* voltage	as calculated in the model
VCE	V	External *CE* voltage	as calculated in the model
VSC	V	External *SC* voltage	as calculated in the model
BETADC		Common emitter forward current gain	$\frac{I_C}{I_B}$
GM	A/V	Transconductance (Same definition as for SGPM)	$\left.\frac{\partial I_T}{\partial V_{BEi}}\right\|_{V_{CEi}} = \left.\frac{\partial I_T}{\partial V_{BEi}}\right\|_{V_{BCi}} + \left.\frac{\partial I_T}{\partial V_{BCi}}\right\|_{V_{BEi}}$
GMAVL	A/V	Transconductance for avalanche current	$\left.\frac{\partial I_{AVL}}{\partial V_{BEi}}\right\|_{V_{BCi}}$
GMS	A/V	Transconductance of the parasitic substrate PNP	$\left.\frac{\partial I_{TS}}{\partial V_{BCx}}\right\|_{V_{SCi}} - \left.\frac{\partial I_{TS}}{\partial V_{SCi}}\right\|_{V_{BCx}}$
RPIi	Ω	Intrinsic input resistance	$\frac{1}{r_{\pi i}} = \frac{\partial I_{BEi}}{\partial V_{BEi}}$

Variable	Unit	Description	Definition
RPIx	Ω	Extrinsic input resistance	$\frac{1}{r_{\pi x}} = \frac{\partial I_{BEp}}{\partial V_{BEx}} - \frac{\partial I_{BEt}}{\partial V_{BEx}}$ (second term is due to tunnelling current)
RMUi	Ω	Intrinsic feedback resistance	$\frac{1}{r_{\mu i}} = \frac{\partial I_{BCi}}{\partial V_{BCi}} - \left.\frac{\partial I_{AVL}}{\partial V_{BCi}}\right\|_{V_{BEi}}$ (second term is due to avalanche current)
RMUx	Ω	Extrinsic feedback resistance	$\frac{1}{r_{\mu x}} = \frac{\partial I_{BCx}}{\partial V_{BCx}}$
RMUs	Ω	Intrinsic substrate feedback resistance	$\frac{1}{r_{\mu s}} = \frac{\partial I_{SC}}{\partial V_{SCi}}$
RO	Ω	Output resistance (same definition as for SGPM)	$\frac{1}{r_o} = -\left.\frac{\partial I_T}{\partial V_{BCi}}\right\|_{V_{BEi}}$
ROs	Ω	Output resistance for the parasitic substrate PNP	$\frac{1}{r_{os}} = -\frac{\partial I_{TS}}{\partial V_{SCi}}$
CPIi	F	Total intrinsic *BE* capacitance	$C_{\pi i} = C_{jEi} + C_{dE}$
CPIx	F	Total extrinsic *BE* capacitance	$C_{\pi x} = C_{iEp} + C_{Eox}$
CMUi	F	Total intrinsic *BC* capacitance	$C_{\mu i} = C_{jCi} + C_{dC}$
CMUx	F	Total extrinsic *BC* capacitance	$C_{\mu x} = C_{jCx} + C_{Cox} + C_{dS}$
CCS	F	*CS* junction capacitance	C_{jS}
RBI	Ω	Internal base resistance	as calculated in the model
CRBI	F	Shunt capacitance across RBI	as calculated in the model
TF	s	Total forward transit time	as calculated in the model
FT	Hz	Transit frequency (still simplified expression, but improved vs. SGPM)	$\frac{g_m}{C_{BE} + C_{BC} + (\tau_f + rC_{BC})g_m}$, $C_{BE} = C_{\pi i} + C_{\pi x}$, $C_{BC} = C_{\mu i} + C_{\mu x}$, $r = r_{Cx} + r_E + r_B/\beta_0$

Variable	Unit	Description	Definition
VEF	V	Effective forward Early voltage	$\frac{I}{I_T}\frac{\partial I_T}{\partial V_{CEi}}\Big\|_{V_{BEi}} - V_{CEi}$
VER	V	Effective inverse Early voltage	$\frac{I}{I_T}\frac{\partial I_T}{\partial V_{BEi}}\Big\|_{V_{BCi}} - V_{BEi}$

6 Experimental Results

This chapter contains selected examples that demonstrate HICUM's capabilities of modelling bias, frequency, geometry and temperature dependent transistor behaviour. If not specified otherwise, all results were obtained using a *scalable single basic parameter set* (cf. chapter 4 and 5). The results cover not only a large variety of processes, ranging from low-speed (6 GHz) to high-speed (50 GHz SiGe) processes and even an example for a vertical pnp, but also various modes of operation (d.c. small-signal, large-signal). The major emphasis is on high-frequency (h.f.) characteristics and figures of merit that are related to h.f. (circuit) applications. Considering the above mentioned variables (bias, geometry, temperature, frequency), model verification is becoming a quite difficult task, the effort of which is often severely underestimated.

Wherever possible, the following comparisons are performed in normalized form and in variables that are related to circuit design; for instance, often the current density I_C/A_E is employed (to allow process comparisons), and the bias points are defined by $(I_C/A_E,V_{CE})$. The results do not contain examples for junction capacitance modelling, which has already been shown to be accurate. The experimental results given below cover the following areas:

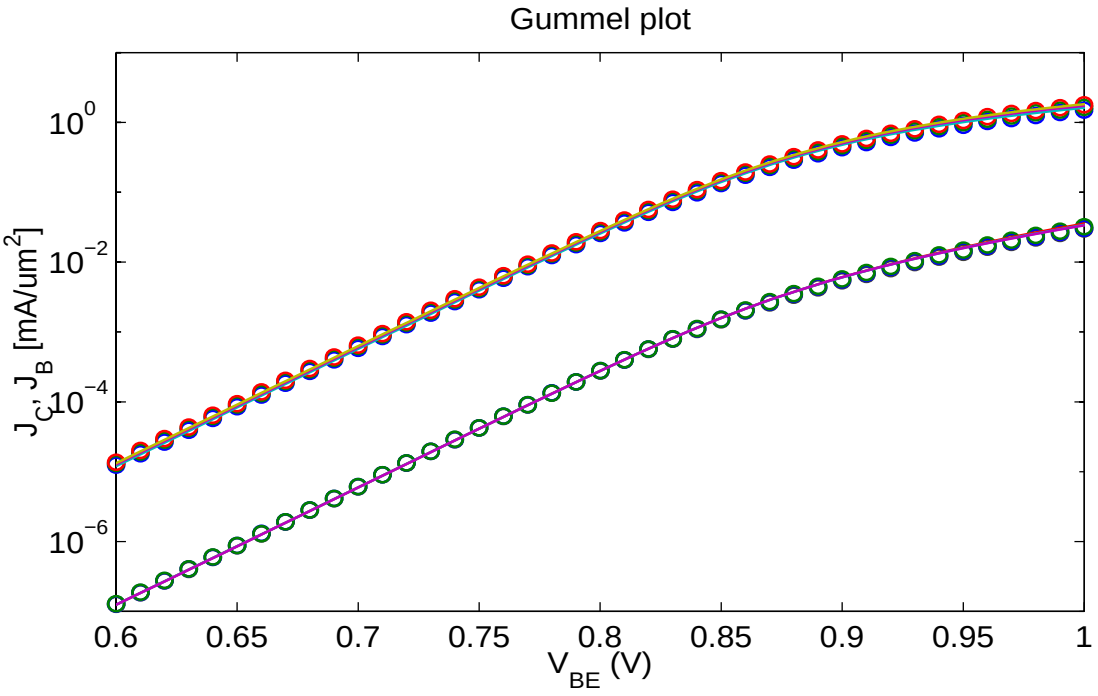
- d.c. characteristics including I-V and current gain curves as well as conductances vs. bias.
- Bias dependence of transit time τ_f and transit frequency f_T. An accurate approximation of the transit time and the junction capacitances, which are a fundamental (linearly independent) variables in HICUM, guarantee an accurate modelling of composite parameters, such as f_T and y-parameters.
- For small-signal characteristics, y-parameters are preferred, since they can be easier linked directly to elements in the transistor equivalent circuit (e.g. [13,28,36]). The examples contain comparisons of all four y-parameters vs. frequency, bias, and geometry.
- High-speed switching is difficult to measure directly and accurately for today's fast transistors; therefore, HICUM was verified by 2D and 3D mixed-mode device/circuit simulation [37]. For older (slower) processes, however, HICUM could be verified experimentally [25,31].
- Temperature dependent modelling has been pursued and compared to experimental data for several process generations (e.g. [31,32,41]), leading to reliable model formulations.
- Noise: both 1/f and high-frequency noise have been investigated as a function of bias, frequency and geometry (cf. [5,6,7,8]) and have been compared to measurements.
- Non-linear h.f. distortion can be considered as another way to verify a model's large-signal behaviour. In the presented examples, the output power P_{out} as response to a single-tone input power P_{in} is compared to measurements over frequency, bias and geometry for different types of transistors.
- Predictive and statistical modelling capability is important for reducing design cycle time, but have not been included for bipolar applications in commercial simulators and design tools in a physics-based and generic way. The given examples show f_T as one of several useful figures of

merit (FoM) for high frequency applications; compared to other h.f. FoMs, f_T is clearly defined and can most easily be measured, although its measurement time is still not suitable for statistical data acquisition.

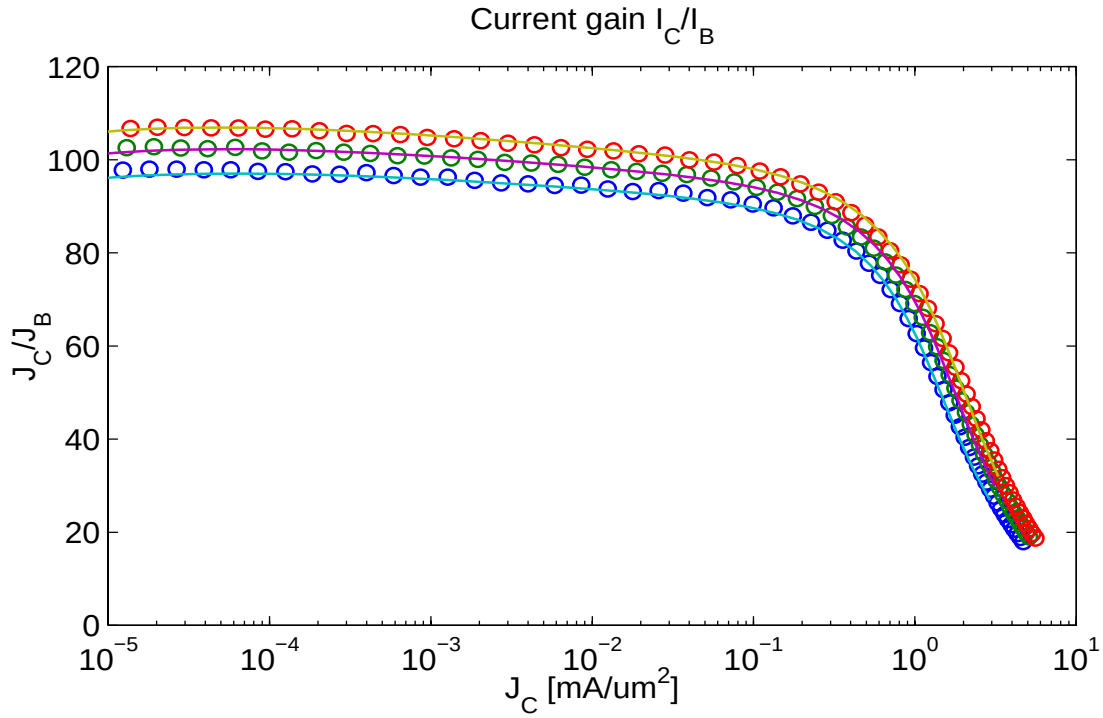
- Circuit results have been included for a CML ring-oscillator as standard benchmark circuit for digital applications. Sufficiently simple benchmark circuits for wireless applications are more difficult to obtain.

6.1 DC characteristics

(a)

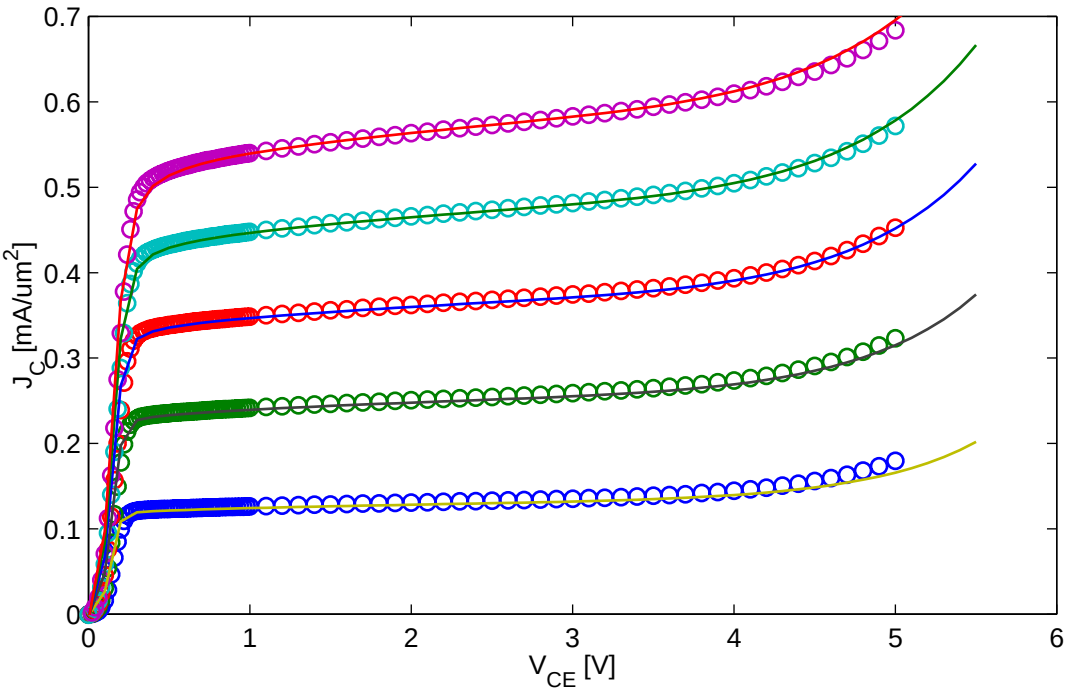


(b)

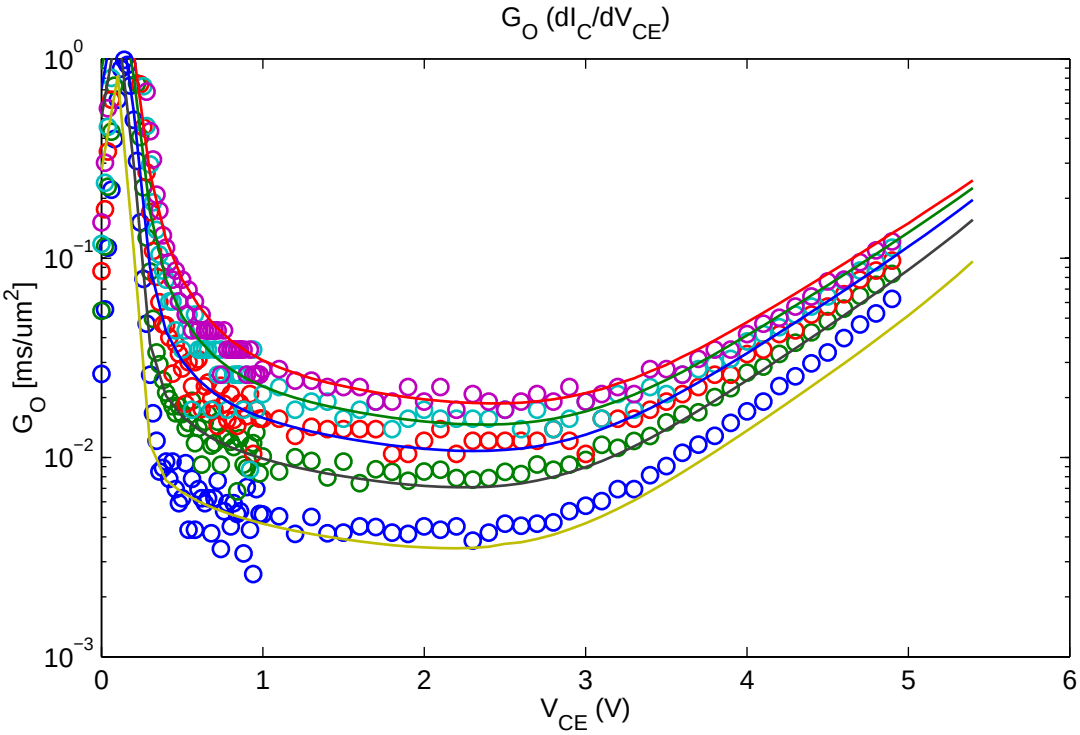


Comparison between measurement (symbols) and HICUM (solid lines) from a single transistor parameter extraction for a 12 GHz bipolar transistor [4]: (a) Gummel plot; (b) current gain. V_{BC}/V = 0,-2,-4; emitter size: 0.6*4.8µm^2

(a)

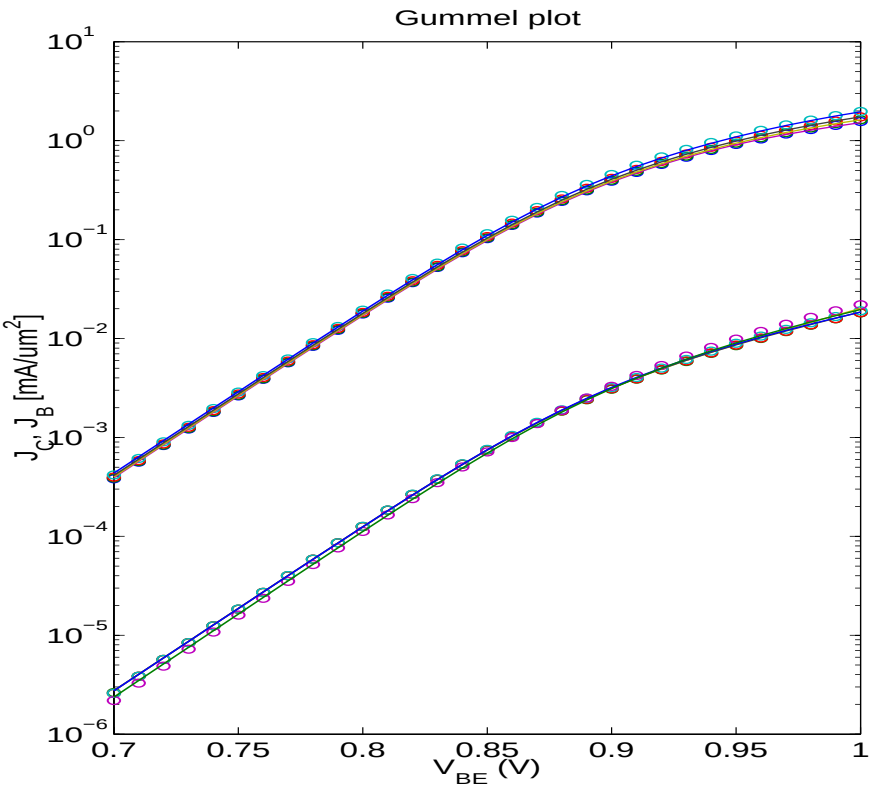


(b)

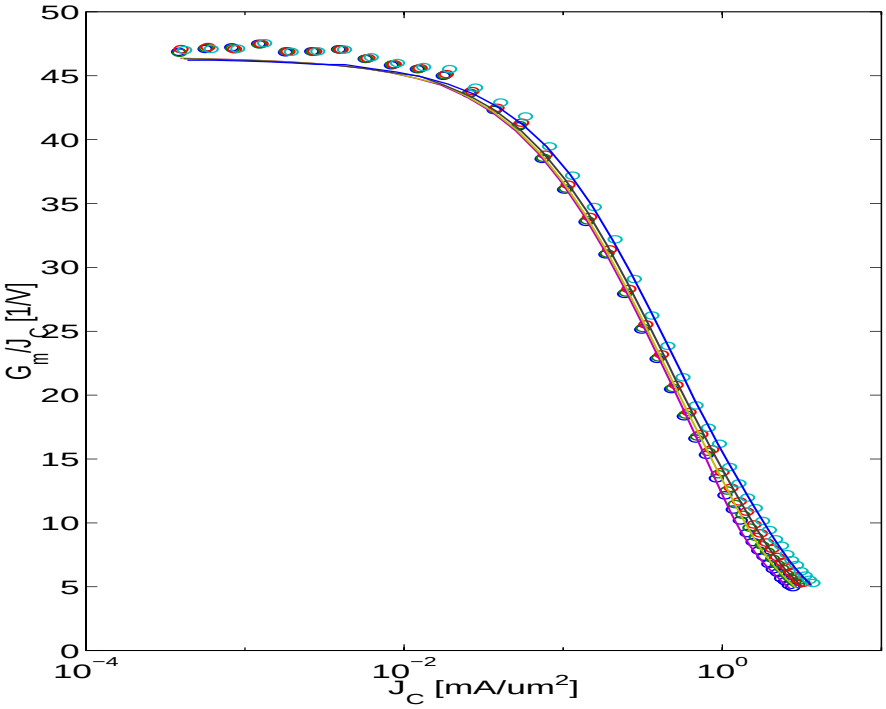


Comparison between measurement (symbols) and HICUM (solid lines) from a single transistor parameter extraction for a 12 GHz bipolar transistor [4]: (a) output characteristics for I_B=const; (b) output conductance dI_C/dV_{CE}; emitter size: 0.6*4.8µm^2

(a)

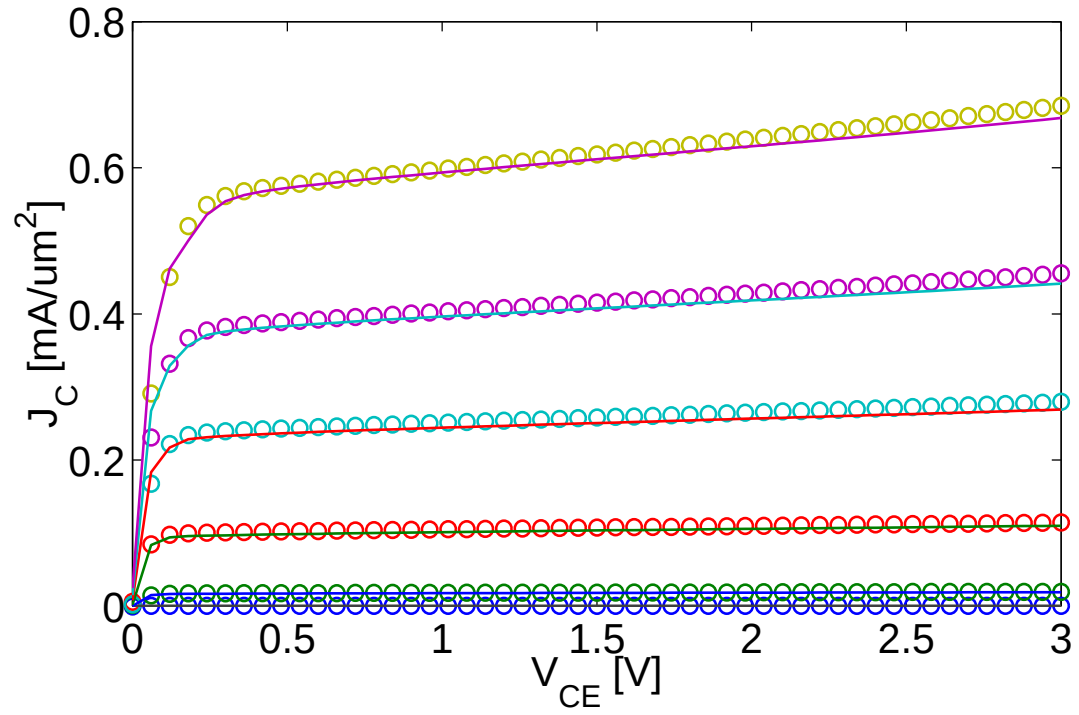


(b)

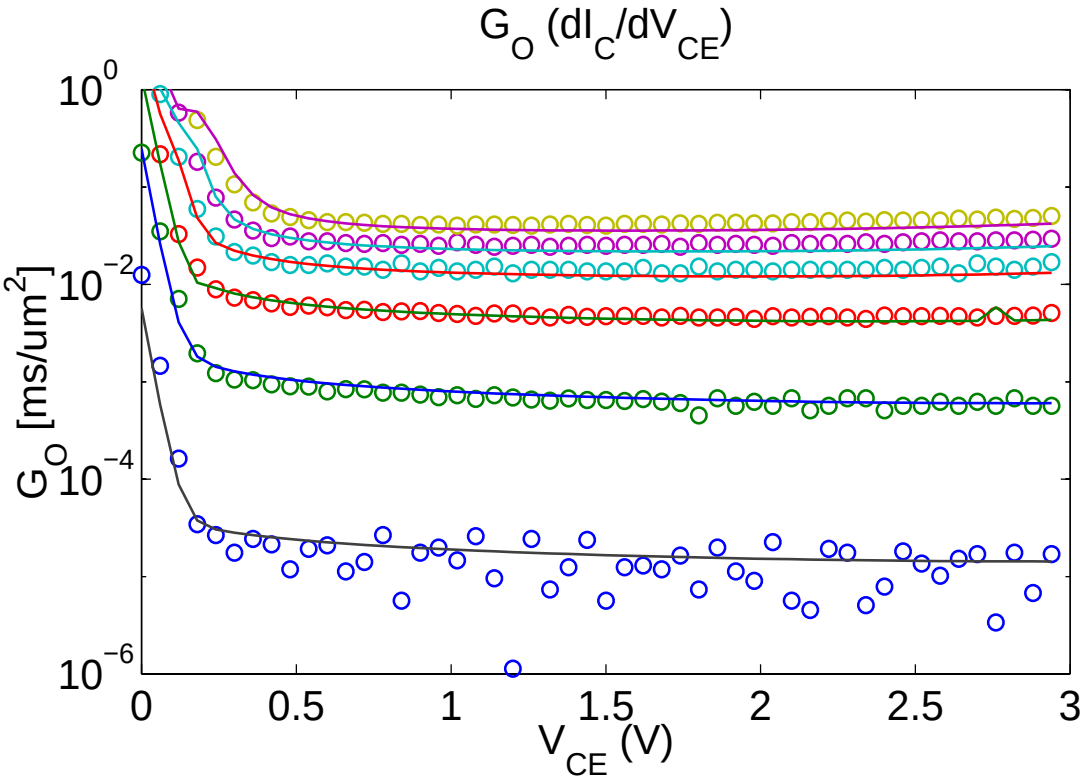


Comparison between measurement (symbols) and HICUM (solid lines) for a 25 GHz bipolar transistor: (a) Gummel plot; (b) normalized transconductance. V_{CE}/V=0.5,0.8,1.5,3;
emitter size: 0.4*14µm^2

(a)



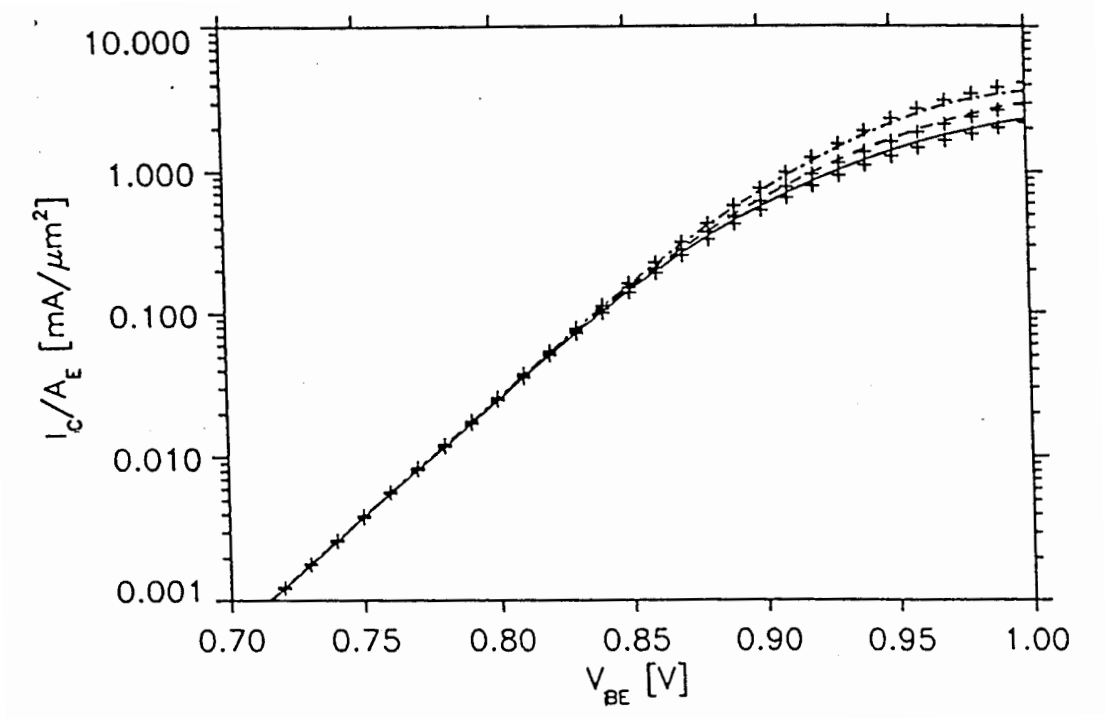
(b)



Comparison between measurement (symbols) and HICUM (solid lines) for a 25 GHz bipolar transistor: (a) output characteristics for V_{BE}=const; (b) output conductance dI_C/dV_{CE}; emitter size: 0.4*14µm^2.

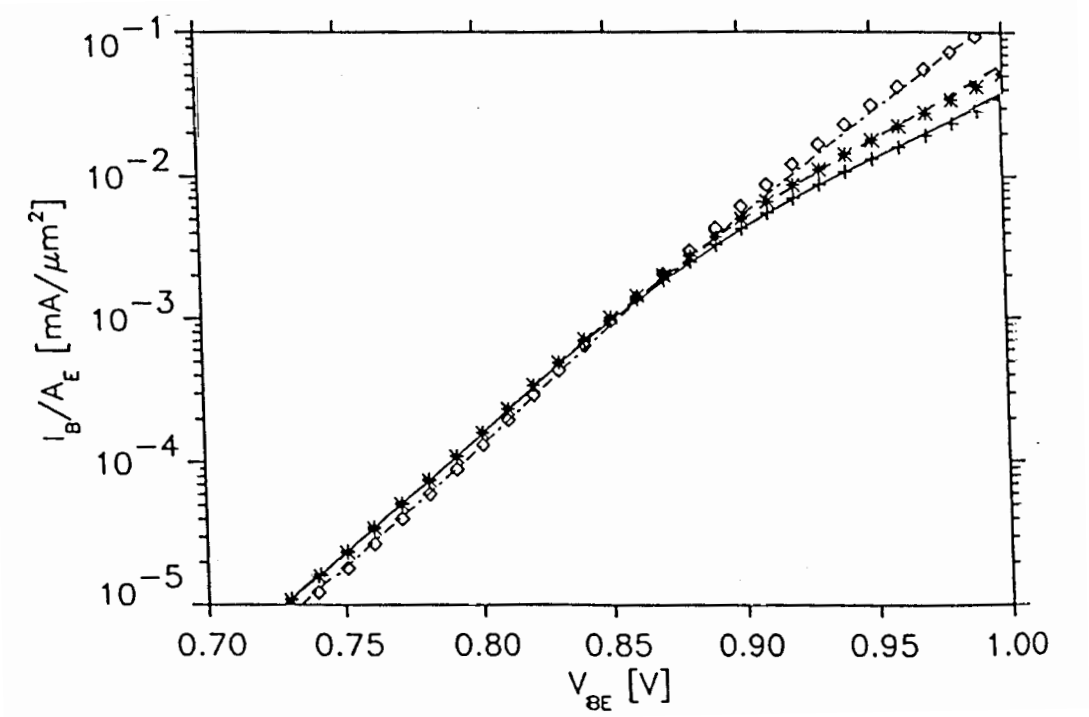
(a)

(a)



(b)

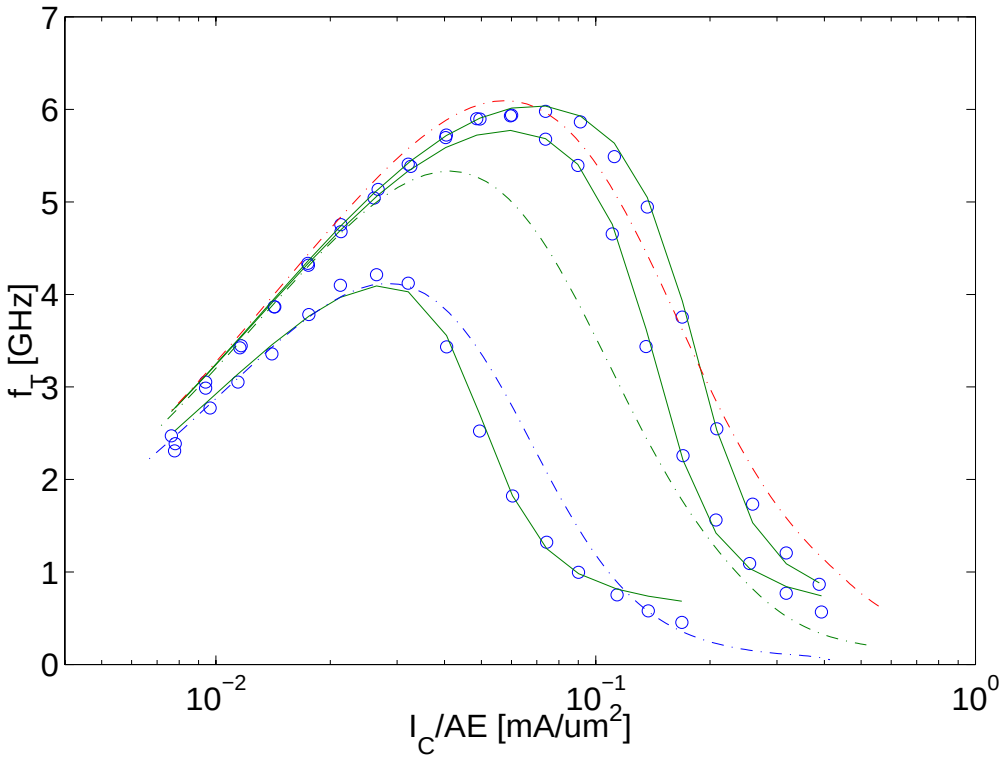
(b)



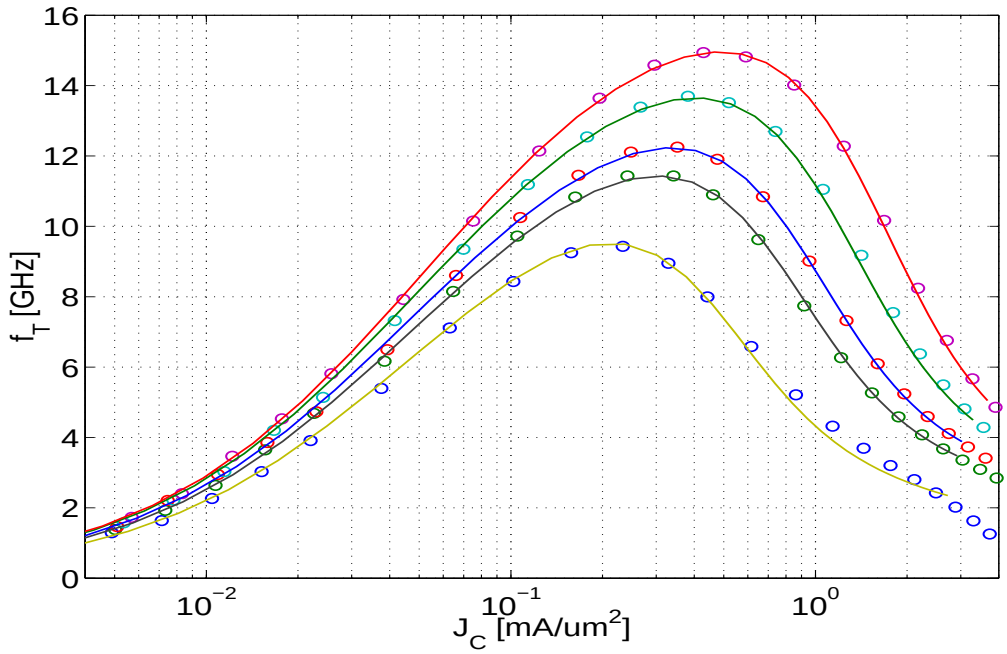
Comparison between measurement (symbols) and HICUM (solid lines) for a 45 GHz IBM SiGe bipolar transistor [47,48]: (a) collector current density; (b) base current density.
V_{CE}/V=0.8,1.6,2.4; emitter size: 0.5*10μm^2. Self-heating and avalanche breakdown are quite pronounced for this transistor.

6.2 Transit frequency and transit time

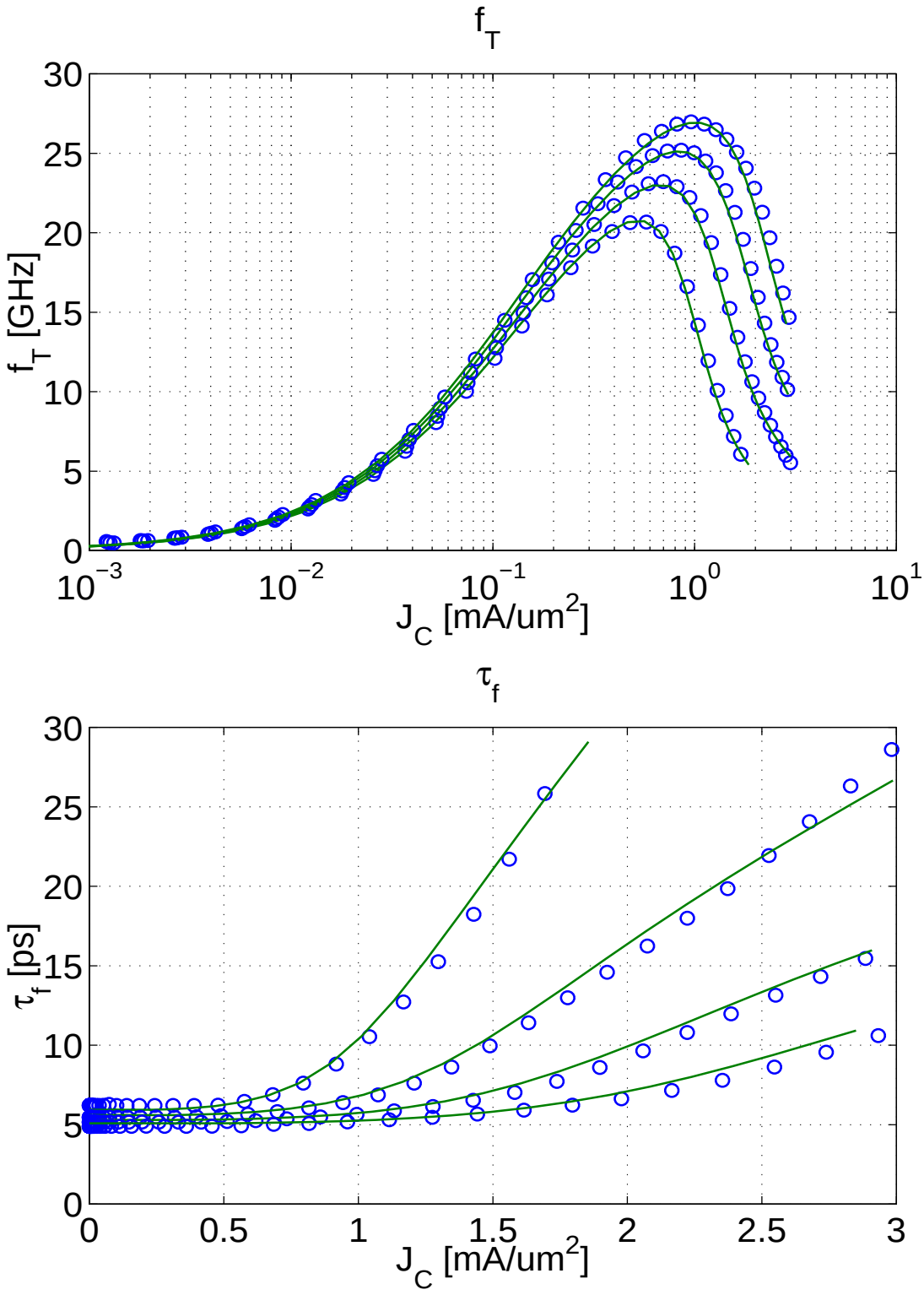
(a)



(b)

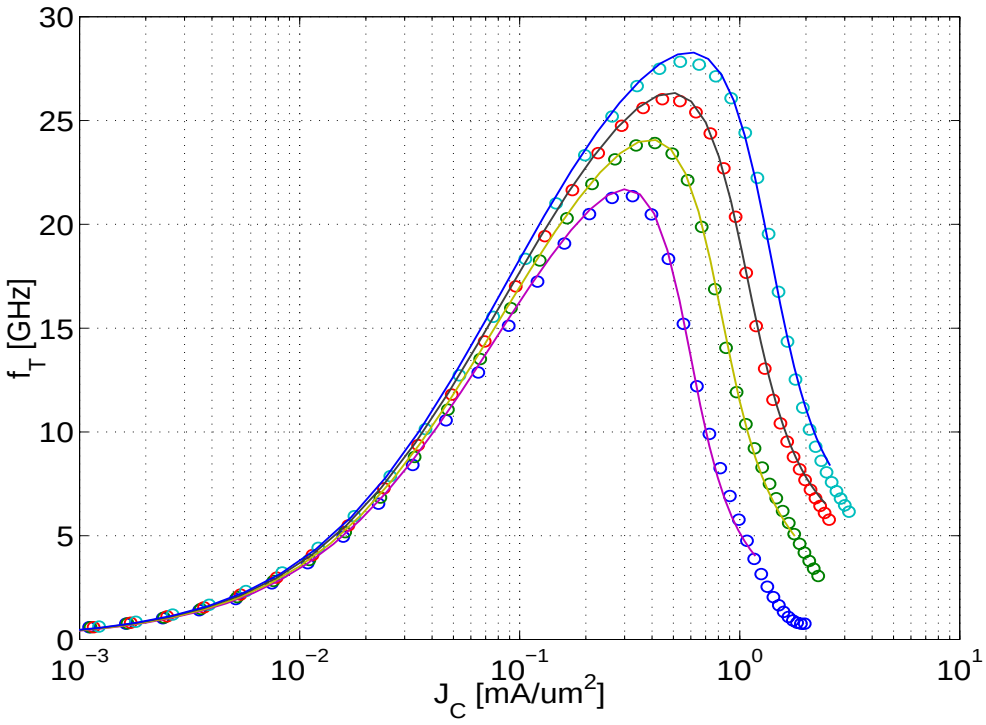


Transit frequency vs. collector current density (V_{BC}=const) for different bipolar processes. Comparison between measurement (symbols) and HICUM (solid lines) from single transistor parameter extraction: (a) emitter size 0.5*10µm^2, V_{BC}/V=0,-5,-10 (the dashed lines are the results of the SPGM) [17,41]; (b) emitter size 0.6*4.8µm^2; V_{BC}/V = 0.5, 0, -0.5, -2,-4 [4,17].

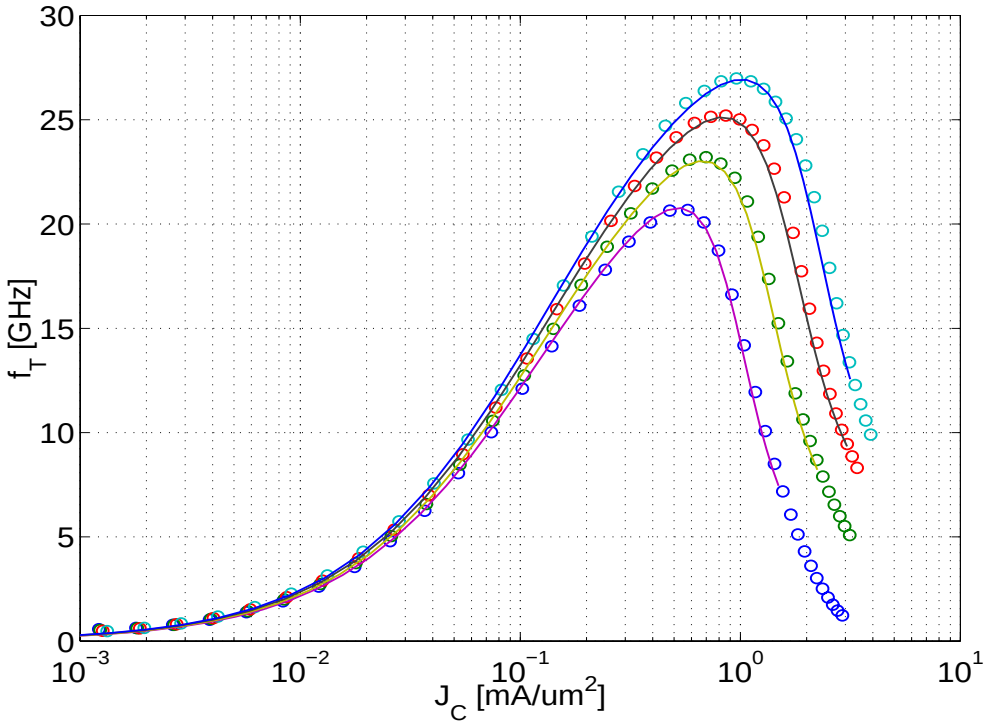


Comparison between measurement (symbols) and HICUM (solid lines) for a 25GHz bipolar process [41]: (a) transit frequency; (b) transit time. Emitter size 0.4*14µm^2, V_{CE}/V=0.5,0.8,1.5,3.

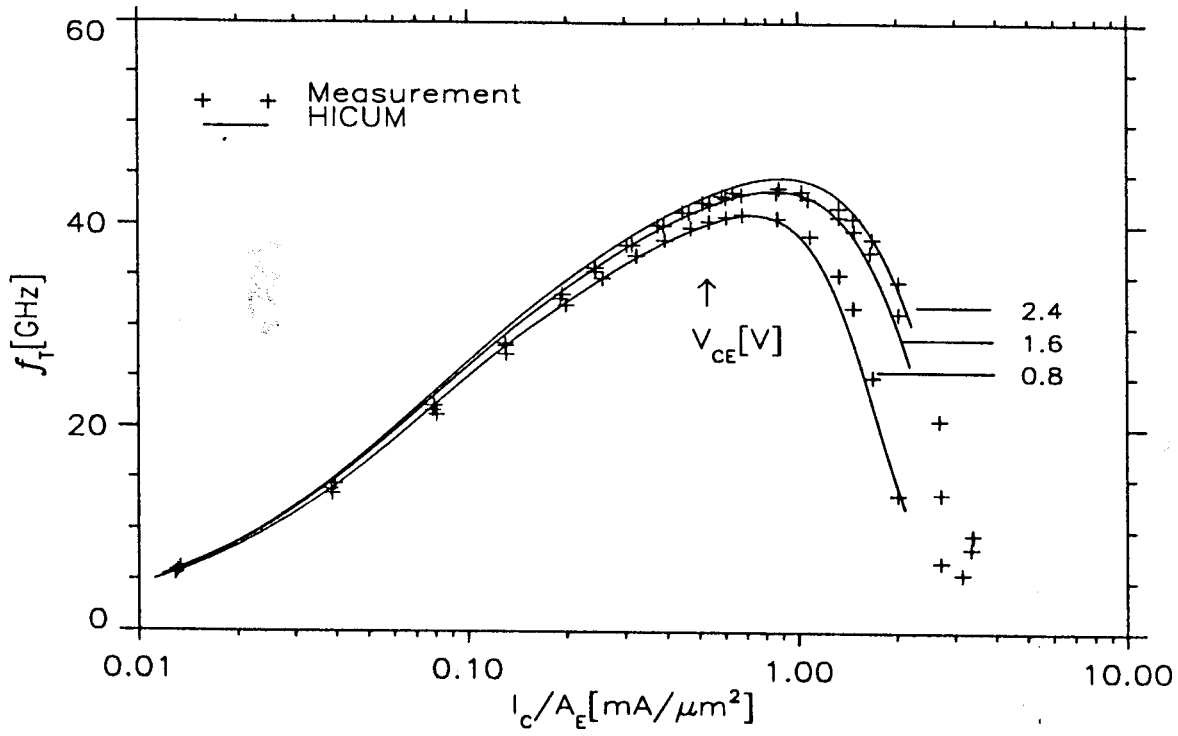
(a)



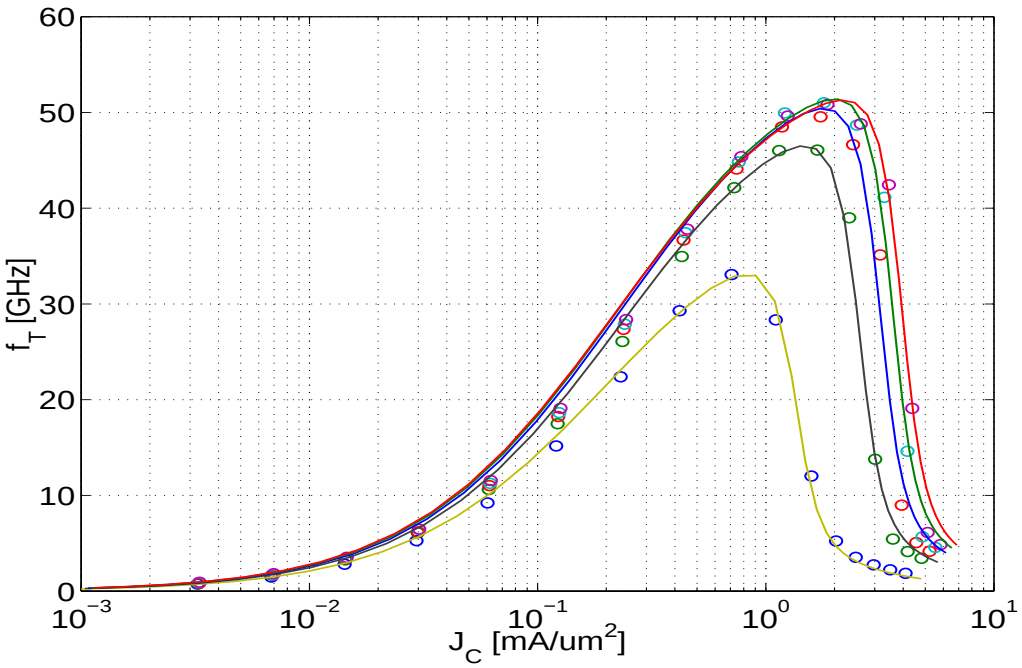
(b)



Comparison for the bias dependent transit frequency between measurement (symbols) and HICUM (solid lines) for a 25GHz bipolar process. Transistor size: (a) 1.2*14µm^2; (b) 0.4*1.4µm^2. V_{CE}/V=0.5, 0.8, 1.5, 3.



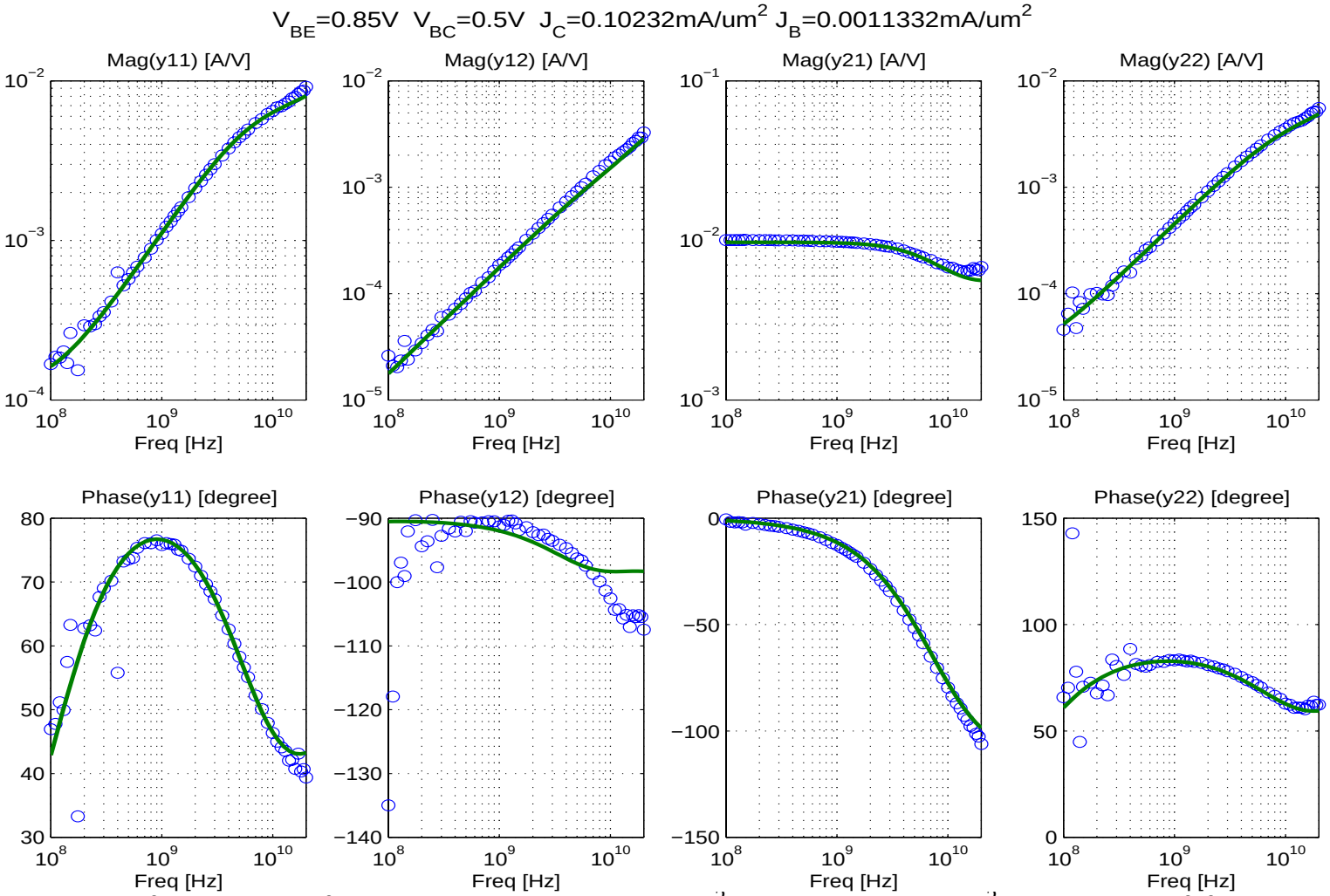
Bias dependent transit frequency of an IBM SiGe bipolar transistor. Comparison between measurement (symbols) and HICUM (solid lines) [48]; emitter size 0.5*10μm^2; V_{CE}/V=0.8,1.6,2.4.



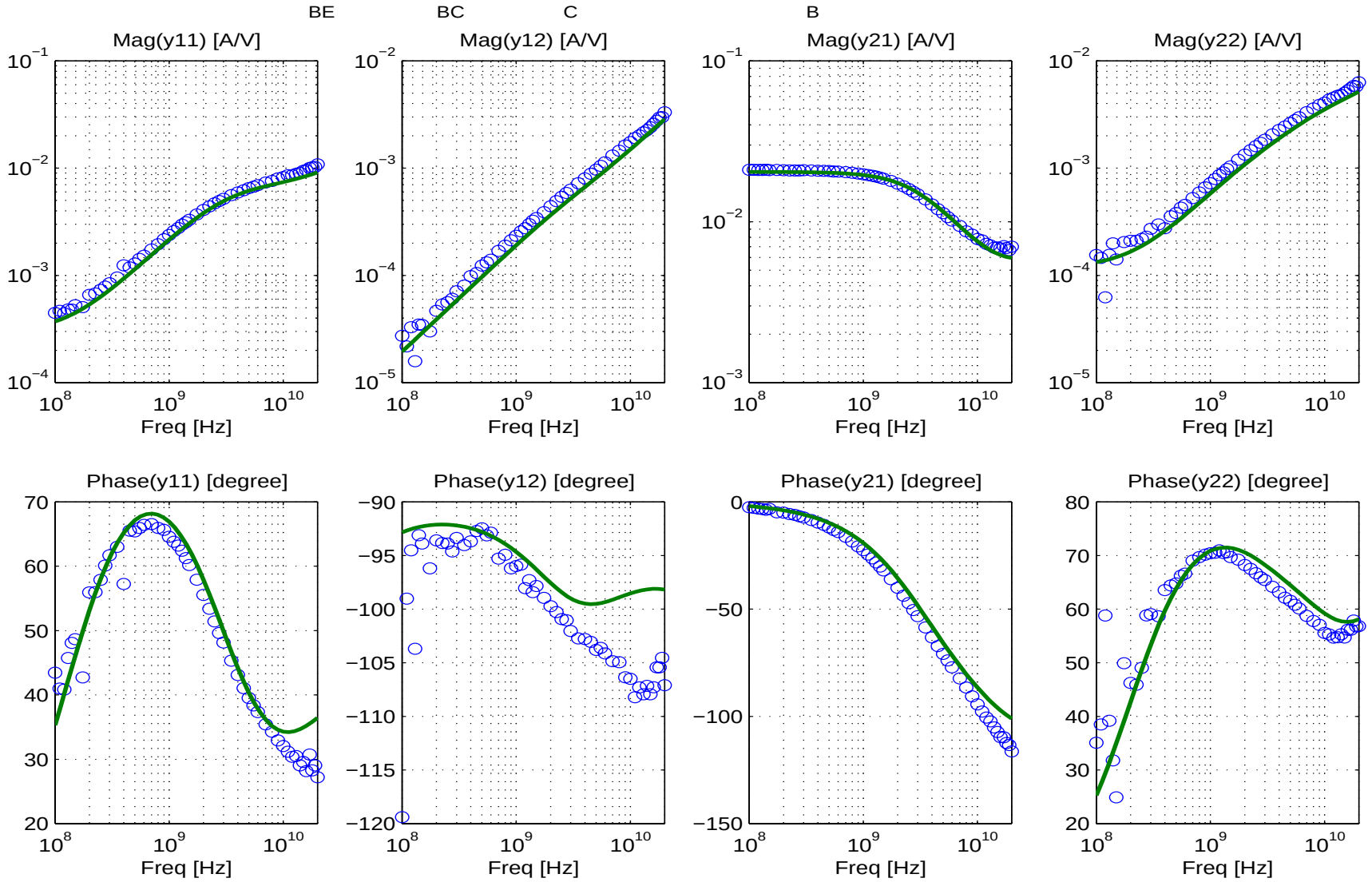
Bias dependent transit frequency of a SiGe bipolar process [4]. Comparison between measurement (symbols) and HICUM (solid lines); emitter size 0.4*2μm^2; V_{BC}/V = 0.5, 0, -0.5, -1, -1.5.

6.3 High-frequency small-signal characteristics

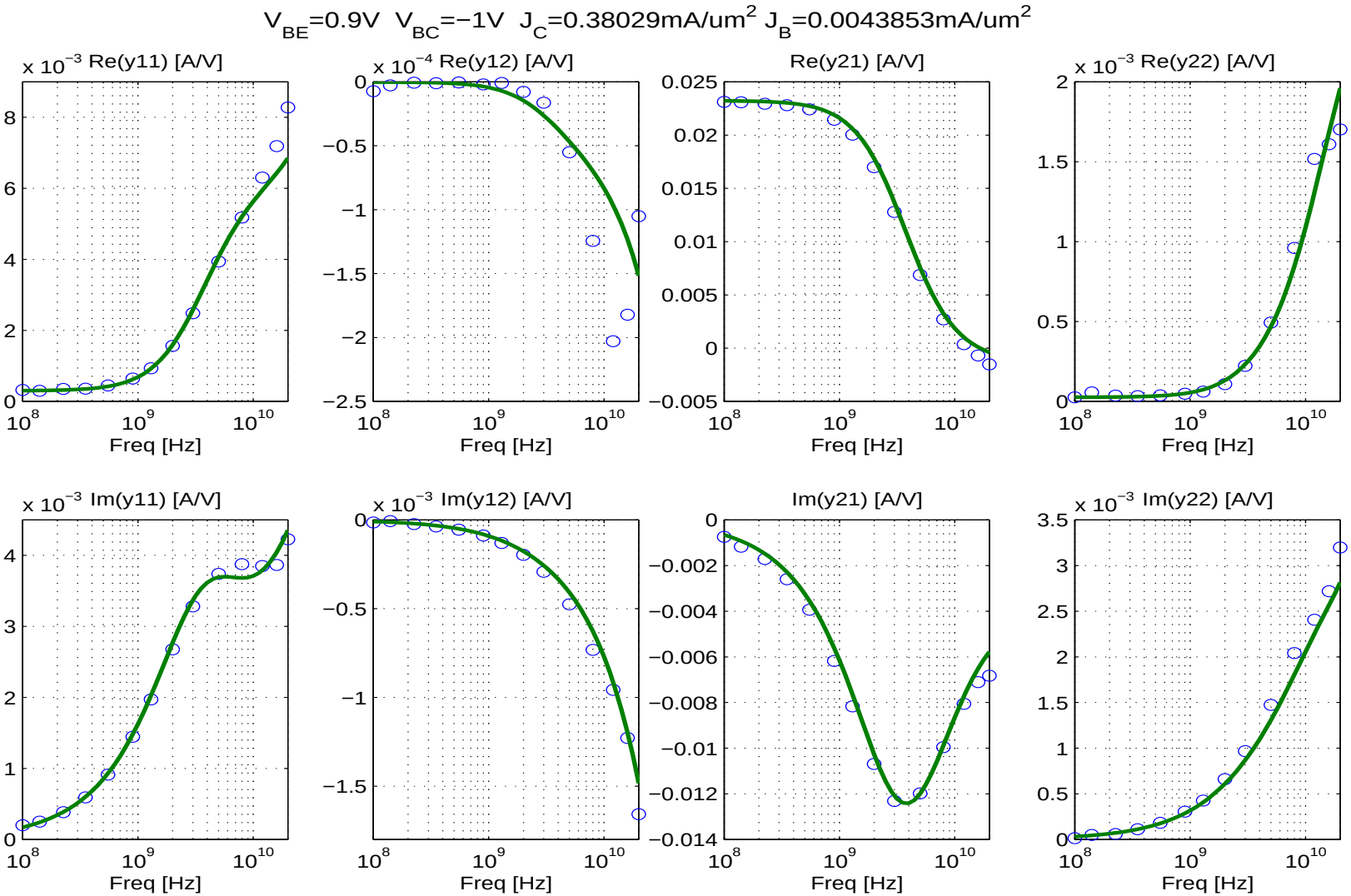
Note: real{y_{12}} is very small and usually of little practical interest, but can cause the modelled phase of y_{12} to deviate from measurements.



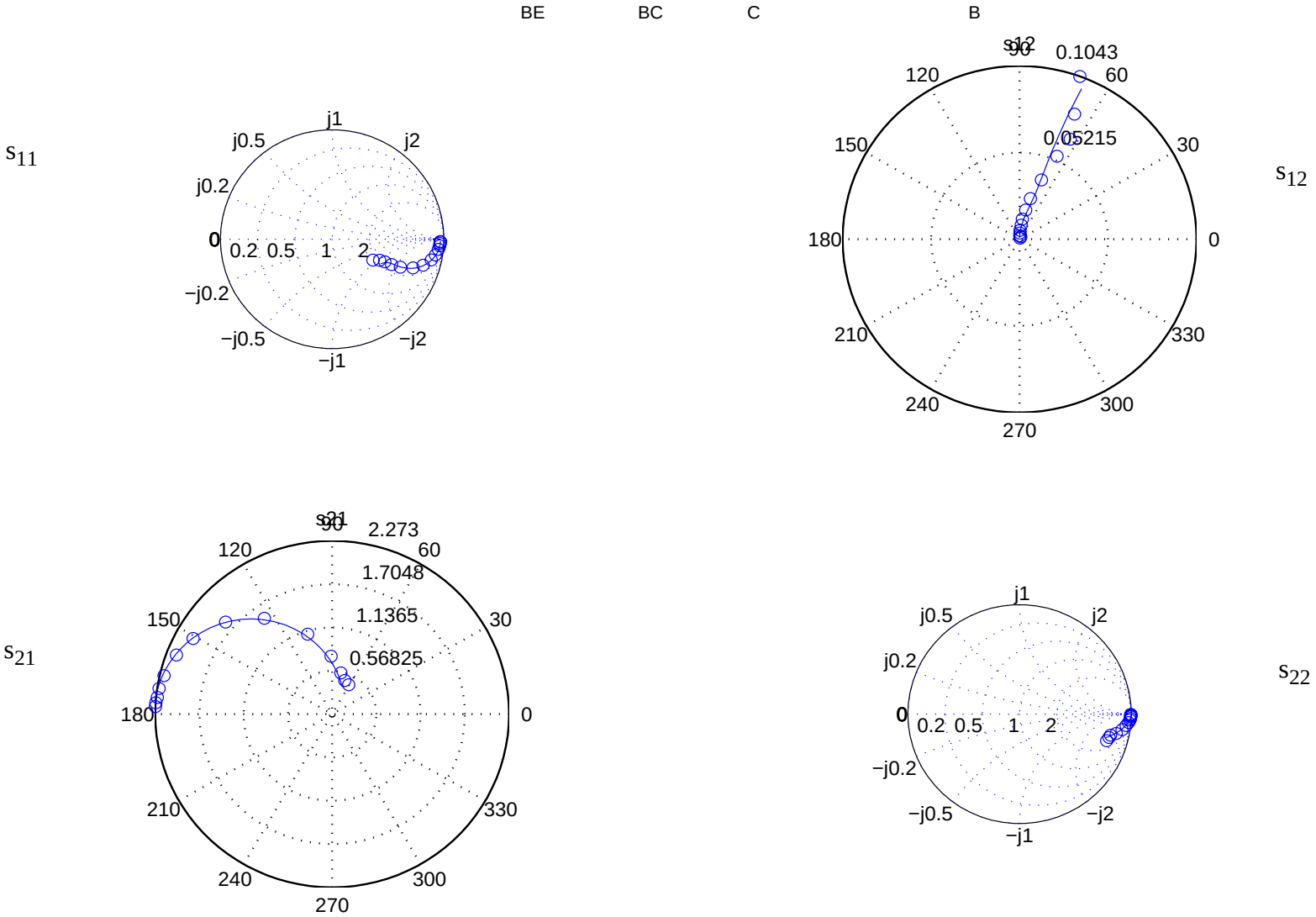
Frequency dependence of Y-parameters for a 12 GHz transistor (0.6*4.8µm^2) at I_C/A_E = 0.1mA/µm^2, V_{BC} = 0.5 V (cf. f_T curves): comparison between measurement (symbols) [4] and HICUM (lines). Single transistor parameter extraction.



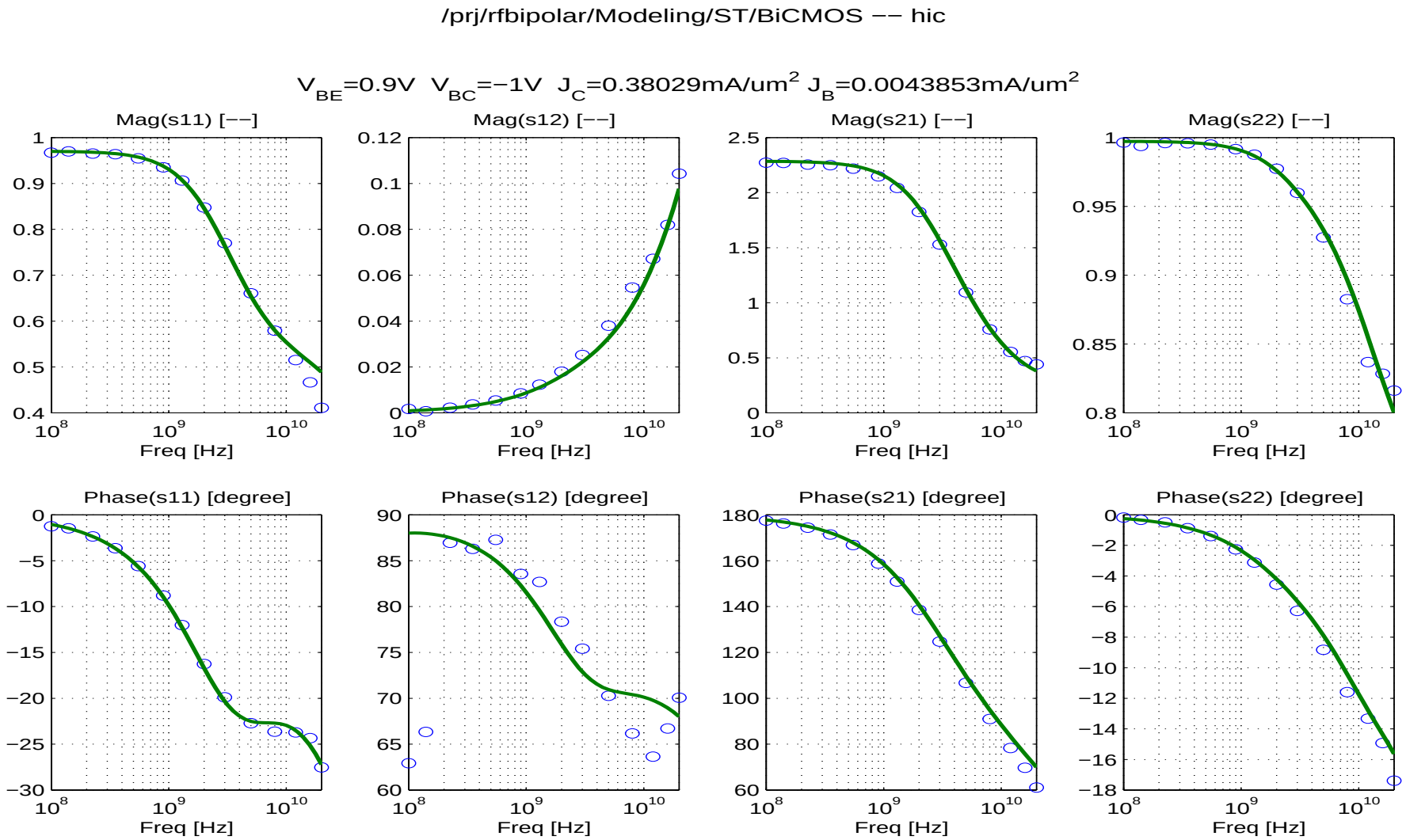
Frequency dependence of Y-parameters for a 12 GHz transistor ($0.6*4.8\mu m^2$) at $I_C/A_E = 0.34$ mA/μm^2, $V_{BC} = 0.5$ V (cf. f_T curves): comparison between measurement (symbols) [4] and HICUM (lines). Single transistor parameter extraction.



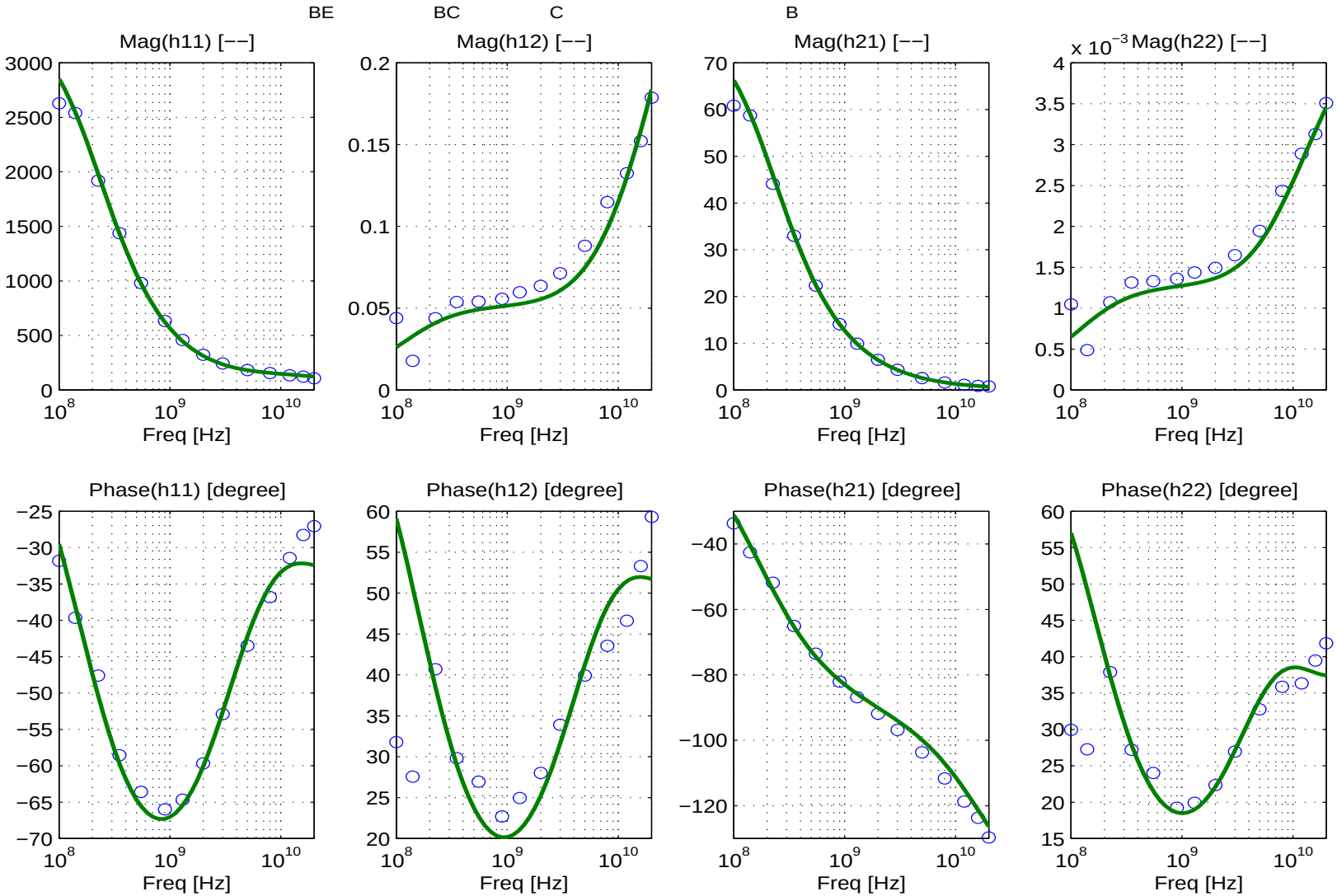
Frequency dependence of Y-parameters for a 12 GHz transistor (0.6*4.8µm^2) at I_C/A_E = 0.38 mA/µm^2, V_{BC} = -1 V (cf. f_T curves): comparison between measurement (symbols) [4] and HICUM (lines). Single transistor parameter extraction.



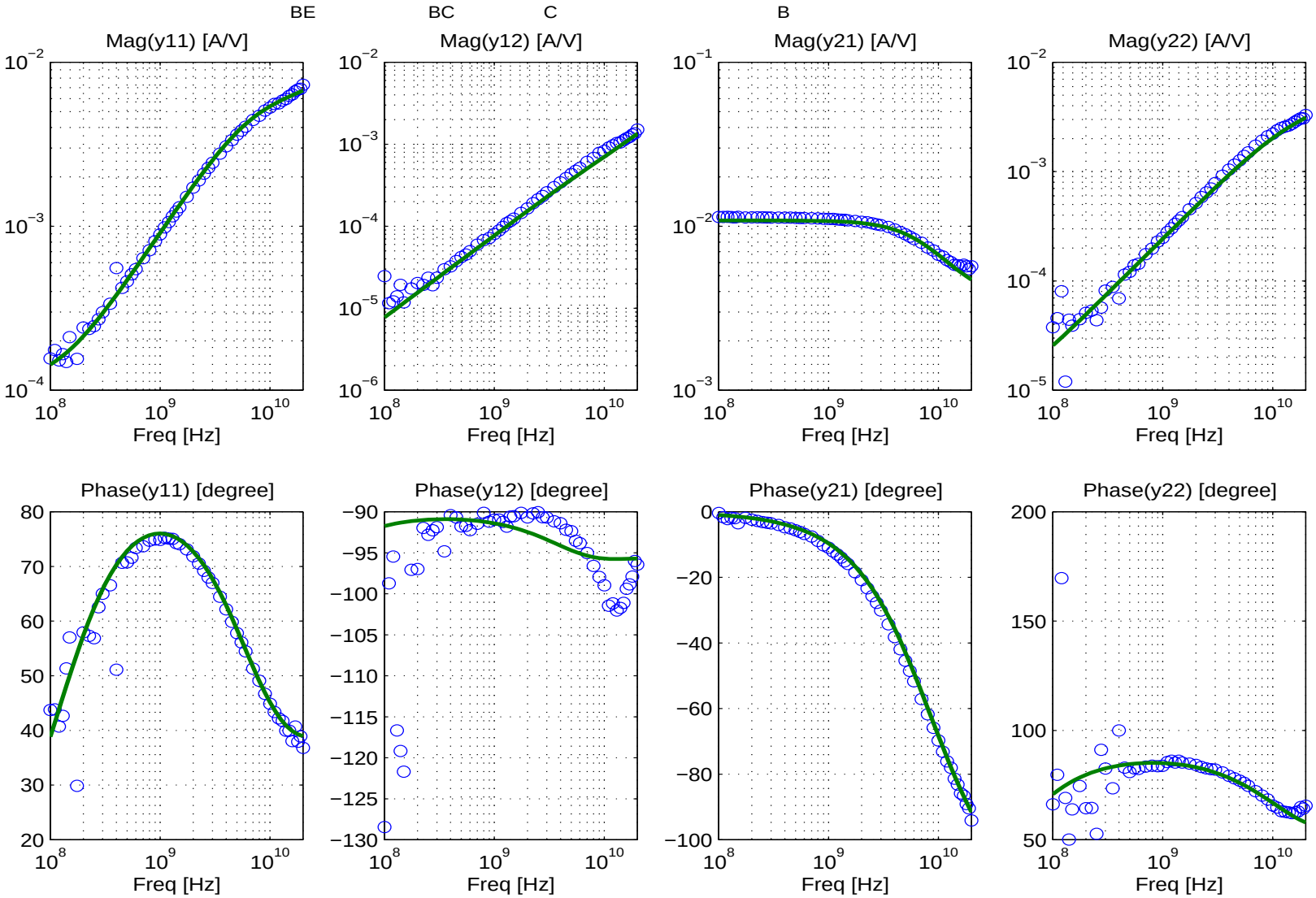
Frequency dependence of S-parameters (in Smith and polar chart) for a 12 GHz transistor ($0.6*4.8\mu m^2$) at I_C/A_E = 0.38 mA/μm^2, V_{BC} = -1 V (cf. f_T curves): comparison between measurement (symbols) [4] and HICUM (lines). Single transistor parameter extraction.



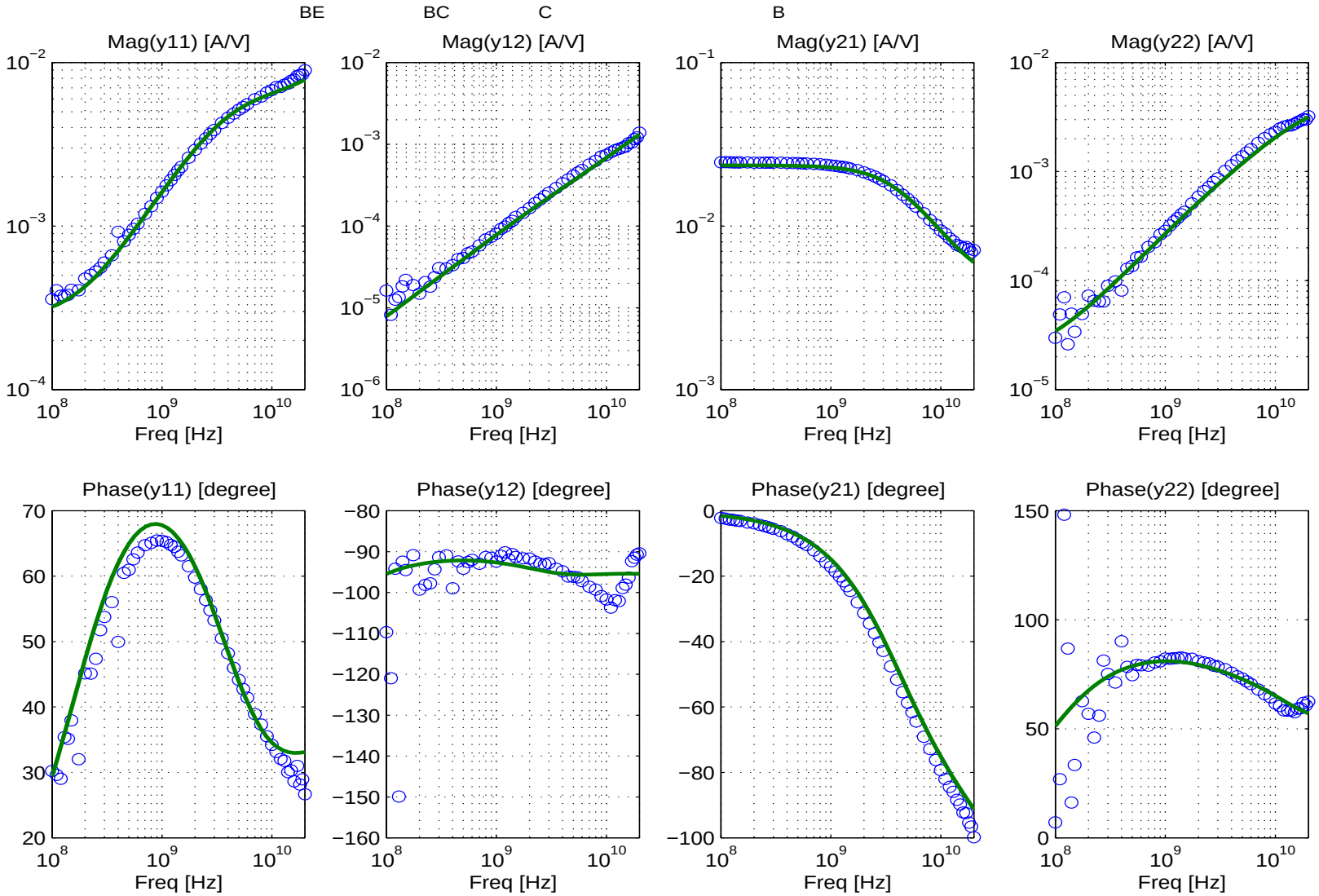
Frequency dependence of S-parameters (in magnitude and phase) for a 12 GHz transistor (0.6*4.8µm^2) at I_C/A_E = 0.38 mA/µm^2, V_{BC} = -1 V (cf. f_T curves): comparison between measurement (symbols) [4] and HICUM (lines). Single transistor parameter extraction.



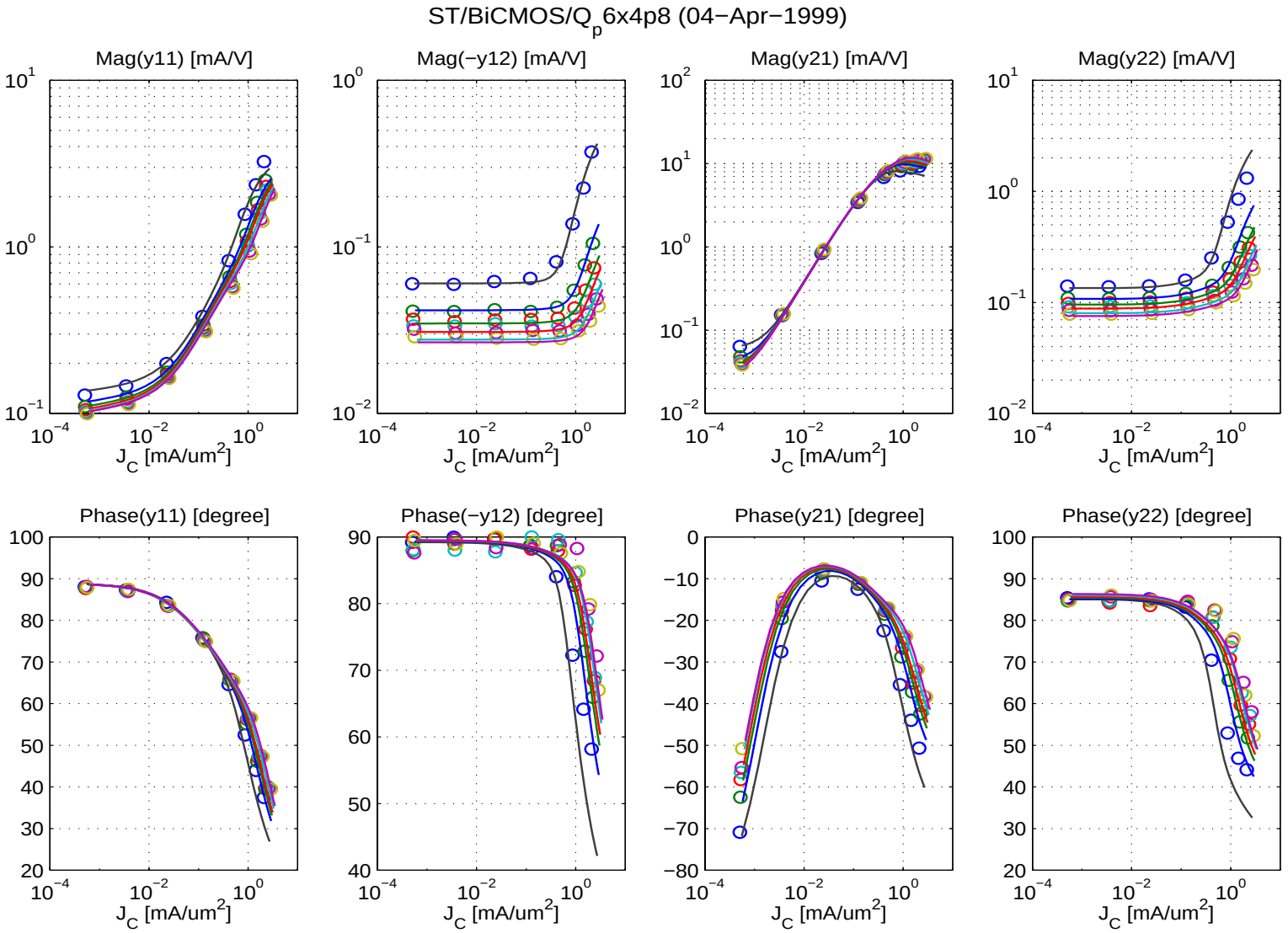
Frequency dependence of H-parameters for a 12 GHz transistor (0.6*4.8µm^2) at I_C/A_E = 0.38 mA/µm^2, V_{BC} = -1 V (cf. f_T curves): comparison between measurement (symbols) [4] and HICUM (lines). Single transistor parameter extraction.



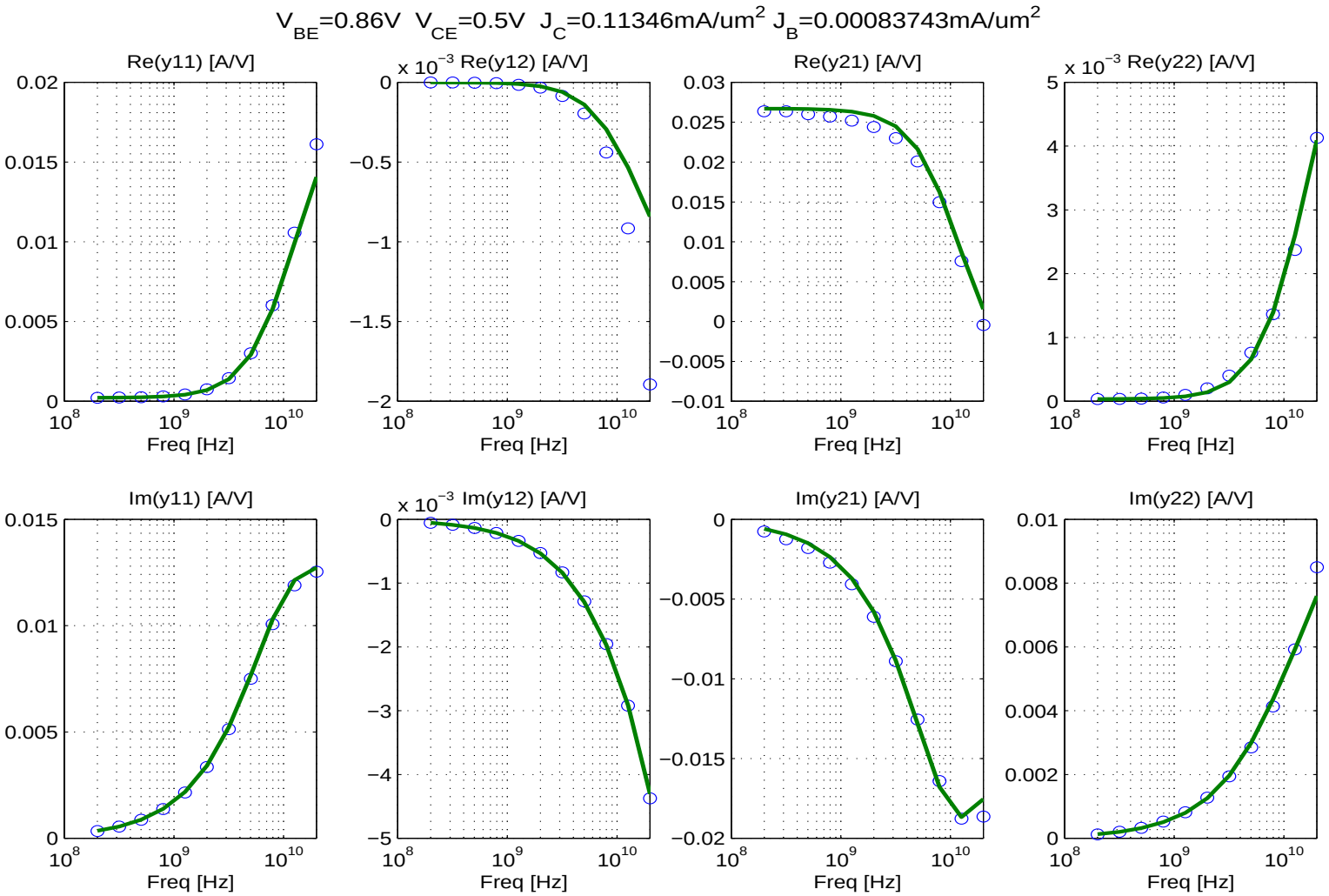
Frequency dependence of Y-parameters for a 12 GHz transistor (0.6*4.8µm^2) at I_C/A_E = 0.12 mA/µm^2, V_{BC} = -3 V (cf. f_T curves): comparison between measurement (symbols) [4] and HICUM (lines). Single transistor parameter extraction.



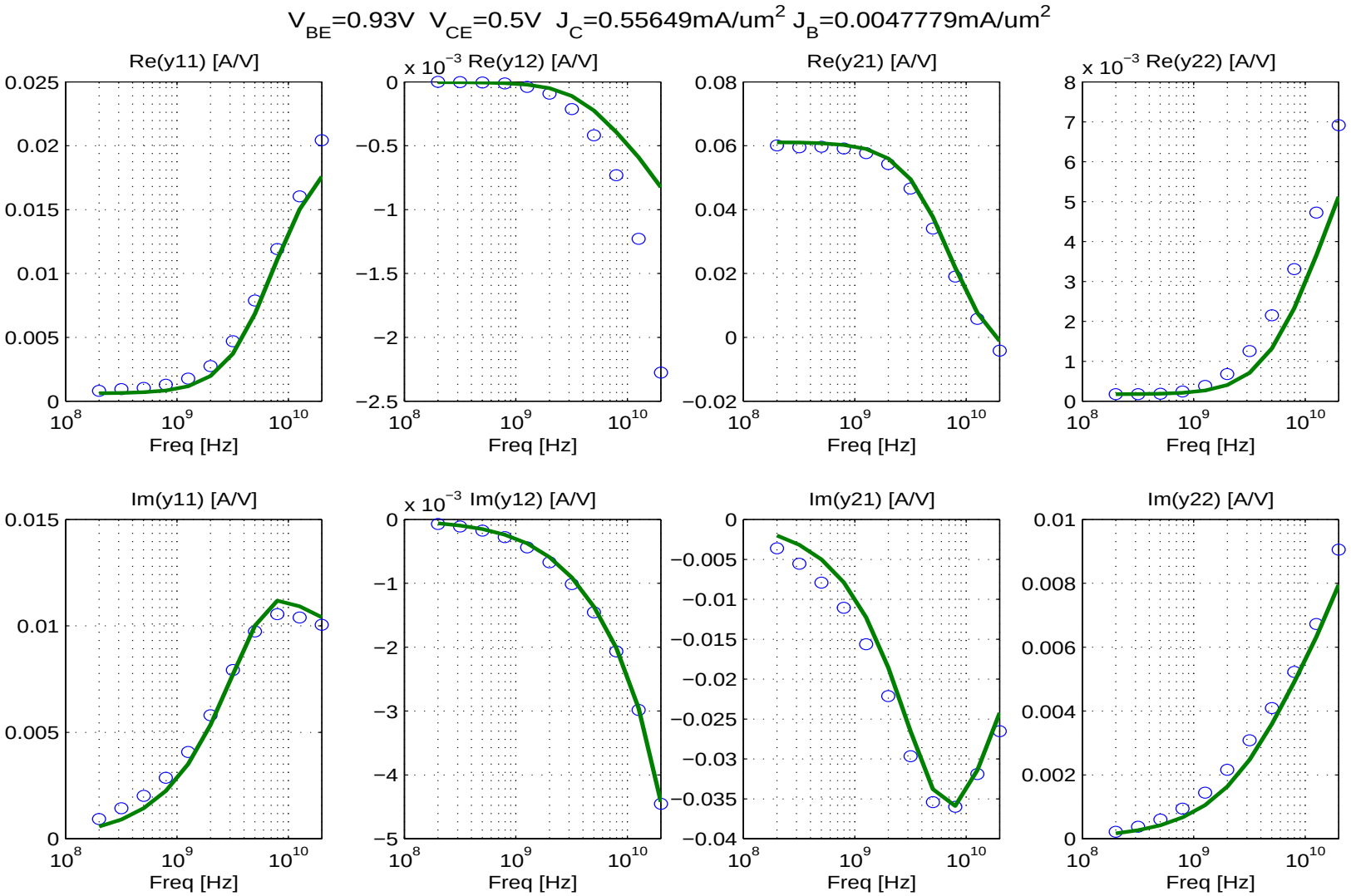
Frequency dependence of Y-parameters for a 12 GHz transistor ($0.6*4.8\mu m^2$) at $I_C/A_E = 0.425$ mA/μm^2, V_{BC} = -3 V (cf. f_T curves): comparison between measurement (symbols) [4] and HICUM (lines). Single transistor parameter extraction.



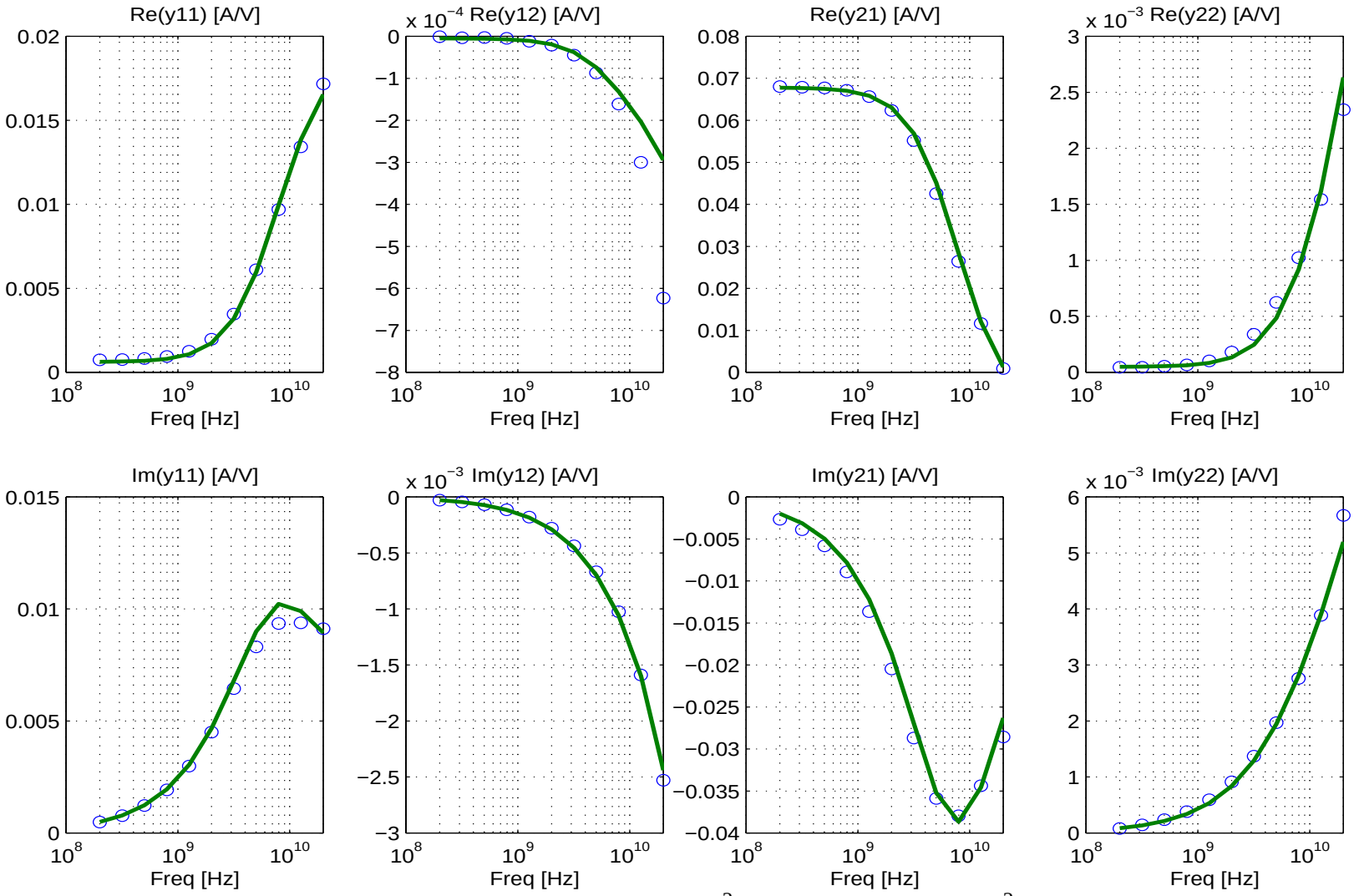
Y-parameters as a function of collector current density for a 12 GHz transistor ($0.6*4.8\mu m^2$) at f = 1GHz: comparison between measurement (symbols) and HICUM (lines). V_{CB}/V= -0.5, 0, 0.5, 2, 4.



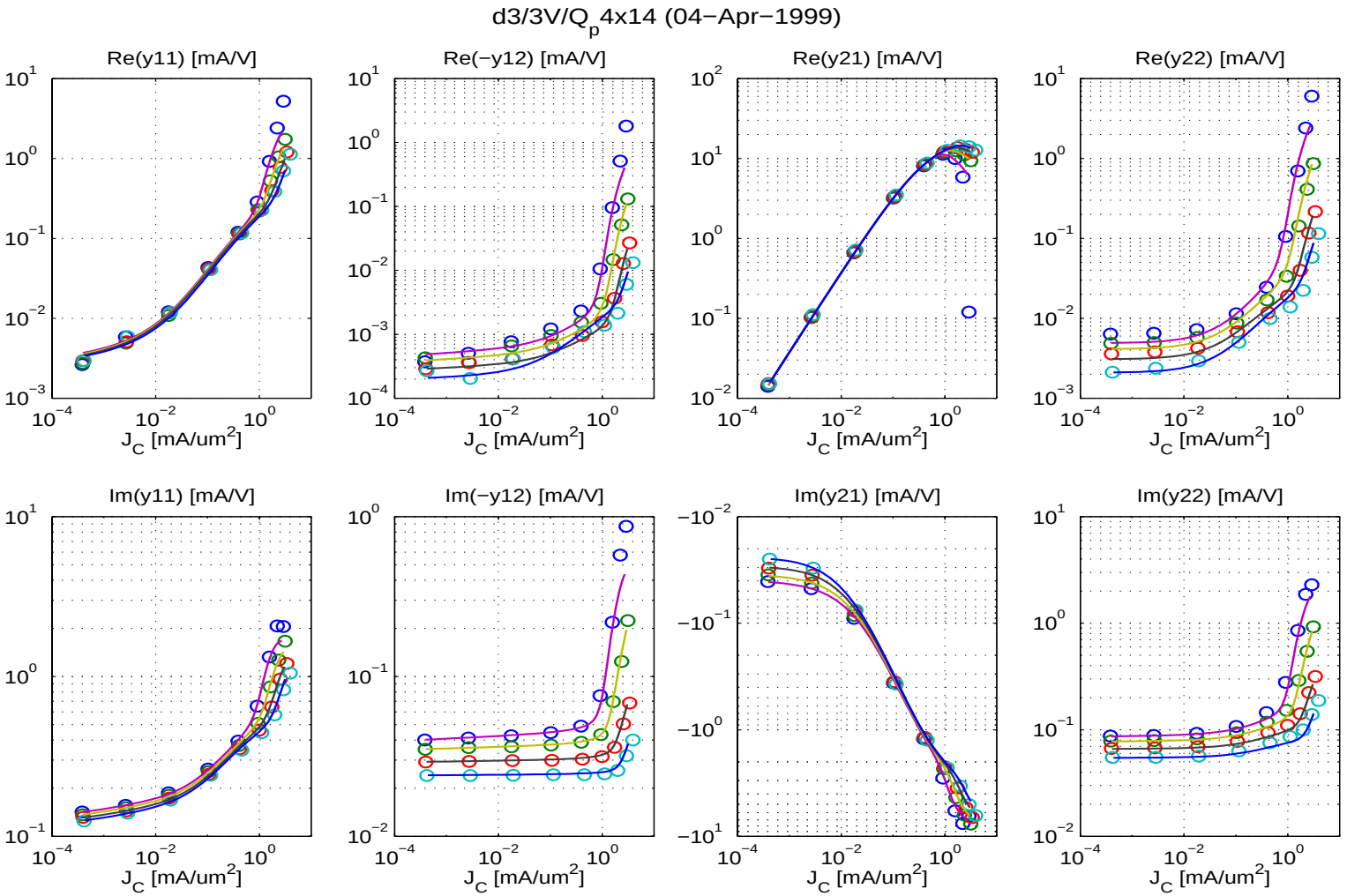
Frequency dependence of Y-parameters for a 25 GHz transistor (0.4*14µm^2) at I_C/A_E = 0.1 mA/µm^2, V_{CE} = 0.5 V (cf. f_T curves): comparison between measurement (symbols) and HICUM (lines).



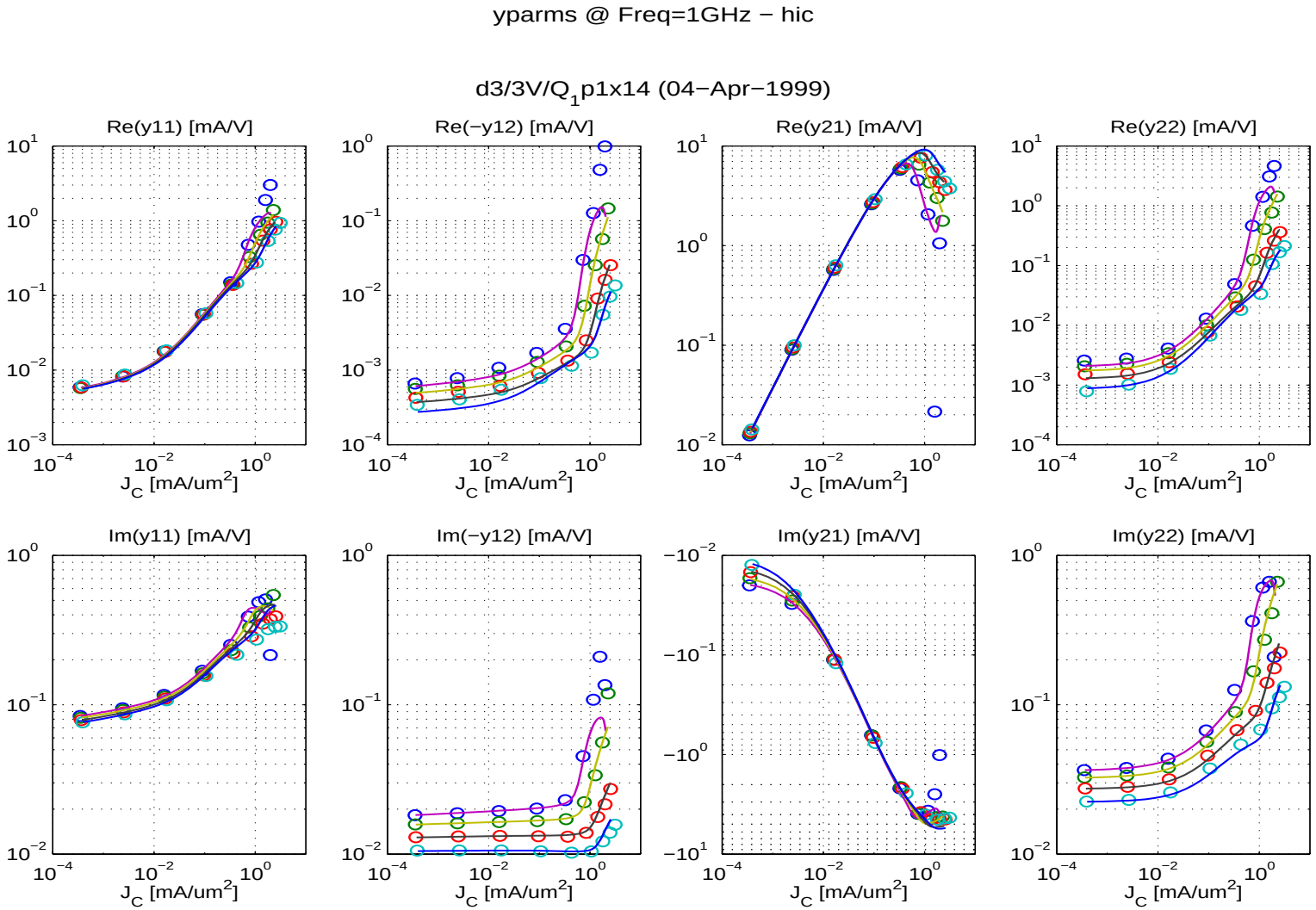
Frequency dependence of Y-parameters for a 25 GHz transistor (0.4*14µm^2) at I_C/A_E = 0.56 mA/µm^2, V_{CE} = 0.5 V (cf. f_T curves): comparison between measurement (symbols) and HICUM (lines).



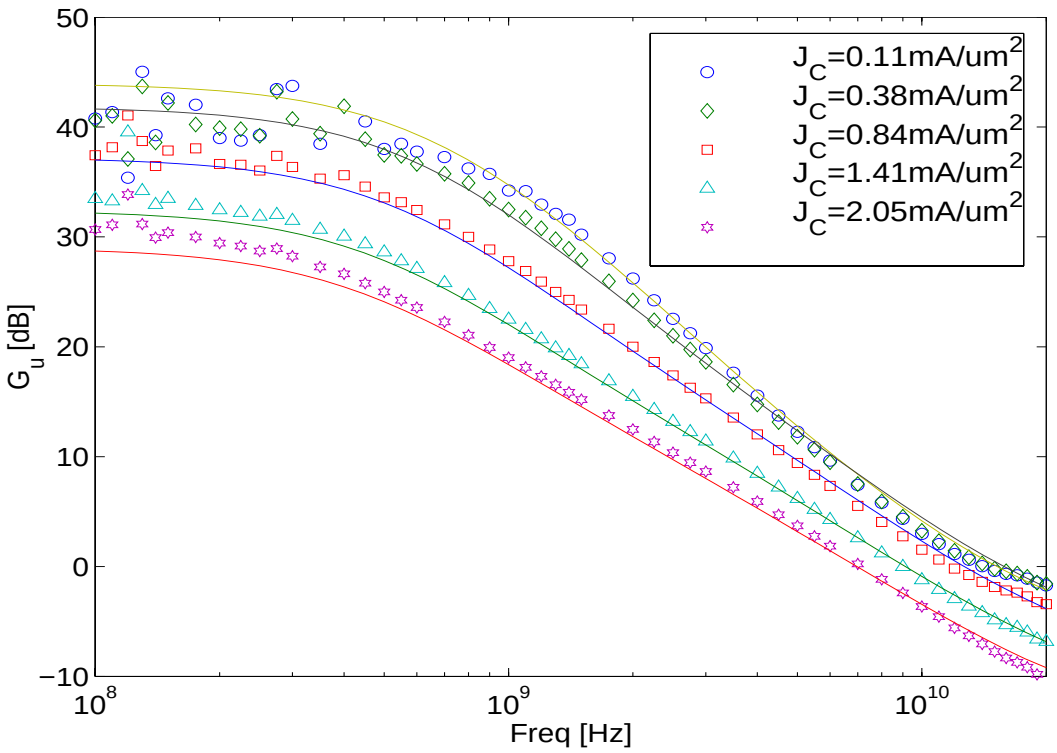
Frequency dependence of Y-parameters for a 25 GHz transistor (0.4*14µm^2) at I_C/A_E = 0.67 mA/µm^2, V_{CE} = 3 V (cf. f_T curves): comparison between measurement (symbols) and HICUM (lines).

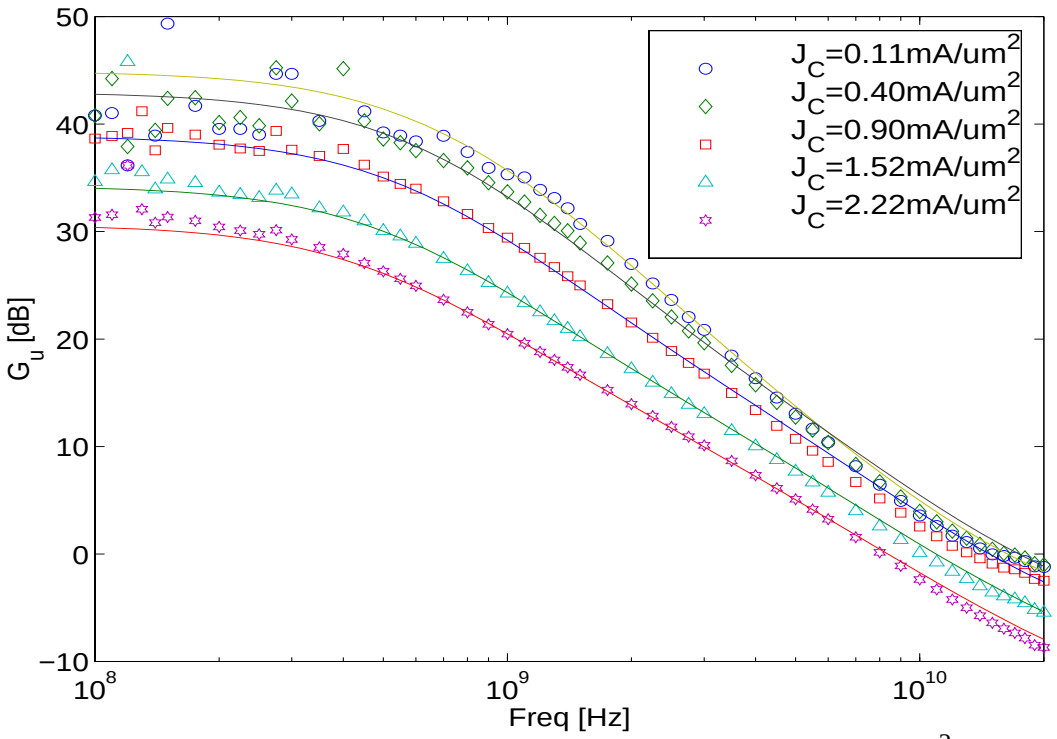


Y-parameters as a function of collector current density (V_{CE} = const.) for a 25 GHz transistor (0.4*14µm^2) at f = 1 GHz: comparison between measurement (symbols) and HICUM (lines). V_{CE}/V= 0.5, 0.8, 1.5, 3.

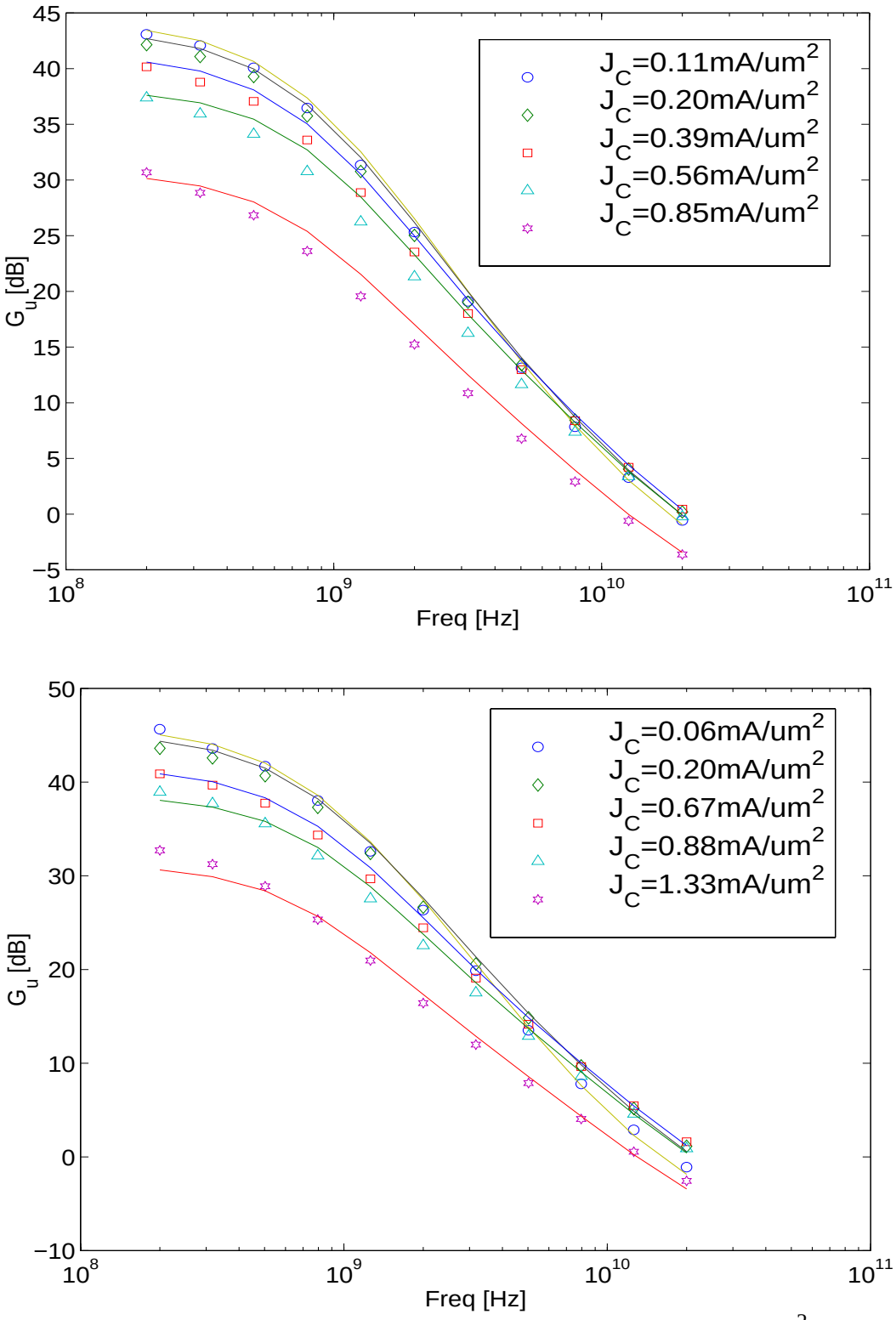


Y-parameters as a function of collector current density (V_{CE} = const.) for a 25 GHz transistor (1.2*14µm^2) at f = 1 GHz: comparison between measurement (symbols) and HICUM (lines). V_{CE}/V= 0.5, 0.8, 1.5, 3.





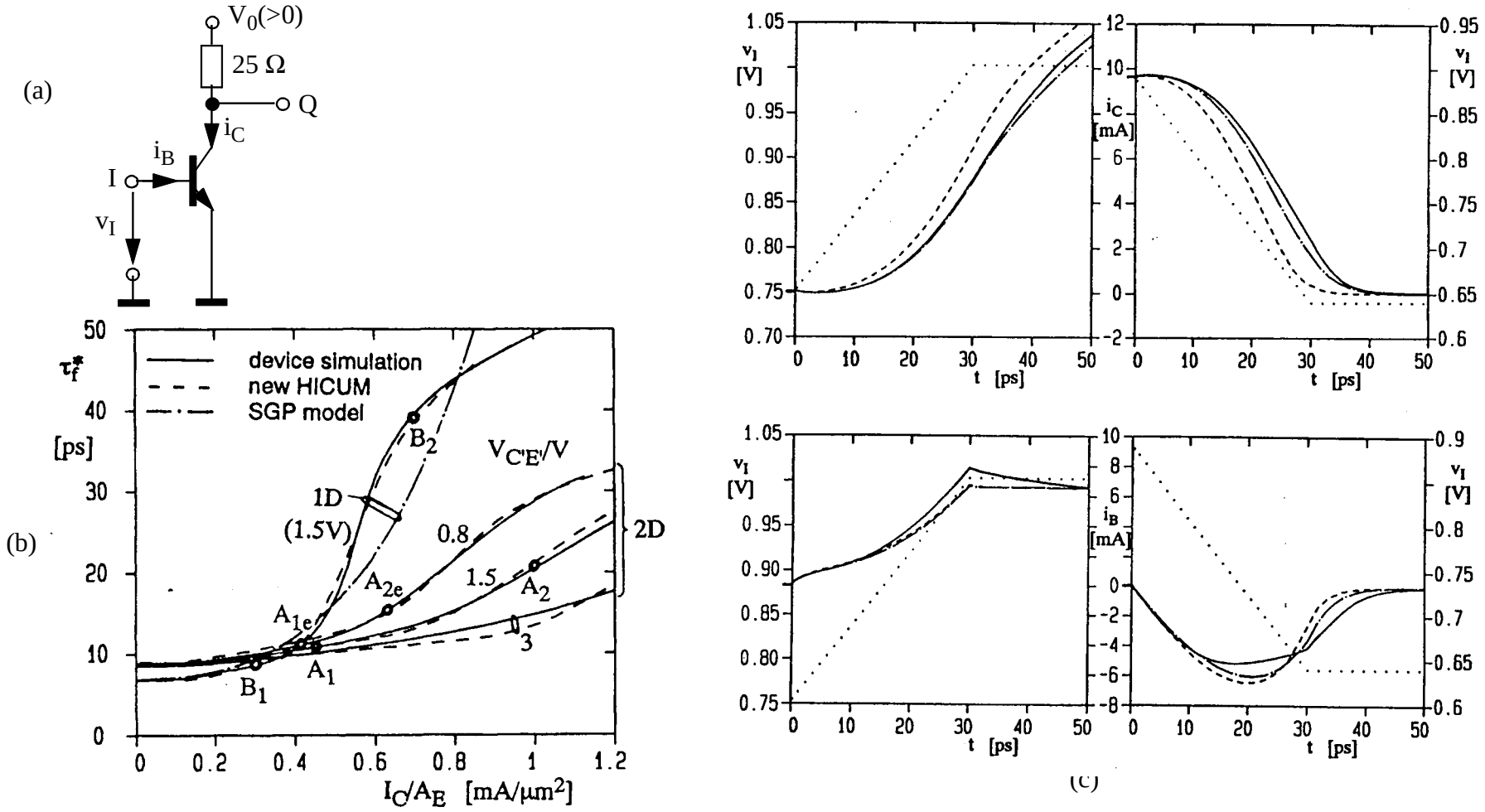
Unilateral gain G_U as a function of frequency for a 12 GHz transistor (0.6*4.8µm^2) at various bias points. Comparison between measurement (symbols) and HICUM (lines): (a) V_{BC} = -1 V; (b) V_{BC} = -2 V. Note the high accuracy even at current densities far beyond I_C/A_E(@peak f_T).



Unilateral gain G_U as a function of frequency for a 25 GHz transistor (0.4*14µm^2) at various bias points. Comparison between measurement (symbols) and HICUM (lines): (a) V_{CE} = 0.5 V; (b) V_{CE} = 0.8 V. Note the high accuracy even at current densities far beyond I_C/A_E(@peak f_T).

6.4 High-speed transient (switching) operation

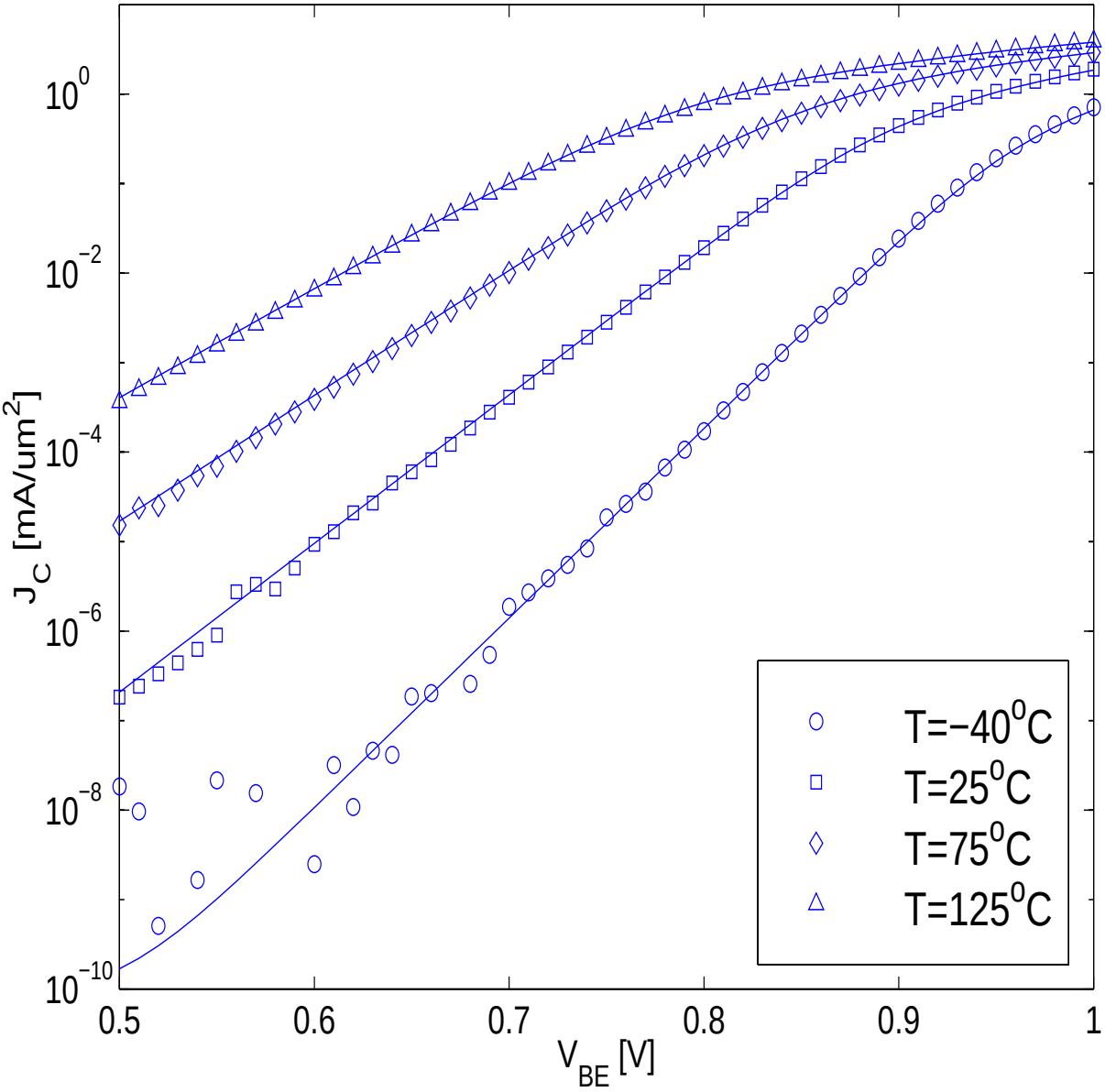
(2D mixed-mode device/circuit simulation [37]; for experimental results of an older process see [25])



(a) Transistor inverter (worst-case for switching behaviour comparison). (b) Transit time vs. collector current density of a 14 GHz bipolar transistor. (c) Switching-on and -off behavior for i_C (top) and i_B (bottom) into and out of, respectively, the bias point A_2 in Fig. (b). Comparison between device simulation (solid lines), HICUM with NQS effects (dash-dotted lines), and HICUM without NQS effects (dashed lines) [37].

6.5 Temperature dependence

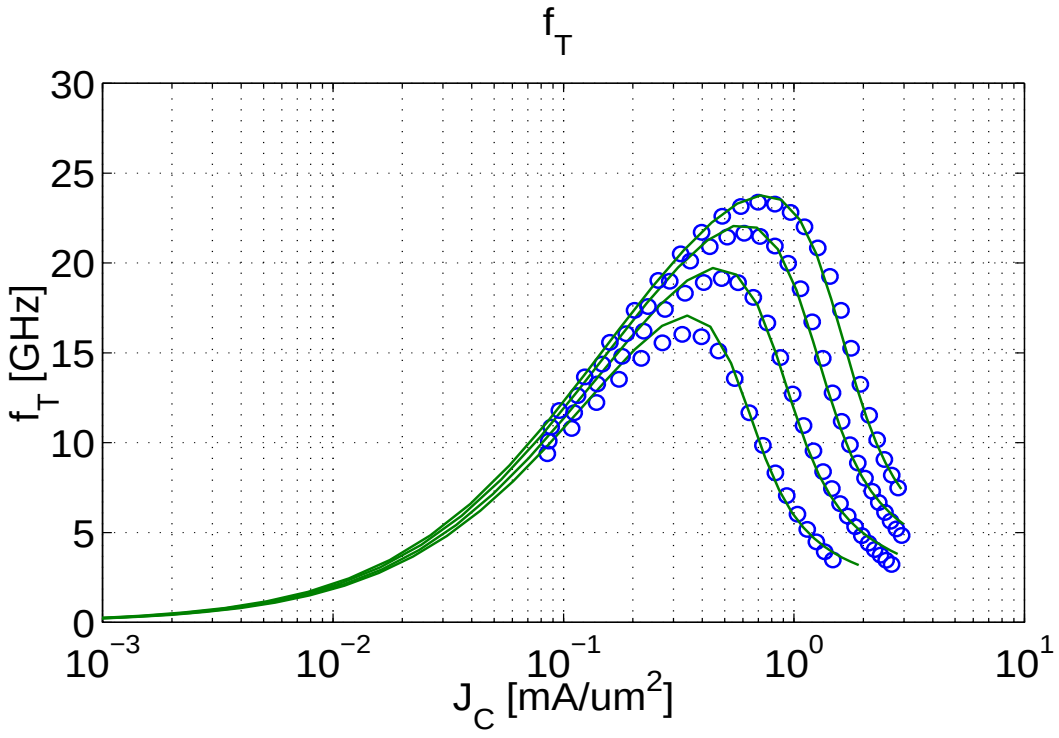
6.5.1 DC characteristics



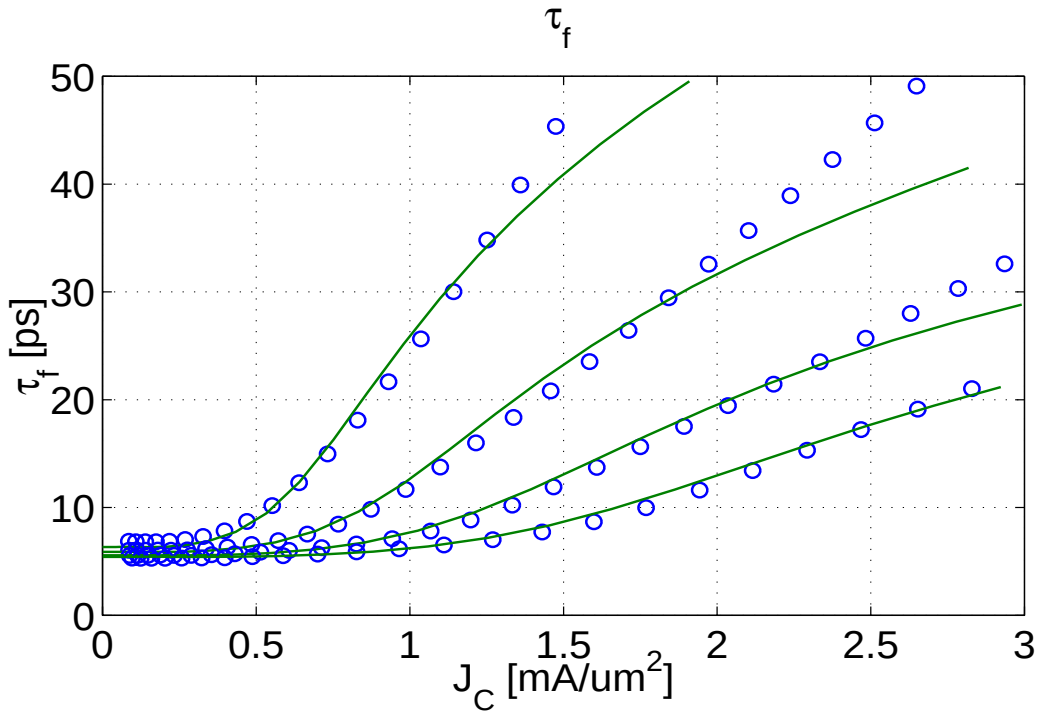
Comparison between measurement (symbols) and HICUM (solid lines) for a 25 GHz bipolar transistor: collector current density I_C/A_E vs. V_{BE} for different temperatures. Emitter size: 0.4*14 µm^2; V_{BC} = 0 V.

6.5.2 AC characteristics

(a)



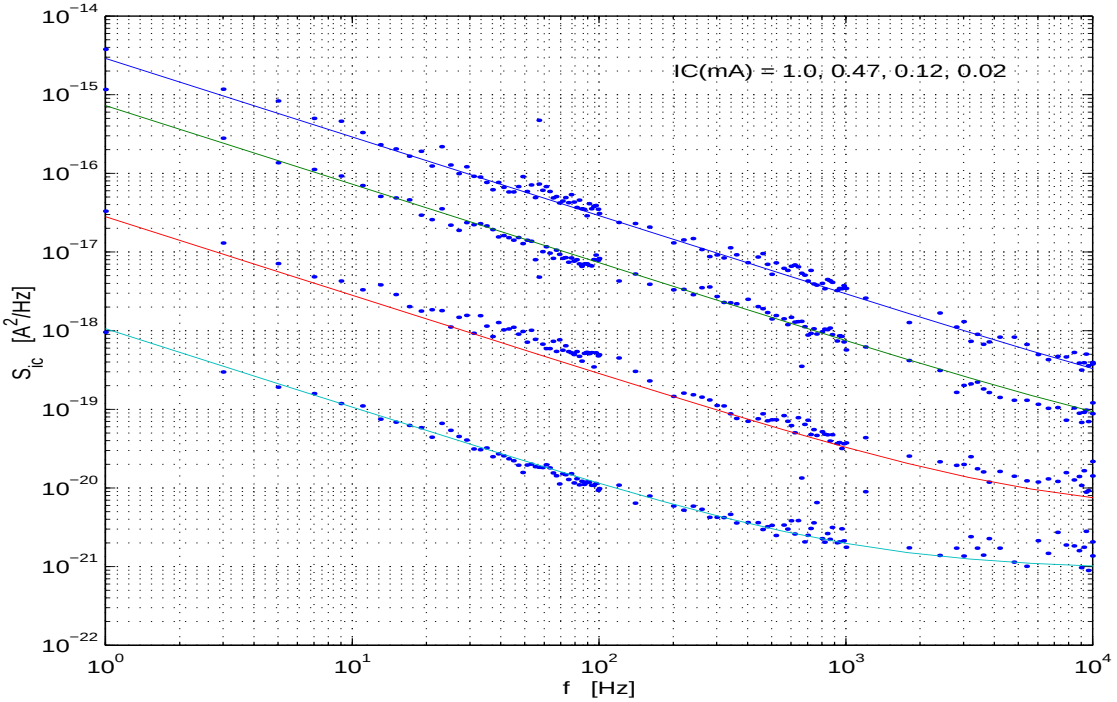
(b)



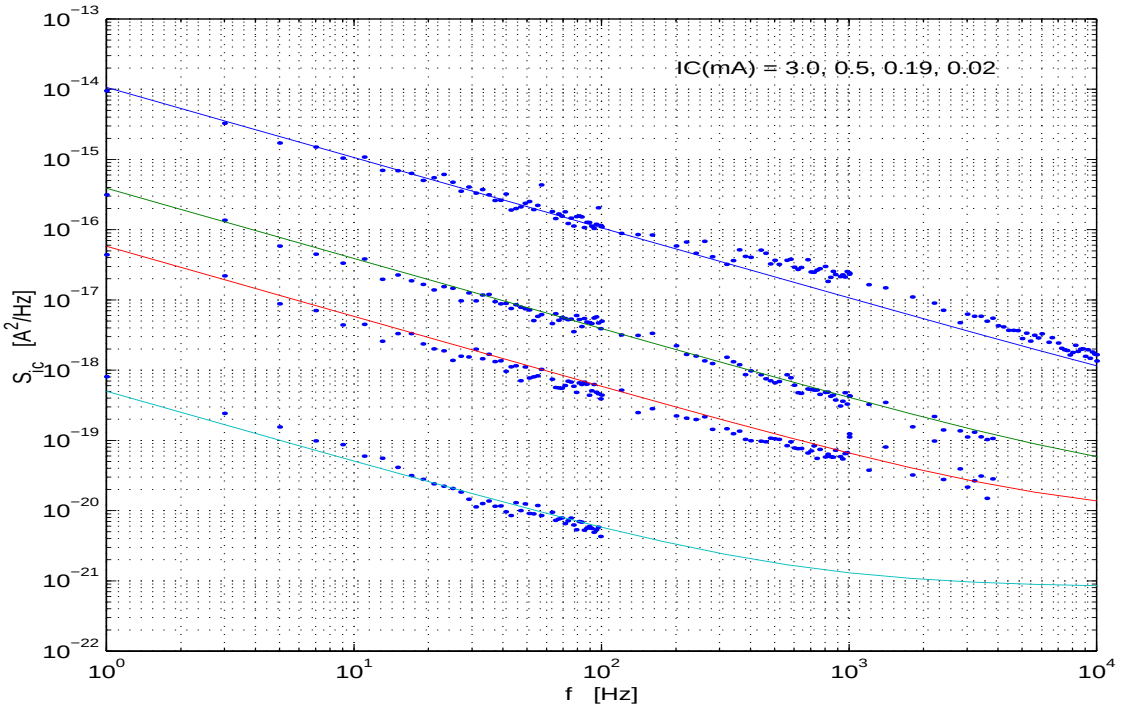
(a) Transit time and (b) transit frequency vs. I_C/A_E for T = 125 C: comparison between measurement (symbols) and HICUM (solid lines) [41]. Emitter size: 0.4*14 µm^2; V_{CE}/V = 0.5,0.8,1.5,3. Note, that the results were generated with a single model parameter set, except for the temperature coefficients of τ_0.

6.6 Low-frequency noise

(a)



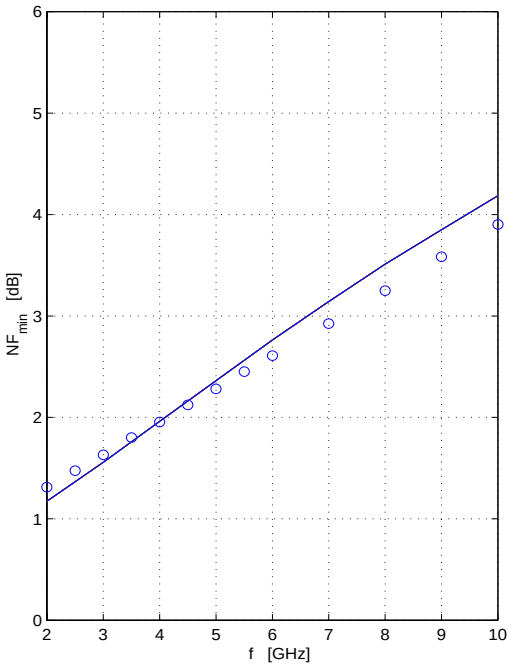
b)

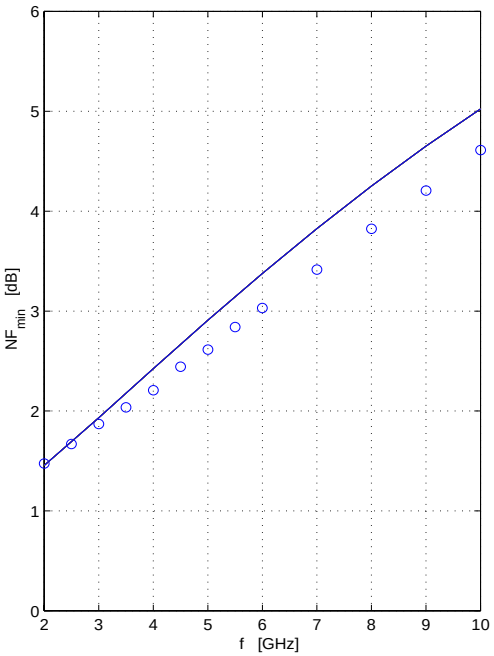


Collector current noise spectral density S_{iC} vs. frequency f for 25 GHz transistors at T = 25 C and various bias points I_C (cf. insert) and V_{CE} = 1 V. Comparison between measurement (symbols) and HICUM (lines): (a) A_{E0} = 0.4*14µm^2, (b) A_{E0} = 0.8*14µm^2.

6.7 High-frequency noise

(a)

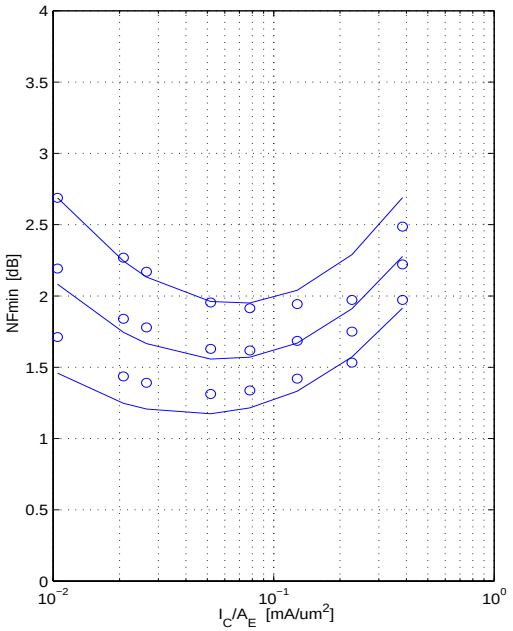


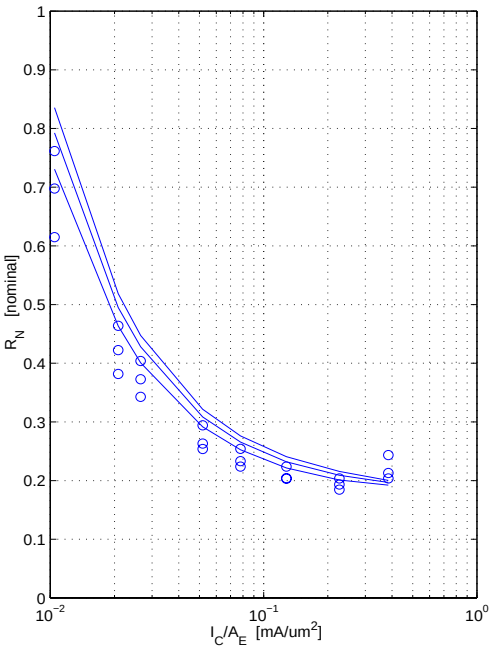


(b)

Minimum noise figure F_{min} vs. frequency f for a 25 GHz transistor. Comparison between measurement (symbols) and HICUM (lines): (a) emitter size is 4*0.4*21µm^2, I_C/A_E = 0.405mA/µm^2, V_{CE} = 1V; (b) emitter size is 0.8*14µm^2, I_C/A_E = 0.03mA/µm^2, V_{CE} = 1V.

(a)





(b)

Comparison between measurement (symbols) and HICUM (lines) for a 25 GHz transistor (4*0.4*21µm^2): (a) Minimum noise figure F_{min} vs. collector current density I_C/A_E; (b) equivalent noise resistance R_n vs. collector current density. f/GHz = 1, 2, 3; V_{CE} = 1V.

6.8 High-frequency distortion

Some general remarks are required for explaining and understanding the distortion results.

The transistors were measured on-wafer in a 50Ω system using the same h.f. pad configuration that is employed for small-signal S-parameter measurements. An automated measurement system was set-up which facilitates bias point sweeps [19,43,44]. The system was carefully calibrated in order to take into account all losses up to the device and to accurately obtain both output power P_{in} and input power P_{out} at the transistor terminals for all relevant frequencies. Single-tone measurements were performed at four different fundamental frequencies f_1/GHz = (0.05, 0.1, 0.9, 1.8). The two low frequencies at 50 and 100 MHz were chosen to be able to separate later the cause of nonlinearities during model comparison. The following table shows the relation between P_{in} specified in dBm by the power sweeper (defined for a 50Ω load) and the respective voltage amplitude.

P [dBm]	-40	-30	-20	-10
$\hat{v}$ [V]	6.4	20	64	200

As response at the output, the signals at the respective fundamental frequency as well as the second and third harmonic frequency (f_2 and f_3) were measured with a spectrum analyser for different transistor types. The table below lists the frequencies that belong together. The resulting P_{out} at the various frequencies can then be compared to model characteristics as a function of d.c. bias and geometry. Figures of merit, such as the 1dB compression point and harmonic distortion, can also be calculated.

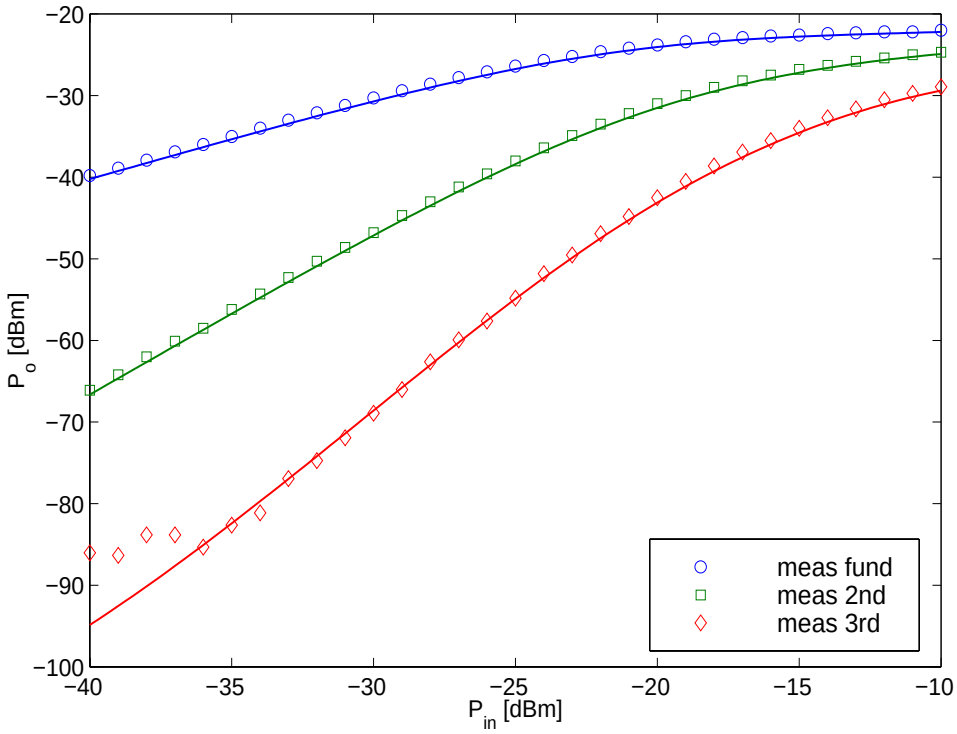
f_1/GHz	0.05	0.1	0.9	1.8
f_2/GHz	0.1	0.2	1.9	3.6
f_3/GHz	0.15	0.3	2.7	5.4

For circuit simulation, the periodic steady-state method available in SPECTRE-RF was used. However, time-domain based simulators seem to generate an incorrect d.c. component (probably converted from the second harmonic) at the transistor input, which causes the d.c. bias point to run

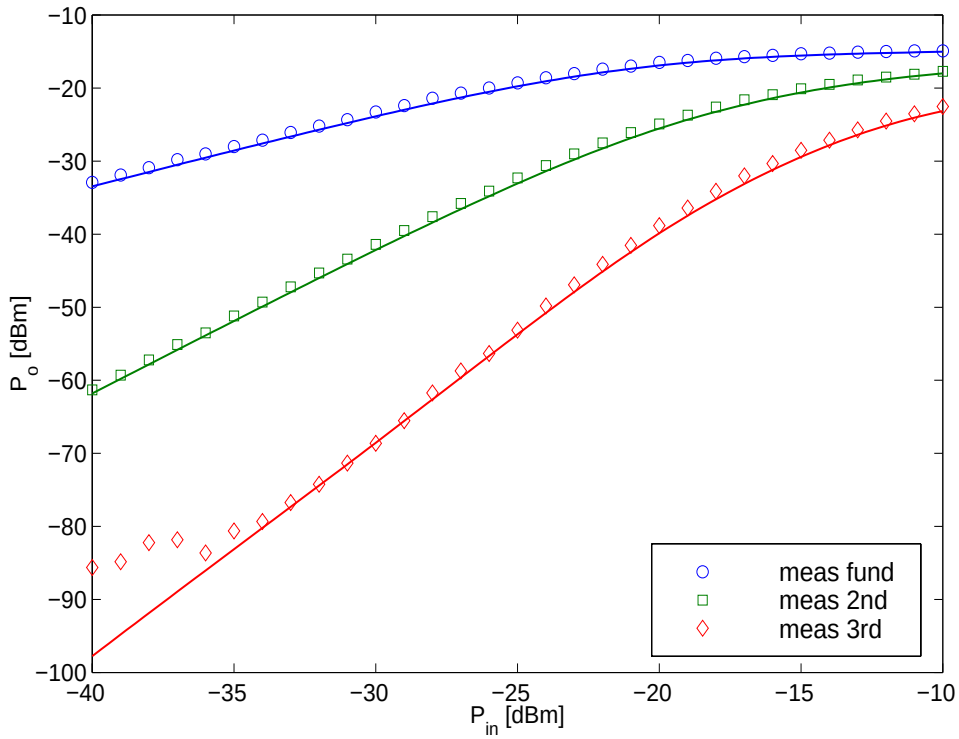
away at high input power. This (probably) numerical effect, which should not occur according to the measurement set-up, was not observed during harmonic balance simulations (using HP-MDS) with the same circuit and parameters. A corresponding correction algorithm was developed and implemented in MATLAB, the results of which were verified by HP-MDS.

For logistical reasons the measurements were carried out on a different die of the same wafer the parameter extraction was performed on. Process variations across the wafer might cause slightly increased deviations between model and measurements. Nevertheless, the model still turned out to be quite accurate.

(a)

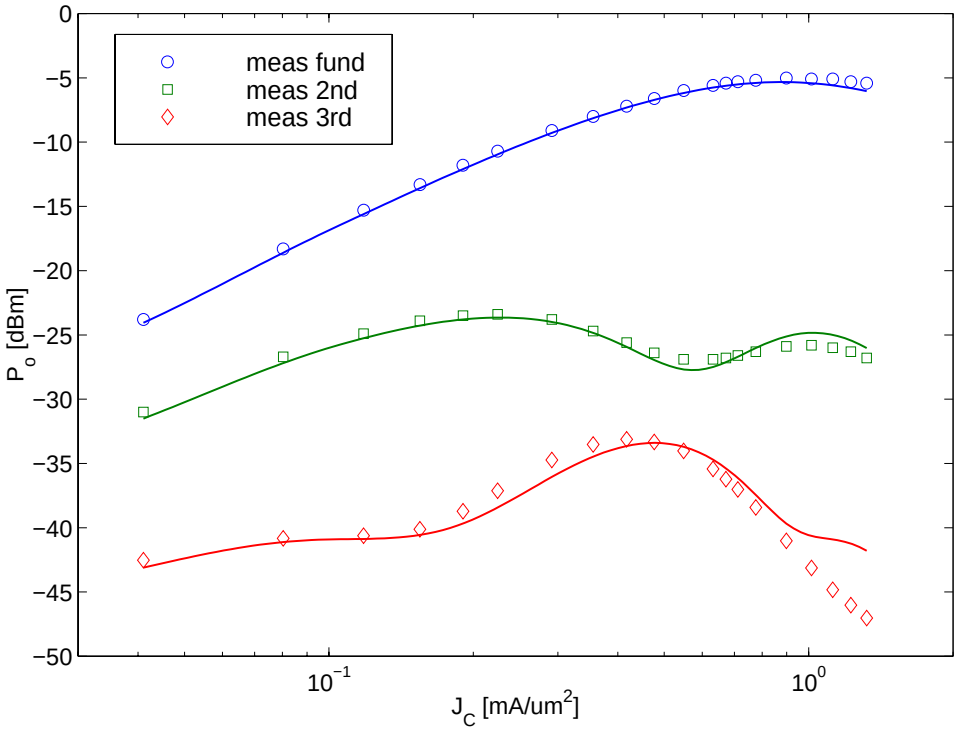


(b)

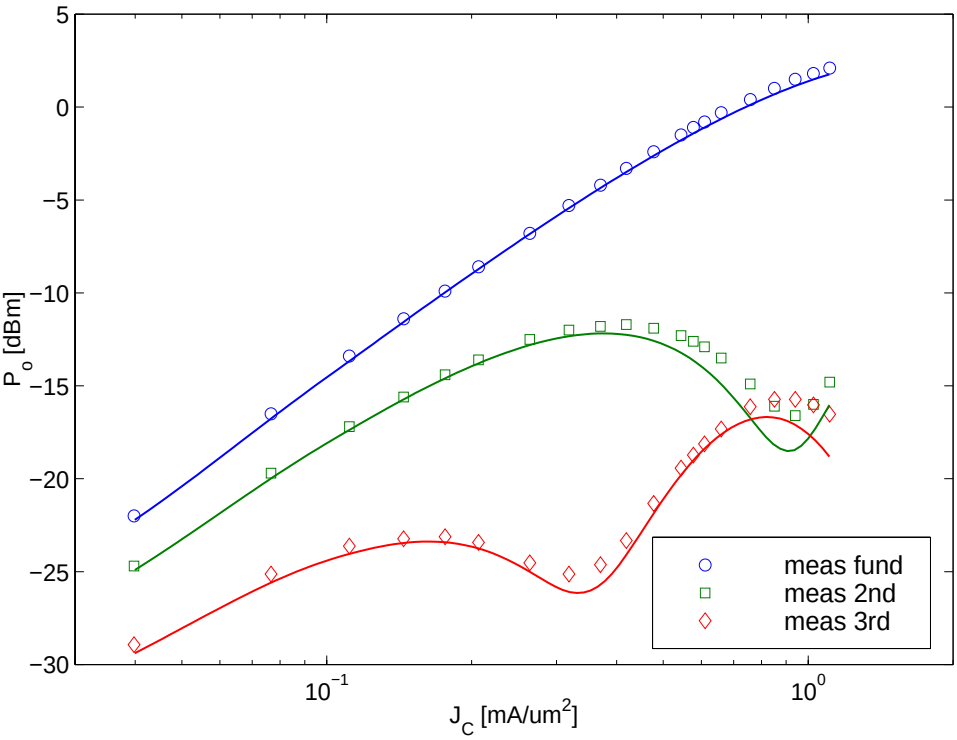


P_{out} vs. P_{in} for f_0 = 0.9 GHz; comparison between measurement (symbols) and HICUM (lines):
(a) 10 GHz (power) transistor (0.4*14µm^2) at I_C/A_E = 0.05 mA/µm^2, V_{CE} = 0.8 V;
(b) 25 GHz transistor (0.4*14µm^2) at I_C/A_E = 0.13 mA/µm^2, V_{CE} = 3 V.

(a)

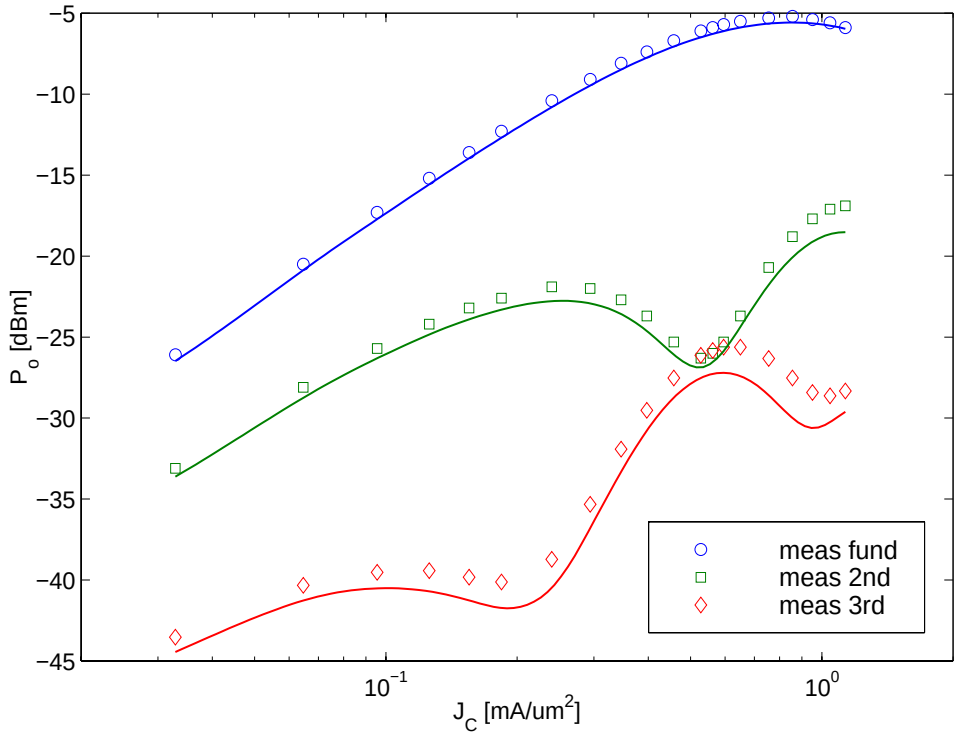


(b)

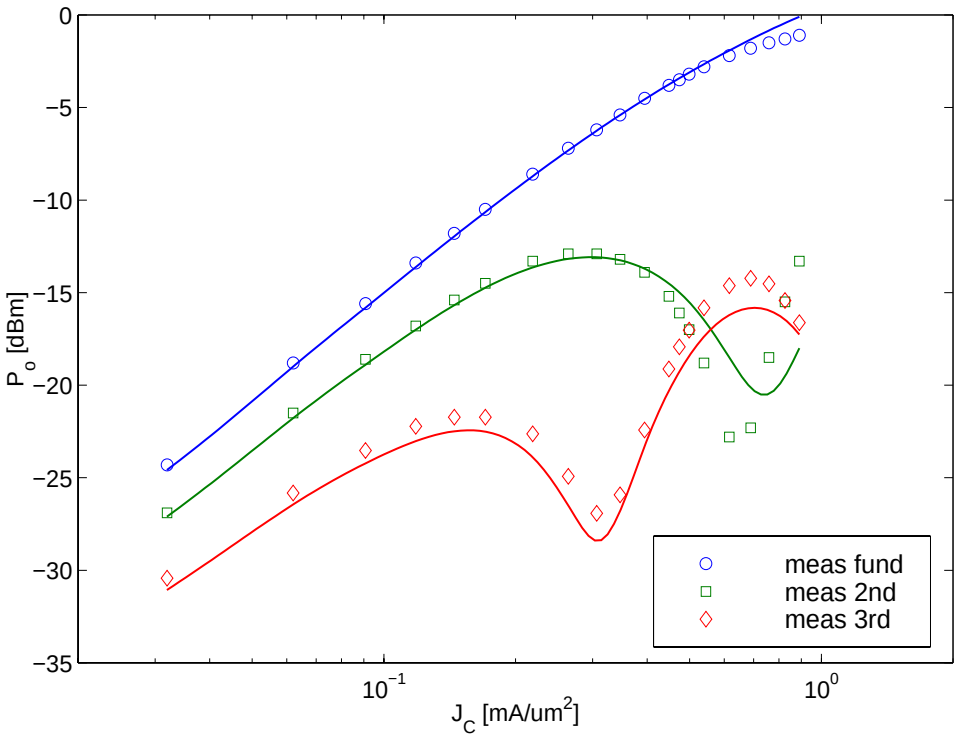


P_{out} vs. collector current density I_C/A_E at f_0 = 0.9 GHz for a 10 GHz (power) transistor (0.4*14µm^2); comparison between measurement (symbols) and HICUM (lines):
(a) P_{in} = -20 dBm; (b) P_{in} = -10 dBm. V_{CE} = 0.8 V.

(a)

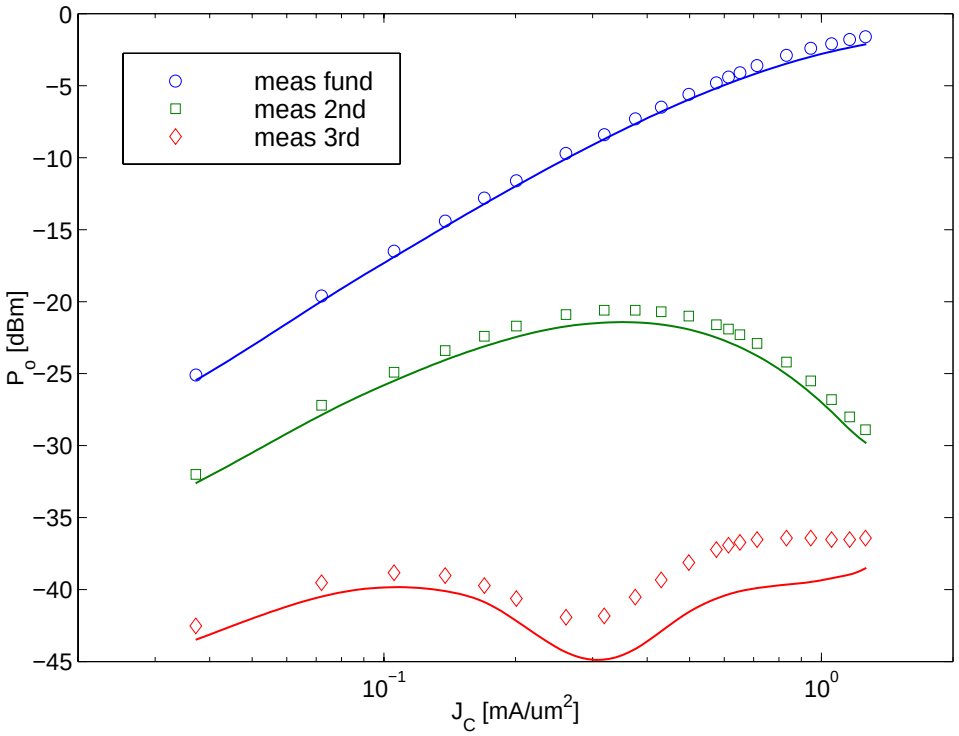


(b)

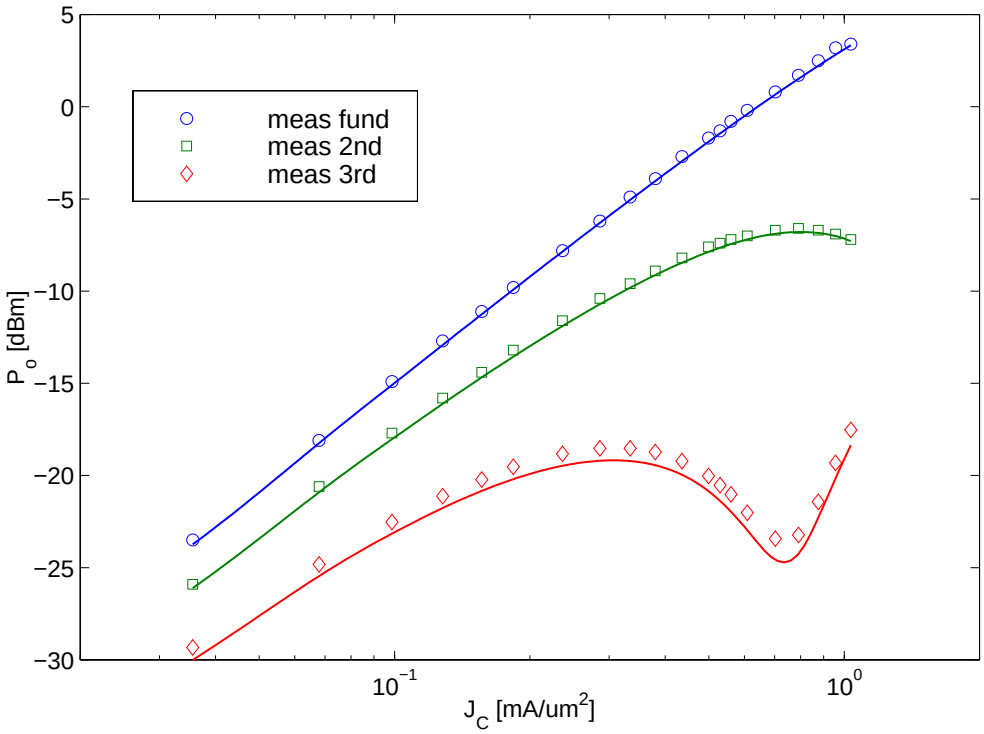


P_{out} vs. collector current density I_C/A_E at f_0 = 0.9 GHz for a 25 GHz transistor (0.4*14µm^2); comparison between measurement (symbols) and HICUM (lines):
(a) P_{in} = -20 dBm; (b) P_{in} = -10 dBm. V_{CE} = 0.5 V.

(a)

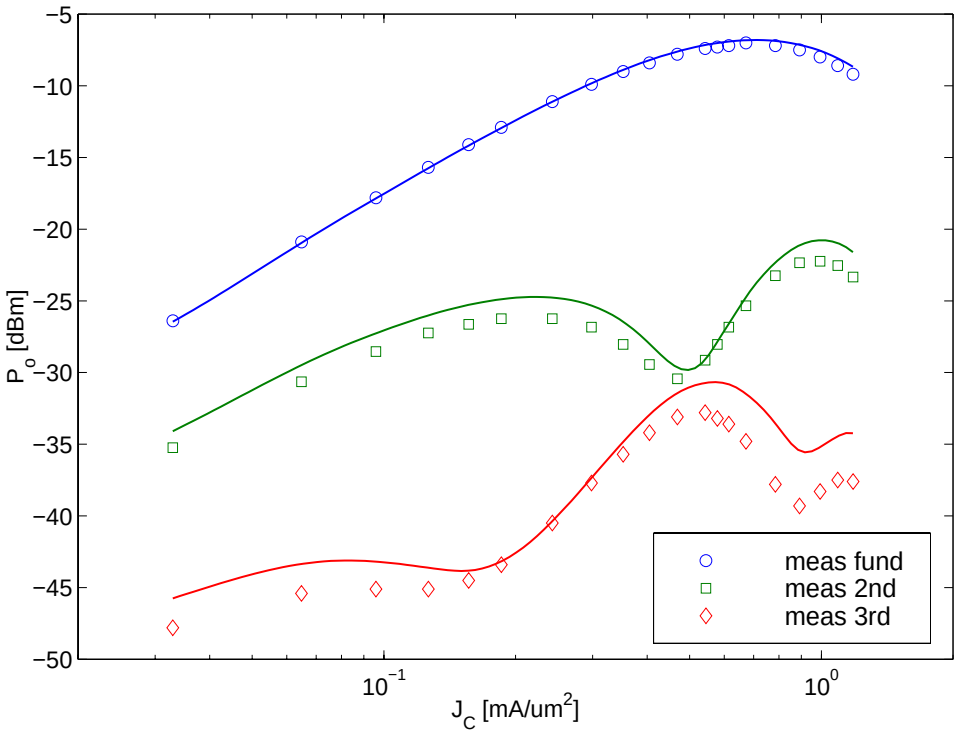


(b)

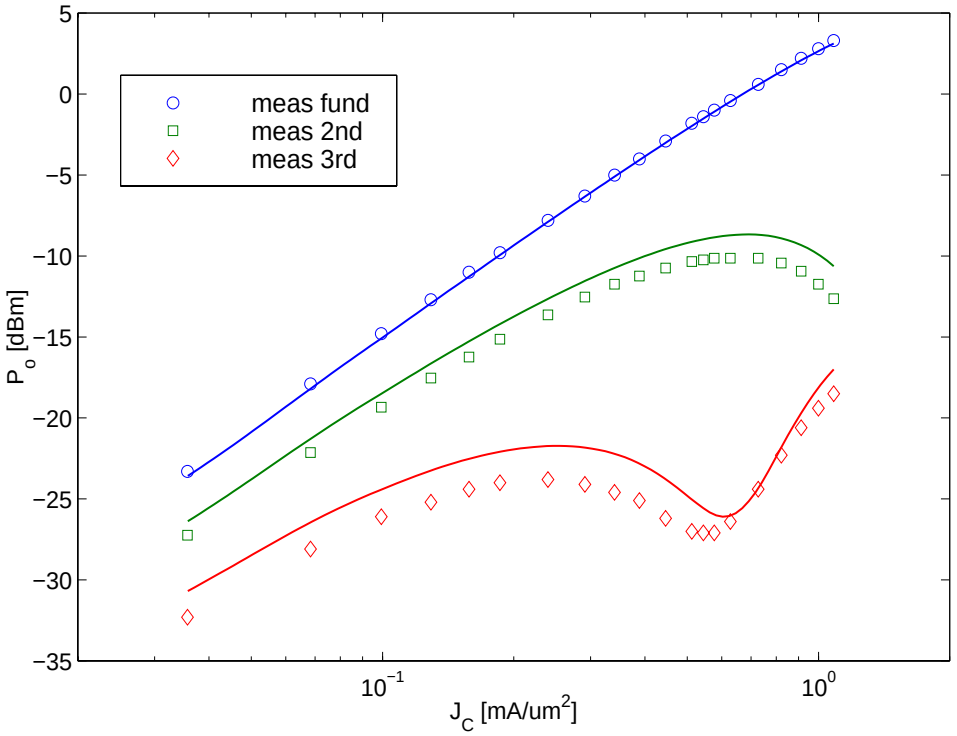


P_{out} vs. collector current density I_C/A_E at f_0 = 0.9 GHz for a 25 GHz transistor (0.4*14µm^2); comparison between measurement (symbols) and HICUM (lines):
(a) P_{in} = -20 dBm; (b) P_{in} = -10 dBm. V_{CE} = 3 V.

(a)

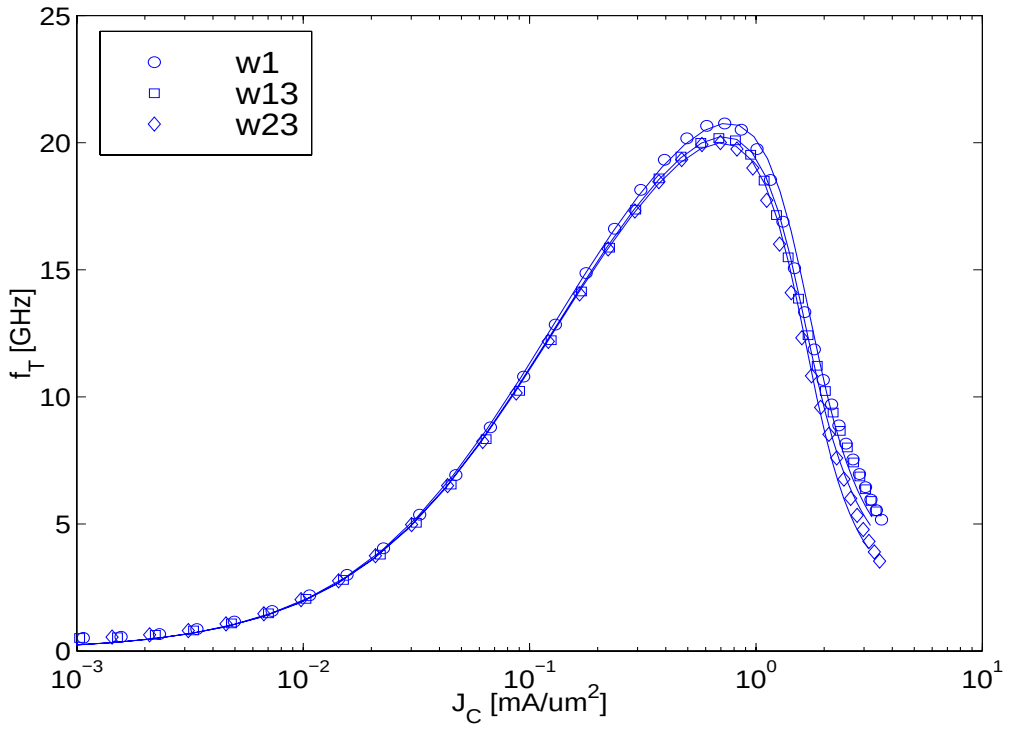


(b)

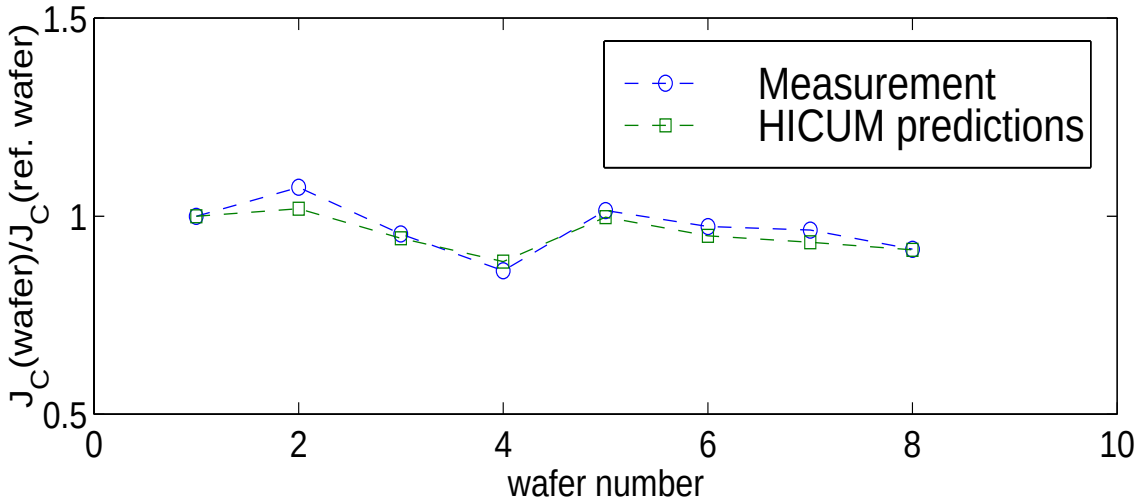


P_{out} vs. collector current density I_C/A_E at f_0 = 1.8 GHz for a 25 GHz transistor (0.4*14µm^2); comparison between measurement (symbols) and HICUM (lines):
(a) P_{in} = -20 dBm, V_{CE} = 0.5 V; (b) P_{in} = -10 dBm, V_{CE} = 3 V.

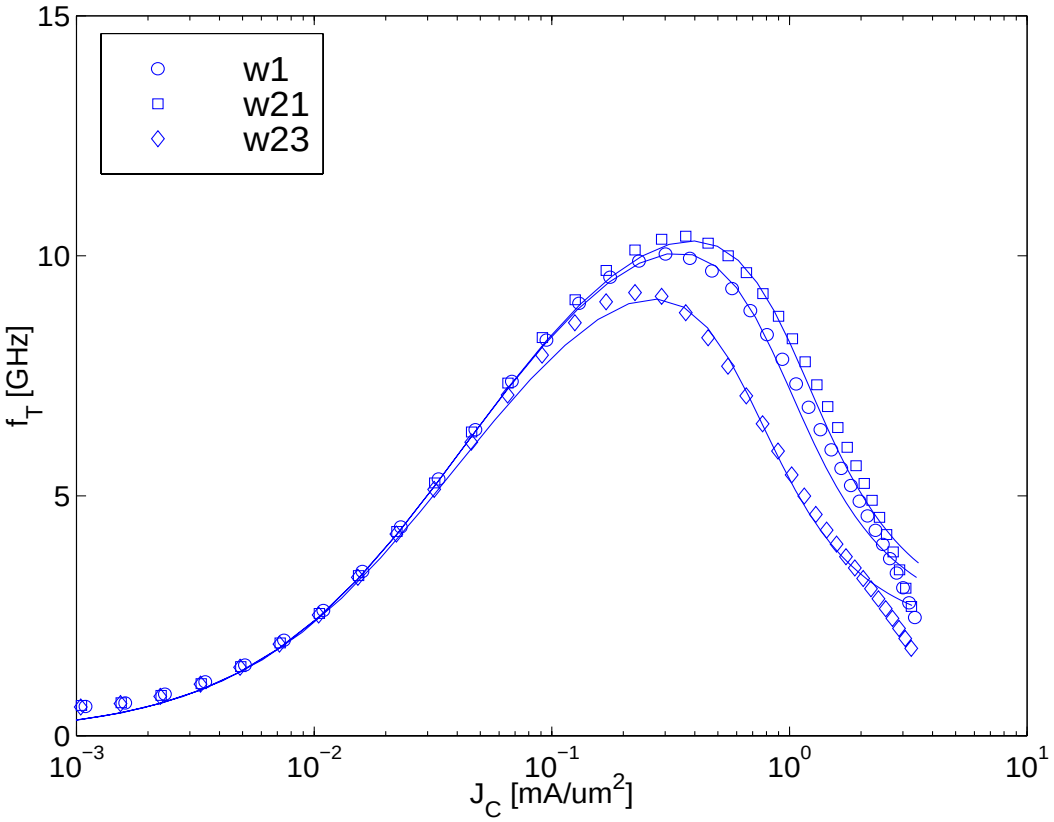
6.9 Predictive modelling



Transit frequency vs. collector current density for several process variations: base line (circles), 10% decrease of selectively implanted collector dose (squares), 25% increase of epi width w_C (diamonds). Comparison between measurement (symbols) and HICUM predictions (solid lines). V_{CE} = 0.8 V; emitter size: 0.4*14 µm^2.

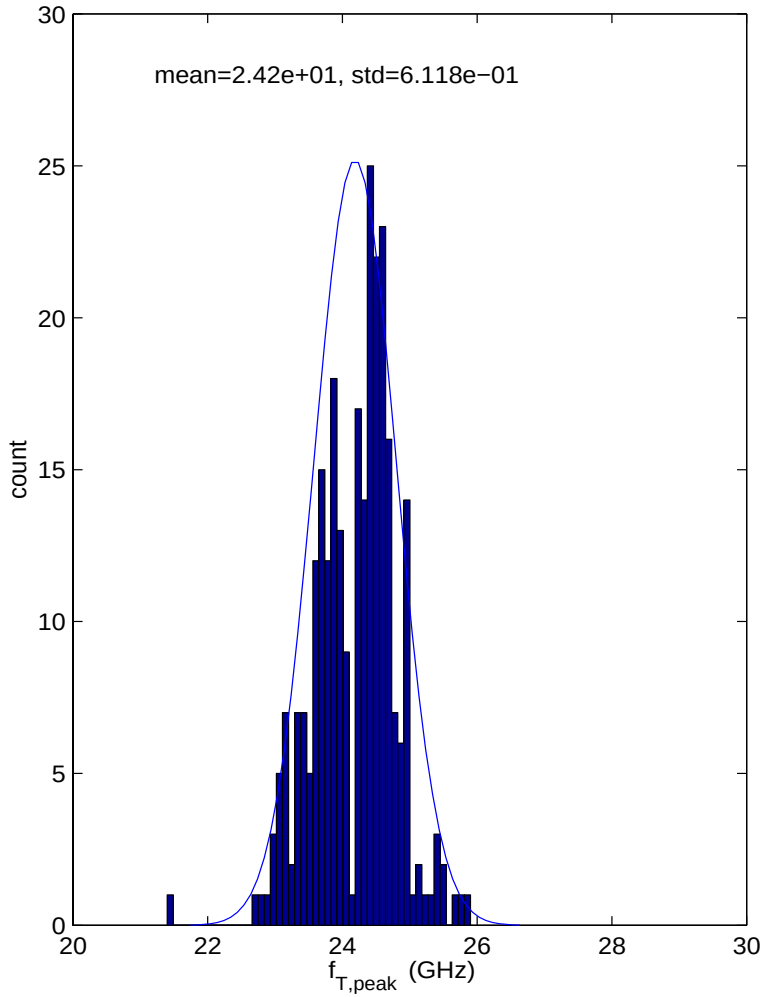


Collector current density at fixed V_{BE} = 0.8V for the same process variants as above; comparison between measurement (o) and HICUM predictions (-). V_{CE} = 0.8V; Emitter size: 0.4*14µm^2

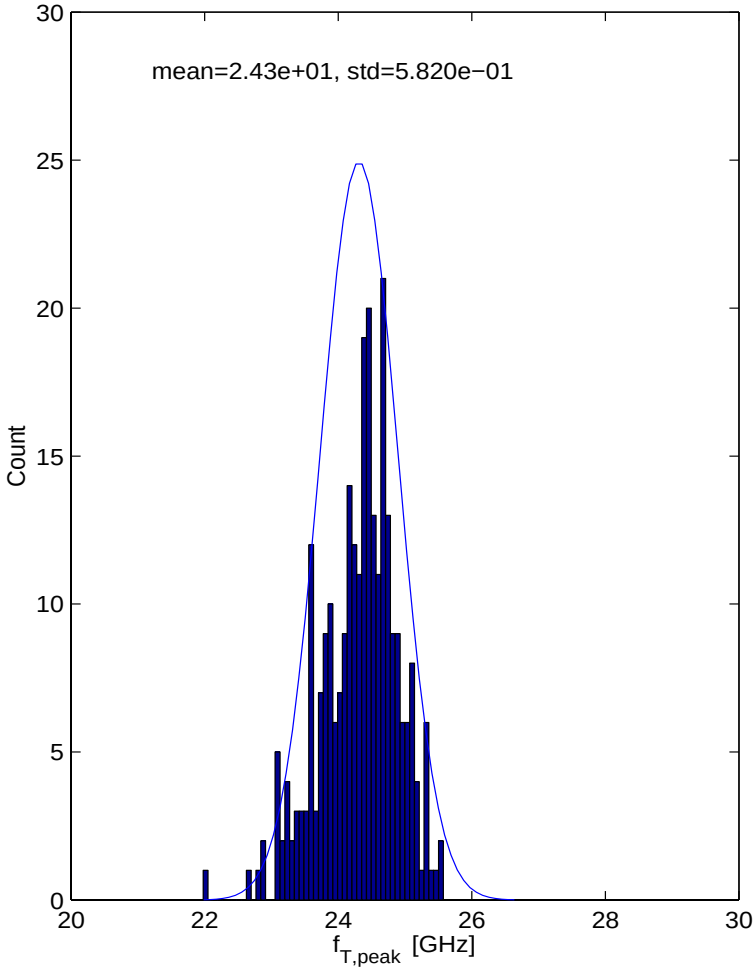


Transit frequency vs. collector current density for several variations of a “high-voltage” process: base line (circles), ≈5% increase of epi collector doping (squares), 25% increase of epi width w_C (diamonds). Comparison between measurement (symbols) and HICUM predictions (solid lines). V_{CE} = 0.8 V; emitter size: 0.4*14 µm^2.

6.10 Statistical modelling

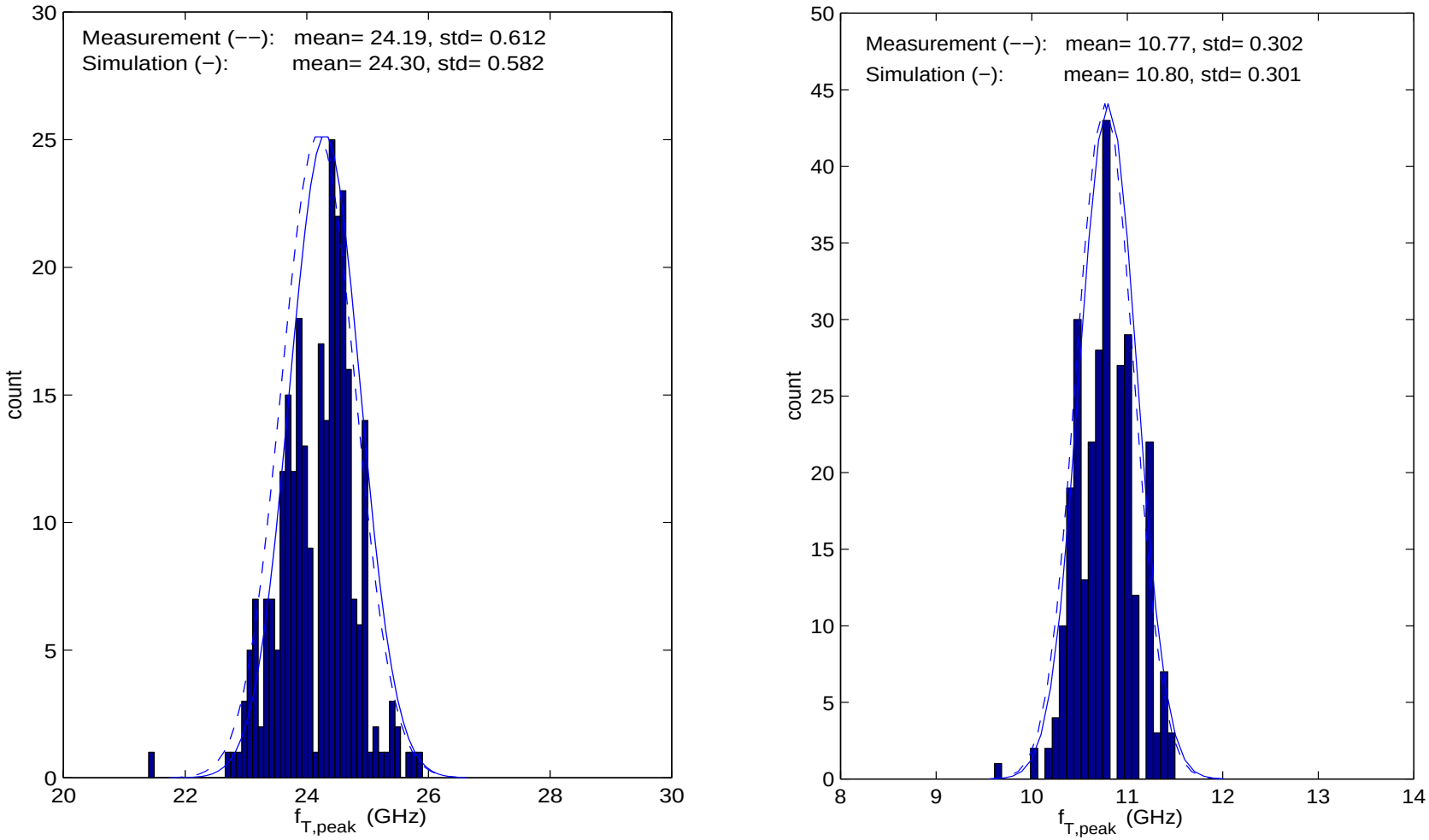


(a)



(b)

Statistical distribution curves of peak f_T for a “high-speed” process. Comparison between (a) measurements and (b) HICUM predictions from process monitors. V_{CE} = 2 V; emitter size: 0.4*14 μm^2. The results were obtained from 5 different lots.

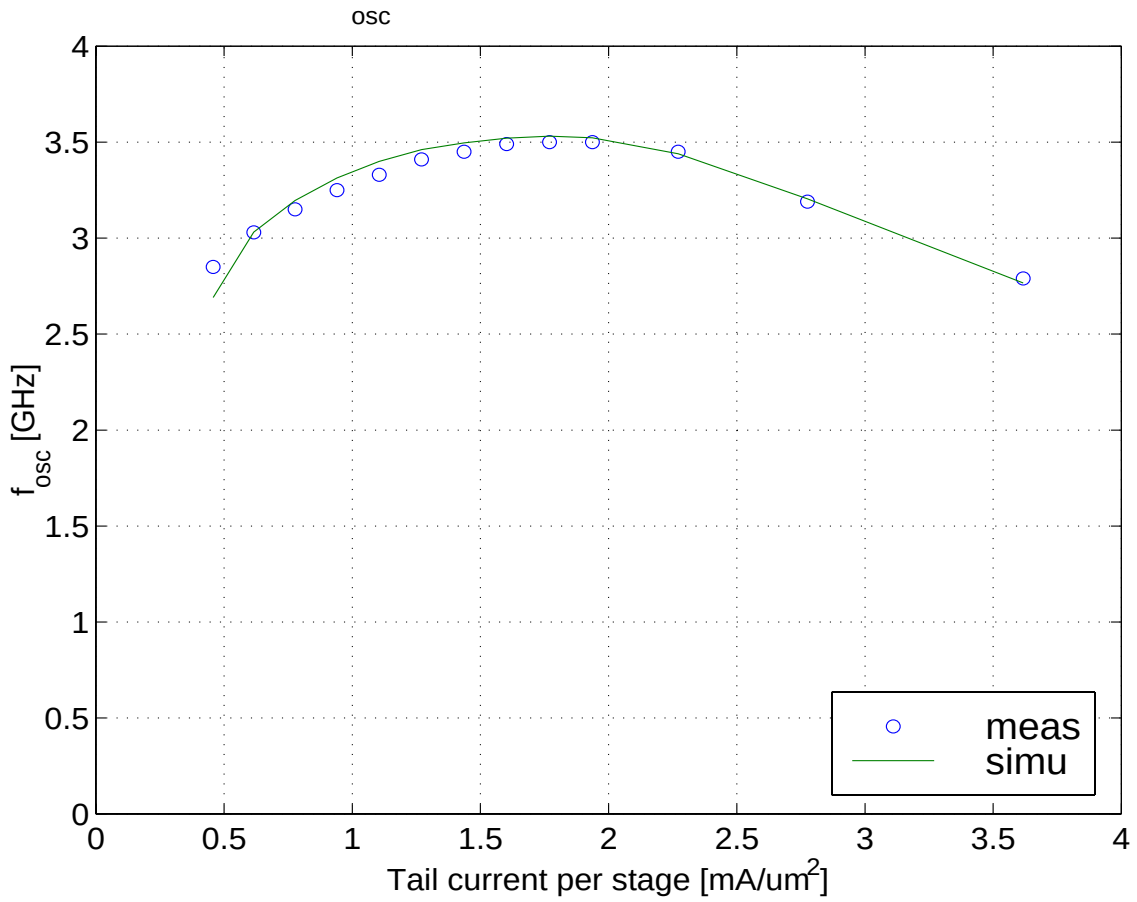


(a) (b)

Statistical distribution curves of peak f_T for transistors with 0.4*14μm^2 emitter size. Comparison between measurements (histogram and solid lines) and HICUM predictions from process monitors (dashed lines): (a) “high-speed” process; (b) “high-voltage” process. The results were obtained from 5 different lots.

6.11 Circuit results

A few remarks are required here. In principle, there is agreement between design and modelling engineers that model validation on benchmark circuits is beneficial for both sides (cf chapter 4). However, this validation loop is rarely closed in an industrial environment for various reasons, such as simply the large schedule and product pressure on one hand and the very limited resources on the other hand. In addition, it is difficult to obtain agreement on which benchmark circuits satisfy at least the majority of design applications. For digital applications, often frequency dividers and ringoscillators consisting of CML or ECL gates are employed; experimental results for the latter will be shown below. For h.f. analog (e.g.. wireless) applications, not only the selection but also the design and testing itself is much more difficult. A larger variety of designs that are suited for on-wafer testing are required. As of now, results of only few production circuits are available that agree well with model “predictions”, but which have not been included here due to proprietary reasons.



Oscillation frequency f_{osc} vs. current density (I_{tail}/A_E) per stage for a CML ring-oscillator fabricated in a 25 GHz process; comparison between measurement (symbols) and HICUM (lines).
Due to power considerations, the smallest manufacturable emitter size ($0.4*0.7\mu m^2$) has been used; no specific or other model parameters were adjusted for this example.

7 References

[1] H.K. Gummel and H.C. Poon, "An Integral Charge-Control Model for Bipolar Transistors", BSTJ Vol. 49, 1970, pp. 827-852.

[2] P. Antognetti and G. Massobrio, "Semiconductor Device Modeling with SPICE", McGraw-Hill, 1988. (SGPM related material only)

[3] B.C. Bouma and A.C. Roelofs, "An Experimental Determination of the Forward-Biased Emitter-Base Capacitance", Solid-State Electron., Vol. 21, 1978, pp. 833-836.

[4] D. Celi, private communication.

[5] S. Voinigescu, M. Maliepaard, M. Schröter, P. Schvan and D. Harame, „A scaleable high-frequency noise model for bipolar transistors and its applications in low-noise amplifier design“, IEEE J. Solid-State Circuits, Vol. 32, pp. 1430-1439, 1997.

[6] X.Y. Chen, M.J. Deen, Z.X. Yan, and M. Schroter, “Effects of emitter dimensions on low-frequency noise in double-polysilicon BJTs ”, Electronics Letters, Vol. 34, No. 2, pp. 219-220, 1998.

[7] X.Y. Chen, M.J. Deen, A.D. van Rheenen, Z.X. Yan, and M. Schroter, “Low-frequency noise in npn and pnp double-polysilicon BJTs, effects of temperature and emitter dimensions”, Proc. IEDMS, pp. - , 1998.

[8] M.J. Deen, S.L. Rumyantsev, and M. Schroter, “On the origin of 1/f noise in polysilicon emitter bipolar transistors”, J. Appl. Phys., Vol. 85, No. 2, pp. 1192-1195, 1999.

[9] [H.K. Gummel, "On the definition of the cutoff frequency f_T", Proc. IEEE, Vol. 57, pp. 2159, 1969.

[10] H.K. Gummel, "A charge-control relation for bipolar transistors", BSTJ, Vol. 49, pp. 115-120, 1970.

[11] R. Dennison and K. Walter, “Local thermal effects in high performance bipolar devices/circuits”, Proc. IEEE Bipolar and BiCMOS Circuits and Technology Meeting, Minneapolis, pp. 164-167, 1989.

[12] C.T. Kirk, “A theory of transistor cutoff frequency falloff at high current densities”, IEEE Trans. Electron Dev., Vol. 9, pp. 914-920, 1962.

[13] A. Koldehoff, M. Schröter, and H.-M. Rein, "A compact bipolar transistor model for very high-frequency applications with special regard to narrow stripes and high current densities", Solid-State Electron., Vol. 36, pp. 1035-1048, 1993.

[14] T.-Y. Lee and M. Schröter, “Methodology for bipolar transistor model parameter extraction”, documentation for the CMC, (http://www.eigroup.org/cmc), Feb. 1999.

[15] T.-Y. Lee et al., “Modeling and parameter extraction of of BJT substrate resistance “, Proc. IEEE Bipolar and BiCMOS Circuits and Technology Meeting, Minneapolis, pp. 101-104, 1999.

[16] [W. Maes, K. DeMeyer, and R. Van Overstraaten, “Impact ionization in silicon: a review and update”, Solid-State Electron., Vol. 33, pp. 705-718, 1990.

[17] C. Mallardeau et al., “A 12V BiCMOS technology for mixed analog-digital applications with high performance vertical pnp”, Proc. ESSDERC ‘90, pp. 397-400, 1990.

[18] P. Mars, "Temperature dependence of avalanche breakdown voltage in pn junctions", Int. J. Electronics, Vol. 32, No. 1, pp. 23-37, 1971.

[19] D.R. Pehlke, private communication, 1998.

[20] M. Pfost, H.-M. Rein, and T. Holzwarth, "Modeling substrate effects in the design of high-speed Si bipolar ICs",. IEEE J. Solid-State Circuits, Vol. 31, pp. 1493-1502, 1996.

[21] R.L. Pritchard, “Transistor Characterictics”, McGraw Hill, 1967.
[22] H.-M. Rein, "Proper choice of the measuring frequency for determining fT of bipolar transistors", Solid-State Electronics, Vol. 26, pp. 75-82 and p. 929, 1983.
[23] H.-M. Rein, "A simple method for separation of the internal and external (peripheral) currents of bipolar transistors", Solid-State Electronics, Vol. 27, pp. 625-632, 1984.
[24] H.-M. Rein, H. Stübing, and M. Schröter, "Verification of the Integral Charge-Control Relation for high-speed bipolar transistors at high current densities", IEEE Trans. Electron Dev., Vol. 32, pp. 1070-1076, 1985.
[25] H.-M. Rein and M. Schröter, "A compact physical large-signal model for high-speed bipolar transistors at high current densities - Part II: Two-dimensional model and experimental results", IEEE Trans. Electron Dev., Vol . 34, pp. 1752-1761, 1987.
[26] H.-M. Rein and M. Schröter, "Base spreading resistance of square emitter transistors and its dependence on current crowding", IEEE Trans. Electron Dev., Vol. 36, pp. 770-773, 1989.
[27] H.-M. Rein and M. Schröter, "Experimental determination of the internal base sheet resistance of bipolar transistors under forward-bias conditions", Solid-State Electron., Vol. 34, pp. 301-308, 1991.
[28] H.-M. Rein, M. Schröter, A. Koldehoff, and K. Wörner, "A semi-physical bipolar transistor model for the design of very high-frequency analog ICs", Proc. IEEE Bipolar and BiCMOS Circuits and Technology Meeting, Minneapolis, pp. 217-220, 1992.
[29] M. Schröter and H.-M. Rein, "Two-dimensional modelling of high-speed bipolar transistors at high current densities using the Integral Charge-Control Relation relation", Proc. ESSDERC '84; see also: Physica B, North Holland Phys. Publ. Div., pp. 332-336, 1985.
[30] [M. Schröter and H.-M. Rein, "A compact physical large-signal model for high-speed bipolar transistors including the high-current region" (in German), NTG meeting, Würzburg, Mai 1986.
[31] M. Schröter, "A compact physical large-signal model for high-speed bipolar transistors with special regard to high current densities and two-dimensional effects", (in German), Dissertation, Ruhr-University Bochum, Bochum, Germany, Jan. 1988.
[32] M. Schröter and H.-M. Rein, "Transit time of high-speed bipolar transistors in dependence on operating point, technological parameters, and temperature", Proc. IEEE Bipolar Circuits and Technology Meeting, Minneapolis, pp. 85-88, 1991.
[33] M. Schröter, "Simulation and modelling of the low-frequency base resistance of bipolar transistors in dependence on current and geometry", IEEE Trans. Electron Dev., Vol. 38, pp. 538-544, 1991.
[34] M. Schröter, "Modeling of the low-frequency base resistance of single base contact bipolar transistors", IEEE Trans. Electron Dev., Vol. 39, pp. 1966-1968, 1992.
[35] M. Schröter, M. Friedrich, and H.-M. Rein, " A generalized Integral Charge-Control Relation and its application to compact models for silicon based HBTs", IEEE Trans. Electron Dev., Vol. 40, pp. 2036-2046,1993.
[36] M. Schröter, (a) "Physical models for high-speed silicon bipolar transistors - A comparison and overview", (in German), Habilitation thesis, 1994 (excerpts are available on request);
(b) "Bipolar transistor modelling for integrated circuit design", Graduate Course, Carleton Univesity, Ottawa, 1995 (contains large portions of (a) in English).
[37] M. Schröter and H.-M. Rein, "Investigation of very fast and high-current transients in digital bipolar circuits by using a new compact model and a device simulator", IEEE J. Solid-State Circuits, Vol. 30, pp. 551-562, 1995.

[38] M. Schröter and D.J. Walkey, "Physical modeling of lateral scaling in bipolar transistors", IEEE J. Solid-State Circuits, Vol. 31, pp. 1484-1491, 1996 and Vol. 32, pp. 171, 1998.

[39] M. Schröter, Z. Yan, T.-Y Lee, and W. Shi, "A compact tunneling current and collector breakdown model", Proc. IEEE Bipolar Circuits and Technology Meeting, Minneapolis, pp. 203-206, 1998.

[40] M. Schröter and T.-Y. Lee, “HICUM - a physics-based scaleable compact bipolar transistor model“, presentation to the Compact Model Council, (http://www.eigroup.org/cmc), Dec. 1998.

[41] M. Schröter and T.-Y. Lee., "A physics-based minority charge and transit time model for bipolar transistors", IEEE Trans. Electron Dev., vol. 46, pp. 288-300, 1999.

[42] M. Schröter et al., “Physics- and process-based bipolar transistor modeling for integrated circuit design", IEEE Journal of Solid-State Circuits, vol. 34 , pp. 1136-1149, 1999.

[43] M. Schröter, D.R. Pehlke and T.-Y. Lee, „Compact modeling of high-frequency distortion in bipolar transistors“, Proc. ESSDERC, Leuven, pp. 476-479, 1999.

[44] M. Schröter, D.R. Pehlke and T.-Y. Lee, „Compact modeling of high-frequency distortion in Si integrated bipolar transistors“, IEEE Trans. on Electron Dev., Vol. 47, pp. 1529-1539, 2000.

[45] H. Stübing and H.-M. Rein, "A compact physical large-signal model for high-speed bipolar transistors at high current densities - Part I: One-dimensional model", IEEE Trans. Electron Dev., vol. 34, pp. 1741-1751, 1987.

[46] S. Sze, "Physics of semiconductor devices", Wiley & Sons, New York, 1981.

[47] H.Q. Tran, “Investigation of SiGe heterojunction bipolar transistors with respect to compact modeling for integrated circuit design”, MSEE. thesis, Carleton University, Ottawa, Canada, 1997.

[48] H.Q. Tran et al., “Simultaneous extraction of thermal and emitter series resistances in bipolar transistors”, Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting, Minneapolis, pp., 1997.

[49] P.B. Weil and L.P. McNamee "Simulation of excess phase in bipolar transistors", IEEE Trans. Circ. Syst., Vol. 25, pp. 114-116, 1978.

[50] J. TeWinkel, "Extended charge-control model for bipolar transistors", IEEE Trans. Electron Dev., Vol. 20, pp. 389-394, 1973.