

2nd International HICUM user's meeting

Monterey, September 2002

D. Berger, D. Céli, T. Burdeau

STMicroelectronics, Crolles, France

HICUM status in ST

- HICUM status

- Extraction tools

- Parameters extraction

- Results

- Extraction issues

- Implementation of HICUM model equation in an in-house program.
- This implementation corresponds to the DEVICE equations (HICUM version 2.1).
- HICUM test structures implemented in test masks.
- Extraction procedures were developed for a single geometry transistor.
- Implementation in an industrial extraction tool ICCAP is in progress.
- Test on different devices and processes have been realized in order to validate the extraction flow and the model equations.
- Regular comparisons between DEVICE and different circuit simulators are made to insure the right implementation of HICUM into CAD tools.

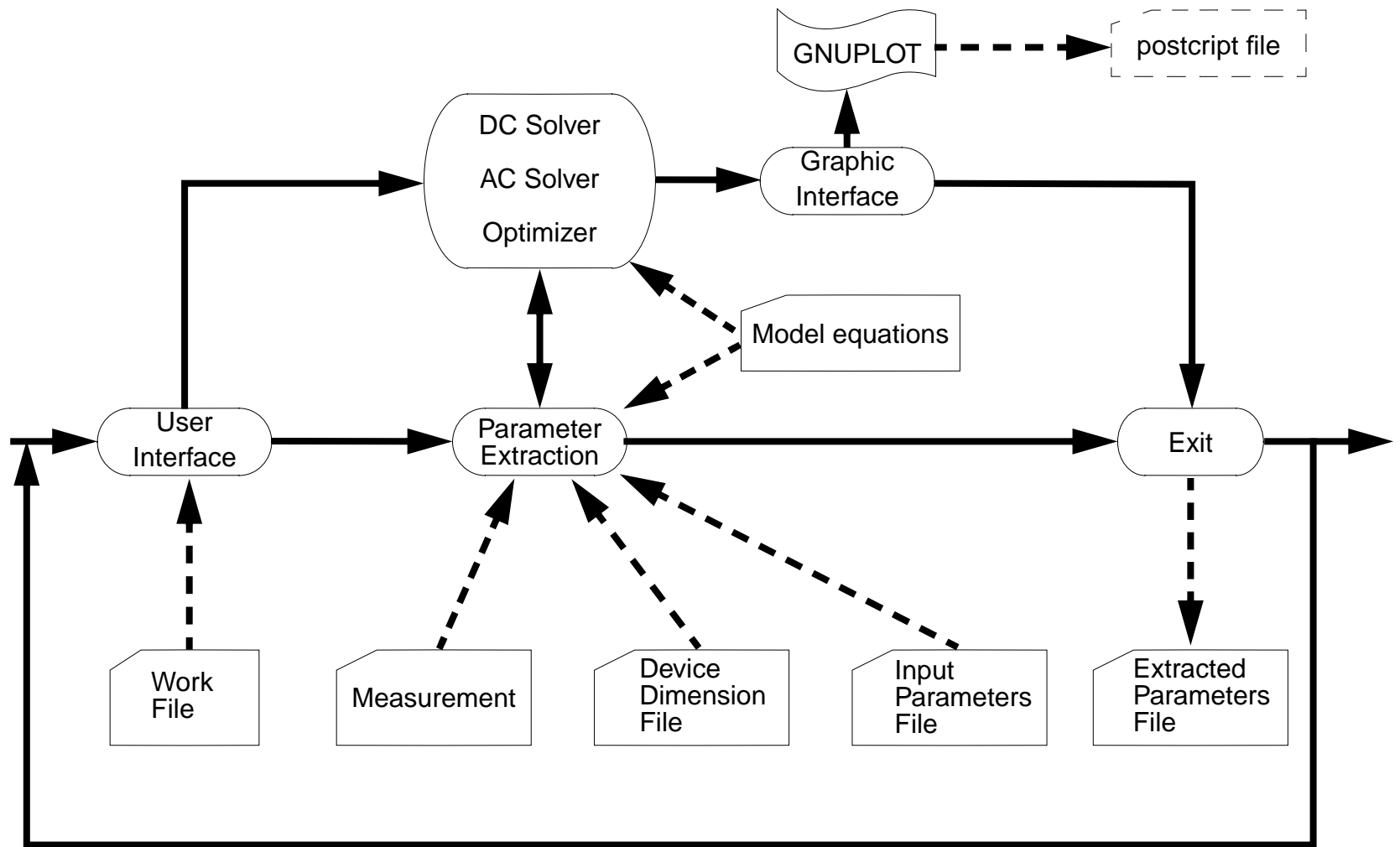
Extraction tools

- HICUM status
- Extraction tools
 - SPEED
 - ICCAP
- Parameters extraction
- Results
- Extraction issues

- All HICUM model equations (version 2.1) have been implemented in a ST in-house program named SPEED (Spice Parameter Extraction tool for Electron Devices).
 - Internal AC-DC solver.
 - Allows to access to internal variables like junction capacitances, currents, transit time... very useful to understand the model and for global optimization.
 - At this time HICUM was not correctly implemented in various circuit simulators.
- Implementation in ICCAP is in progress.
 - ELDO: good convergence but slow interface with ICCAP.
 - ADS : good interface with ICCAP but some convergence problems in high injection level.

SPEED: Spice Parameter Extraction tool for Electron Devices

- HICUM status
- Extraction tools
 - SPEED
 - ICCAP
- Parameters extraction
- Results
- Extraction issues



ICCAP

- HICUM status
- Extraction tools
 - SPEED
 - ICCAP
- Parameters extraction
- Results
- Extraction issues

The screenshot displays the HICUM Single Geometry Extraction Toolkit interface. The main window is titled "HICUM Single Geometry Extraction Toolkit" and contains several panels:

- Import Data and Initialize Parameters**: A button to start the process.
- Choose Simulator**: A button to select the simulation tool.
- Model Parameters Management**: Buttons for "Load Model Parameter Set" and "Store Model Parameter Set".
- Junction Capacitance Analysis**: Includes buttons for "CBE Extraction", "CBC Extraction", and "CCS Extraction".
- DC Analysis**: Includes buttons for "Avalanche Parameters", "Substrate Current Optimization", "Low Injection Collector Current", "I_{bc} Extraction", "Forward Early - HJCI", "R_{bc} Optimization", and "Base Current at Low Injection".
- AC Analysis**: Includes buttons for "Transit Time Extraction at Low Injection", "Transition Frequency Optimization at Low Injection", "Effective knee Current (HJCI)", "Critical Current", and "Transit Time at High Injection".

A secondary window titled "HICUM Ft Optimization (Low Injection)" is open, showing:

- Display Ft Characteristics** and **Ft versus Ic Simulation** tabs.
- Close All Plots** and **Clear Simulation** buttons.
- Optimizations**: Checkboxes for "TB", "DTBH", "TBVL", and "ALJCI".
- Run Optimizer...** and **Run Tuner...** buttons.
- Model Parameters** table:

Min TD [s]	Min DTBH [s]	Min TBVL [s]	Min ALJCI [-]
1f	1p	1f	1m
1.174p	24.00f	153.1f	2.43f
Max TB [s]	Max DTBH [s]	Max TBVL [s]	Max ALJCI [s]
1n	1n	1n	10

Additional controls include "Voltage and Frequency Selection" (Vbe Start [V], Vbe Stop [V], Vbe Step [V], Simulation Frequency [GHz]) and "Get Vbe Limits From Ft versus Vbe Characteristic" and "Select Full Linear Vbe Range" options.

A third window titled "Ft_Ic_Simul:83" displays a plot titled "Ft versus Ic Characteristic". The y-axis is "Ft Meas. [Ghz] Ft Simu. [Ghz] [E+0]" ranging from 0.0 to 100.0. The x-axis is "Ic [A] [LOG]" ranging from 10⁻⁵ to 10⁻¹. The plot shows multiple curves representing the transition frequency (Ft) versus collector current (Ic) for different biasing conditions.

Parameters extraction status

- HICUM status
- Extraction tools
- **Parameters extraction**
 - Status
 - Extraction flow
- Results
- Extraction issues

- An extraction flow for a single transistor geometry has been developed using SPEED (see BCTM paper).
 - Some points still need to be improved to obtain more physical and scalable parameters.
 - The methodology has been successfully tested on different processes and devices.
- A scalable parameter extraction strategy is under development.
 - DC parameters
 - AC parameters
- Preliminary temperature extractions have been done and must be confirmed and automated in order to take into account the self-heating.
 - Self-heating becomes more and more important for SiGe transistors (high f_T , trench isolation,...).

Extraction flow at room temperature

- HICUM status
- Extraction tools
- **Parameters extraction**
 - Status
 - **Extraction flow**
- Results
- Extraction issues

1	Total BE, BC and CS Junction Capacitances
2	Split of BE and BC Junction Capacitances $C_{JEI0}, C_{JEP0}, C_{JCI0}, C_{JCX0}$
3	BC avalanche current F_{AVL}, Q_{AVL}
4	Transfer current at low injection C_{10}, Q_{P0}, H_{JCI} assuming $H_{JEI}=1$
5	Internal BE current $I_{BEIS}, M_{BEI}, I_{REIS}, M_{REI}$
6	Parasitic substrate transistor Reverse BC current $I_{TSS}, I_{BCIS}, I_{BCXS}$
7	Series Resistances R_{CX}, R_E

8	Transit time at low injection $T_0, T_{BVL}, D_{TOH}, A_{LJEI}(=A_{LJEP})$
9	Transfer current at low and medium injection H_{JEI} , correction of C_{10}, Q_{P0}, H_{JCI} obtained in 4
10	Critical current $R_{CI0}, V_{CES}, V_{PT}, V_{Lim}$
11	Transit time at high injection $T_{EF0}, G_{TFE}, T_{HCS}, A_{LHC}$
12	Base Resistance $R_{BI0}, R_{BX}, F_{GEO}, F_{DQR0}$
13	NQS effect A_{LIT}, A_{LQF}

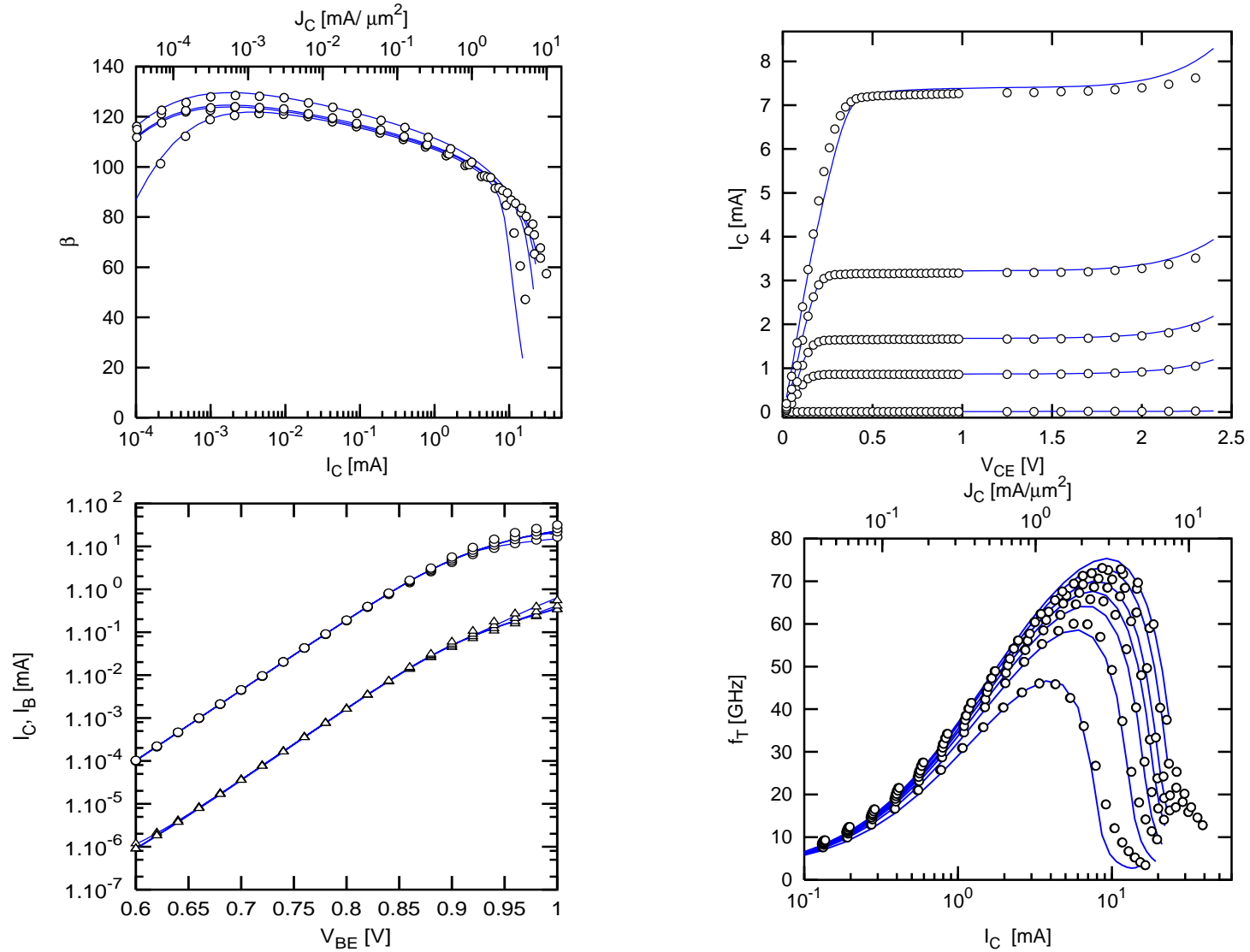


Improvement are required for scalable parameter extraction

Results

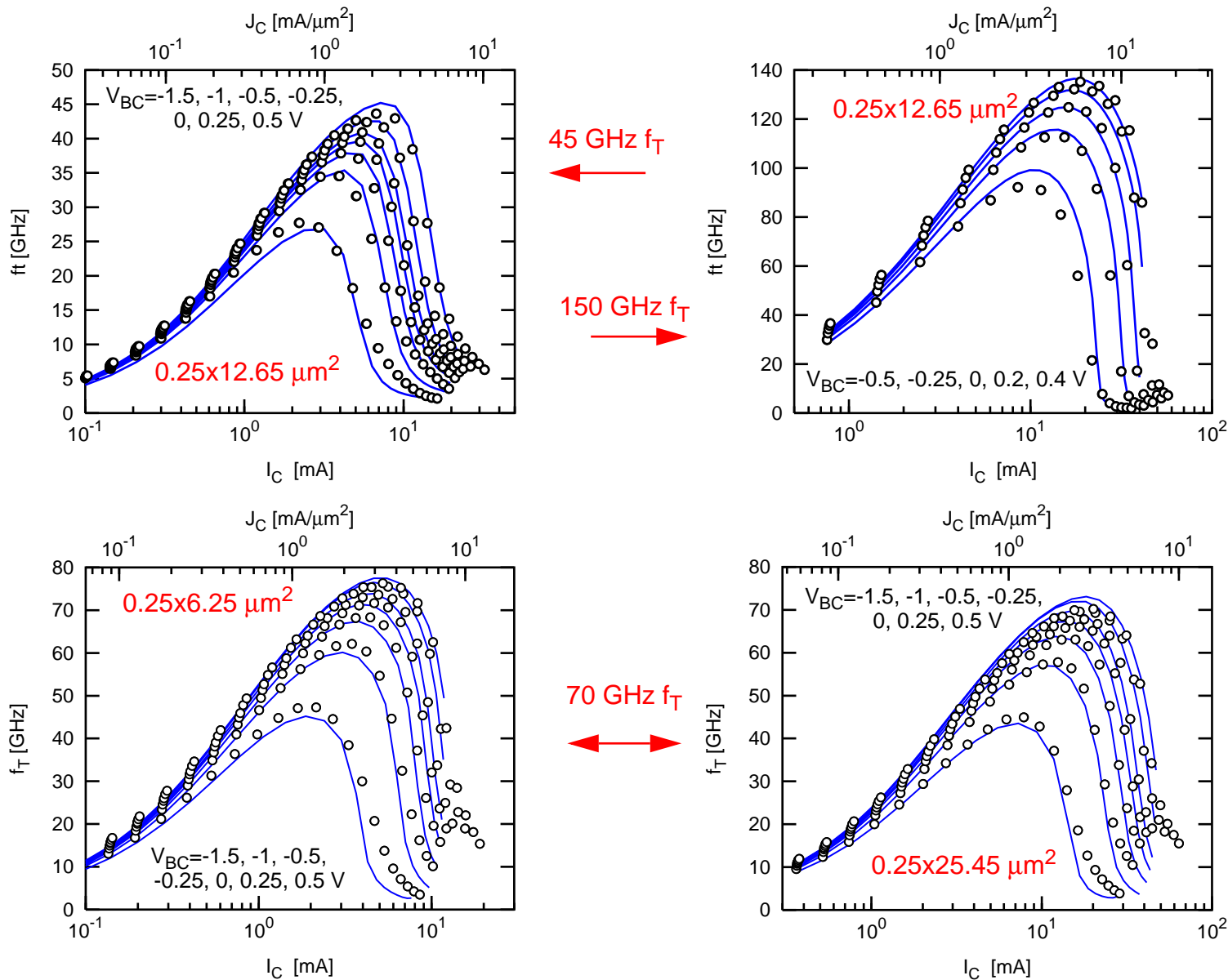
- HICUM status
- Extraction tools
- Parameters extraction
- **Results**
- Extraction issues

□ Transistor with $0.25 \times 12.65 \mu\text{m}^2$ emitter area, 70GHz f_T BiCMOS process



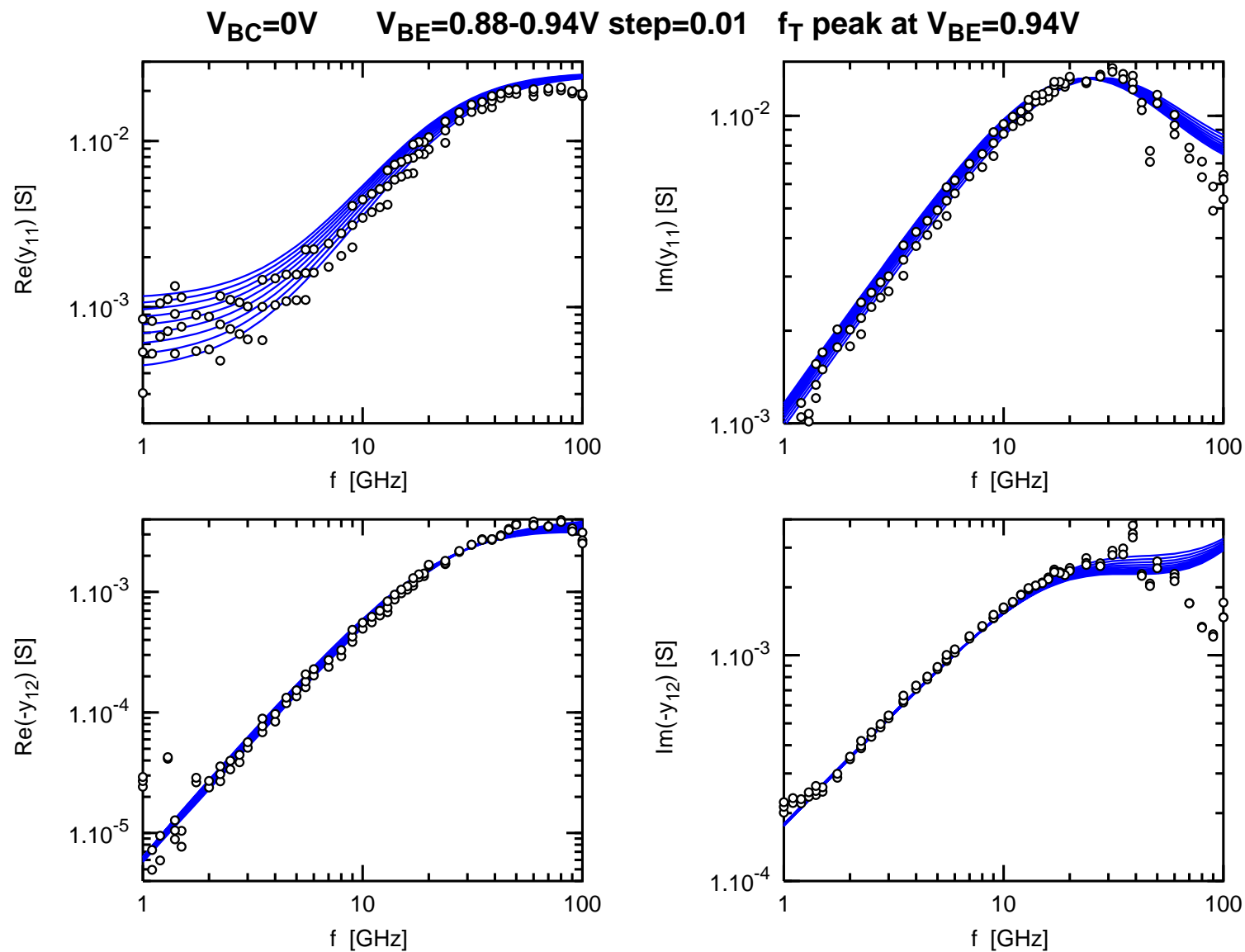
Results on different processes and devices

- HICUM status
- Extraction tools
- Parameters extraction
- Results
- Extraction issues



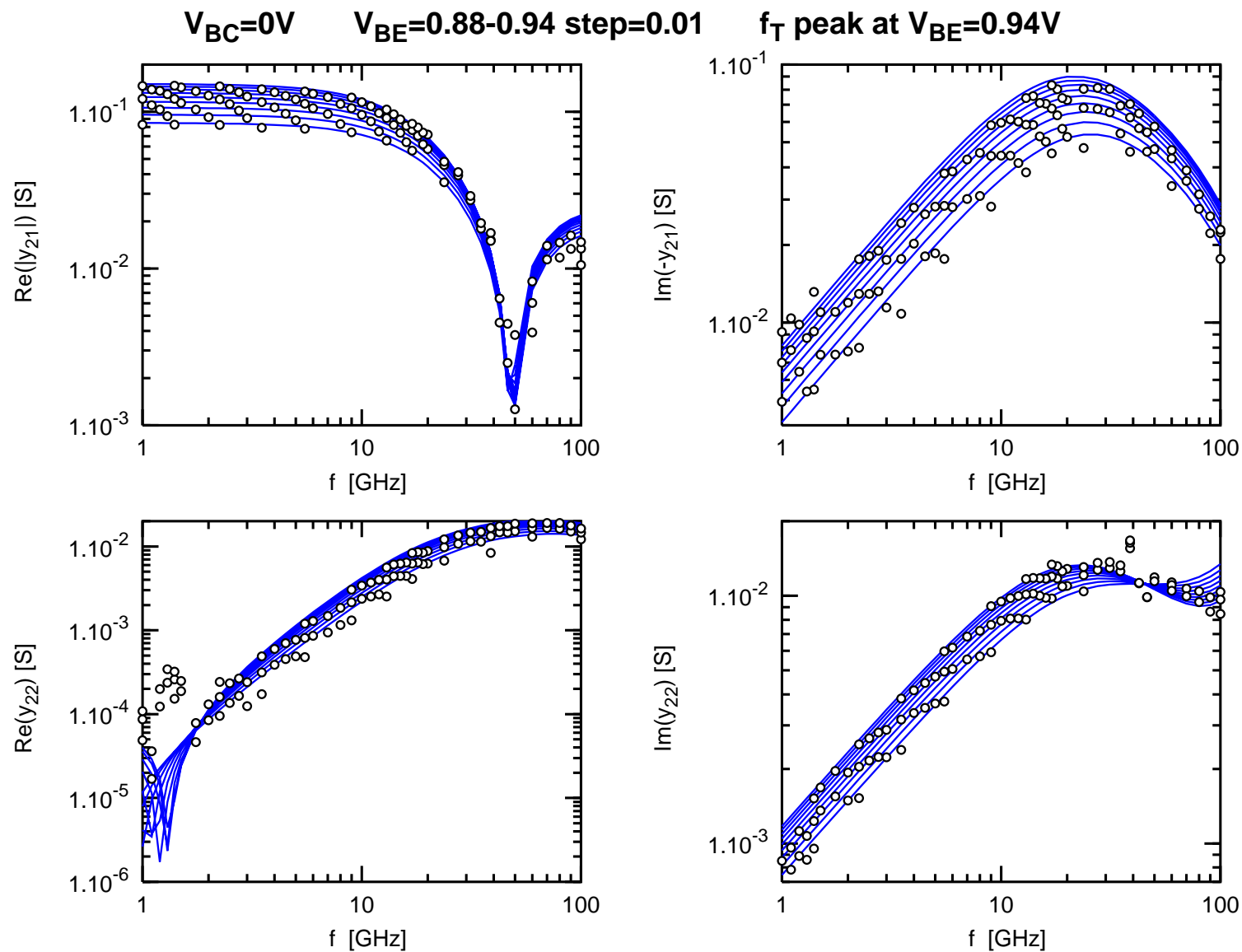
Y_{11} and Y_{12} parameters (0.25x12.65 μm^2 , 150GHz SiGe-C f_T)

- HICUM status
- Extraction tools
- Parameters extraction
- **Results**
- Extraction issues



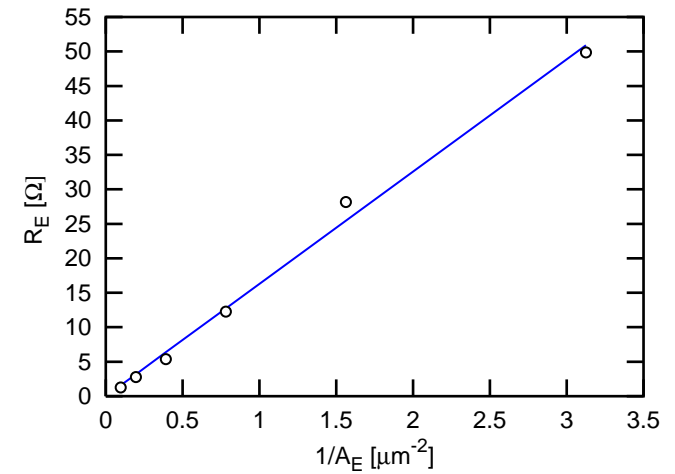
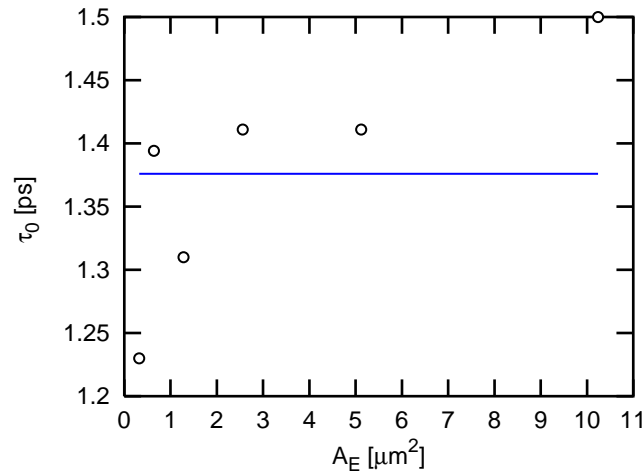
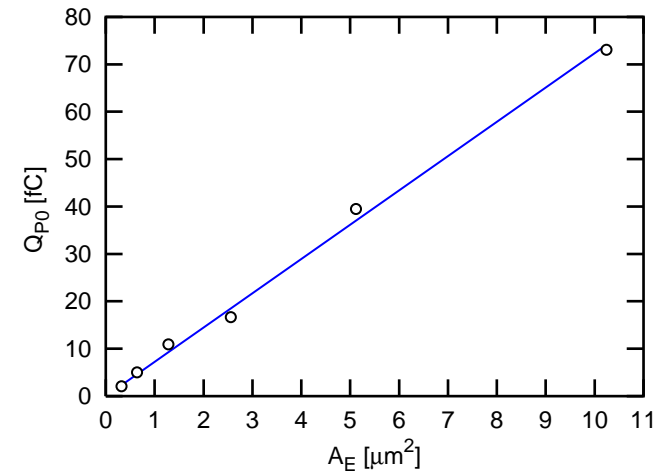
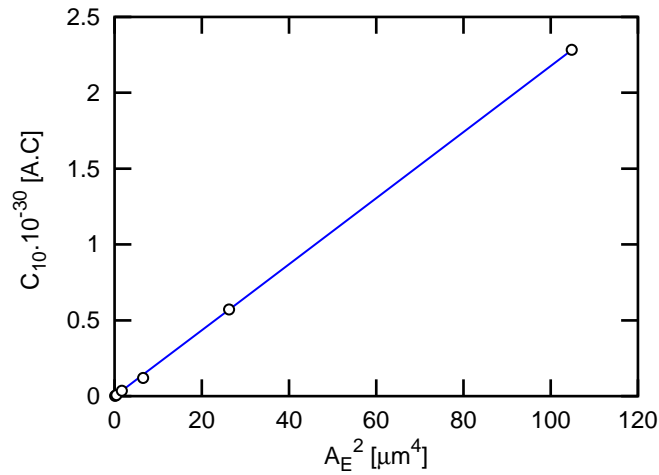
Y_{21} and Y_{22} parameters (0.25x12.65 μm^2 , 150GHz SiGe-C f_T)

- HICUM status
- Extraction tools
- Parameters extraction
- **Results**
- Extraction issues



Scalability (70GHz f_T process)

- HICUM status
- Extraction tools
- Parameters extraction
- **Results**
- Extraction issues



Main extraction issues

- HICUM status
- Extraction tools
- Parameters extraction
- Results
- **Extraction issues**

- Improvement needed to obtain more reliable parameters (physical and scalable) for multigeometry approach.
- The split of the junction capacitances with taking into account overlap capacitances would be more accurate with the multigeometry extraction flow. Work in progress.
- The collector resistance extraction is still a major issue because of its impact on the transit time determination. A better solution would be to calculate R_{CX} from layout and sheet resistance.
- The transit time calculation for f_T curves is still a critical point. Direct extraction from $\frac{1}{2\pi f_T}$ vs. $\frac{1}{I_C}$ curves is not enough accurate for transistor with high f_T . **Solutions ?**