

HICUM User's Meeting
September 29, 2002
Monterey, CA
Doubletree Hotel, 6-8 pm

Accurate modeling of Si and SiGe bipolar transistors has become one of the bottlenecks for designing high-speed/high-frequency circuits for, e.g., wireless and fibre-optic applications. The advanced compact bipolar transistor model HICUM has been developed to address these issues.

A HICUM users meeting was held to provide a technical forum for device modeling and circuit design engineers, that are applying or are interested in using HICUM, for exchanging information on and discussing aspects of the model that are relevant to their work.

Several short presentations were made, that centered around model parameter extraction and reliable model implementation in circuit simulators as the most important issues for industrial model users. Various methods and implementations for extracting the HICUM model parameters were proposed by representatives from various companies and universities. A commercial parameter extraction aid for HICUM using ICCAP is available.

A softcopy of several of the submitted presentations can be obtained from

http://www.iee.et.tu-dresden.de/iee/eb/eb_homee.html

Agenda

6:00 - 6:10 Welcome and overview

6:15 - 7:30 Presentations

Schroter, "Status of HICUM availability in circuit simulators"

Lavenir, Celi, "Status of HICUM integration in circuit simulators"

Ardouin, "HICUM-Aperitif - parameter extraction tool and service"

Berkner, "HICUM experience at Infineon"

Murty, Ahlgren, Haramé, "Experimental evaluation of HICUM"

Berger, Celi, "HICUM parameter extraction at ST"

Jiang, "HICUM model generation and delivery at JazzSemi"

Zimmermann, Zampardi, "Geometry scalable III-V HBT modeling"

Schroter, "TRADICA overview and relation to HICUM"

Schroter, "HICUM/Level0: more experimental results"

7:30 - 8:00 General discussion

Suggestions for further development

Purpose of this users meeting

forum for "free" *technical* discussion and exchange of information

model parameter extraction (= main issue in industry)

- confirm approaches
- identify possible cooperations or availability of tools ...
- discuss test structures and measurement procedures

model availability in circuit simulators

model formulation and development

- physical background and limitations
- status, plans, suggestions for enhancements (also from design community)

clarify questions

- facilitate and stimulate discussions by presentations of already existing results and solutions
- organisational
 - sheet with names and email (to receive information in future)
 - "suggestion" sheet (model development, meeting organisation, distribution of information etc.)
 - presentations/slides: will be posted on our web-site (please email to mschroter@ieee.org)

Status of HICUM

general information

- directly related papers since last workshop:
 - M. Schroter, T.-Y. Lee and M. Racanelli, “A scalable model generation methodology of bipolar transistors for RF IC design“, PA workshop, UCSD, 2001; see also related paper at BCTM 2001.
 - M. Schroter, “The advanced compact bipolar transistor model HICUM - An overview”, IEEE Circuits and Devices Magazine, May 2002, pp. 16-25.
 - D. Berger, D. Celi, M. Schroter, M. Malorny, T. Zimmer, and B. Ardouin, “HICUM parameter extraction flow for a single transistor geometry”, BCTM, Sept./Oct. 2002.
 - M. Schroter, S. Lehmann, and H. Jiang, “HICUM/Level0 - a simplified compact bipolar transistor model”, BCTM, Sept./Oct. 2002.
- 2nd European HICUM Workshop was held in Dresden, Germany, on June 6/7, 2002
 - 2-day workshop with detailed discussions
 - CAD (vendor) participation
 - any interest in US ?

HICUM development (1/2)

- main effects in SiGe and III-V HBTs (partially in cooperation with industry)
 - improved physics-based collector model (incl. high-current effects, barrier effects, avalanche, current dependent BC capacitance)
 - high-frequency noise and physical components
 - high-frequency (single- and two-tone) distortion
 - geometry scaling of III-V HBTs
 - parasitics (capacitance, inductance) from backend connections
 - intra-device substrate coupling (geometry scaling) using *fast* computation methods
 - thermal effects: geometry scaling (incl. junction isolation, deep trench, impact of metallization), coupling (s. DJW's JSSC 9/2002 paper)
- model hierarchy (in conjunction with TRADICA)
 - Level0: finish formulation, release Verilog-A code for evaluation and simulator integration
 - Level4: variable multi-transistor model (for critical applications, e.g. pinch-in, thermal coupling)
 - for both model levels: automated parameter generation from Level2 by TRADICA

HICUM development (2/2)

Other important topics

- parameter extraction
 - geometry scalable modeling:
 - continuous adaption to process development (extensions of existing and new methods)
 - tighter integration with existing tools (at, e.g., XMOD, Atmel, JazzSemi, ...)
 - single transistor procedure and implementation (for HICUM/L0)
 - automated conversion from HICUM to SGPM, xxxx => desired ?
- predictive and statistical modeling:
 - apply existing predictive equations to various SiGe processes (high-frequency and circuit applications)
 - possibly extend equations
- general comment:
new model equations have not been released in order to ensure stable and reliable ...
 - ... model implementation in major circuit simulators *and*
 - ... parameter extraction procedures and application throughout industry

Availability of HICUM/Level2 V2.1 in Circuit Simulators

(Please contact simulator vendor for details and the latest status of availability)

<i>simulator</i>	<i>first release</i>	<i>latest release</i>	<i>comments</i>
ELDO-RF	10/99	9/02	ELDO v5.8_1.1 (AMS 2002.1) with externally accessible thermal node
SPECTRE-RF	10/99	11/01	<ul style="list-style-type: none"> • SPECTRE 4.4.6/4.4.7 with HICUM2.1 • (10/99: CNXT ref = HICUM2.0)
ADS	7/00	2/02	can be combined with ICCAP
Smart-SPICE	11/00	11/00	can be combined with UTMOST
APLAC	10/01	10/01	APLAC 7.62a
HSPICE	2/01	2/02	version 2001.2 with HICUM2.0; AURORA compatible
TEKSPICE	8/02	8/02	various numerical improvements
Apache NSpice	09/02	09/02	
Xpedion, HSIM			code sent as per request, implementation in progress
SPICE3F5	4/02	4/02	replaces DEVICE as ref simulator

- Various (other) proprietary simulators (ASX (IBM), ...)
- Verilog-A version of model code (in progress for Level0 and Level2)

Availability in simulators (cont'd):

- runtime tests

17 stage ECL ring oscillator ($0.2 \times 1.7 \mu\text{m}^2$ transistors of a $0.18 \mu\text{m}$ BiCMOS process)

simulator	tail current [mA]	TRAN t_stop [ns]	volt. swing [mV]	total delay [ns]	initial/DC solution time [s]	TRAN analysis time [s]	CPU type
SPECTRE	0.056	4	196	1.79	0.5	32.76	Sparc5
ELDO	0.056	4	194	1.81	0.1	18.53	Pentium3
SPECTRE	3.6	2	196	0.307	0.07	47.68	Sparc5
ELDO	3.6	2	197	0.297	0.1	15.49	Pentium3

- Reference simulators

- stand-alone kit (source code) at http://www.iee.et.tu-dresden.de/iee/eb/eb_homee.html
- SPICE3F5 at <http://atelecad.com>
- DEVICE at http://www.iee.et.tu-dresden.de/iee/eb/eb_homee.html

- possible option to verify "correct" and unified model implementation:

have a "neutral entity" run a defined set of comparisons (can be automated tool with report capability)
=> implementation "quality stamp" (for a relatively small fee)

HICUM in SPICE3F

Jean Claude PERRAUD (perraud@ensicaen.ismra.fr)

Professeur Associé ISMRA (ENSI CAEN)

Expert CAD / IC Design (CAEN Philips Semiconductor)

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- ATELECAD SPICE 3F5 (ATELECAD KIT)
 - improved SPICE3f5++ (core from Berkeley Spice3f5_1)
 - LINUX or HPUX 9.XX -> 11.xx
- VALIDATION of HICUM SPICE MODEL
 - Analysis : OP , DC , TRAN , AC , NOISE (w/o self-heating, up to 1000000*usual_RTH value)
 - results OP DC AC TRAN:
 - NPN & PNP (identical,symetry)
 - low number of iteration (also with SHT), very good convergence behaviour ...
 - temp + mult OK
 - Self Heating OK
 - clamping for too high temperature
 - very good compliance with Stand-Alone DEVICE simulator (all currents 4 to 5 digits identical)

HICUM in SPICE3F (cont'd)

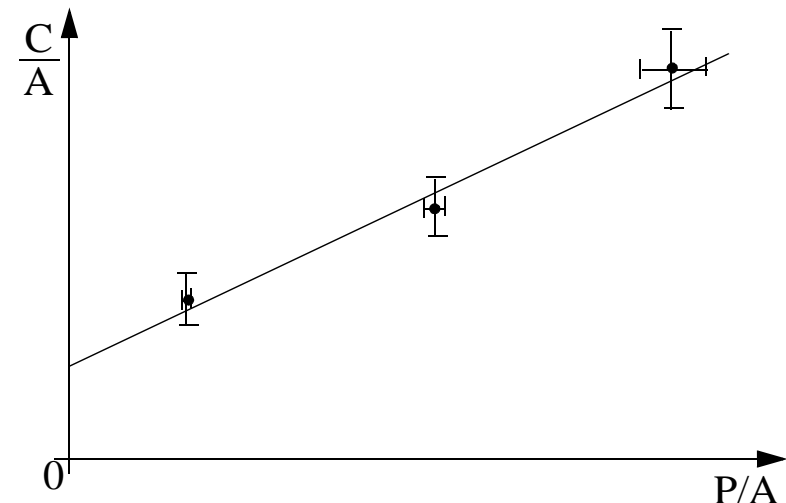
- Comparison to other simulators (status 3/2002)
 - SPECTRE (v4.4.6.100.44) with s.h. (10*usual_RTH)
 - NPN: very close to SPICE for OP,DC,AC; close to SPICE for TRAN
 - PNP : not symmetrical for OP,DC,AC; convergences PB for PNP (when reaching saturation)
 - ELDO (v5.6_1.1) with s.h. (10*usual_RTH)
 - NPN: very close to SPICE for OP,DC,AC; close to SPICE for TRAN
 - PNP: not symmetrical for OP,DC,AC
- General information regarding availability
 - non commercial use: available NOW (need to sign specific agreement/disclaimer ...)
 - commercial use: fair contribution is expected (please contact Prof. Jean Claude Perraud directly)

Geometrie scalable parameter extraction

- consider $\frac{C}{A_0} = \bar{C} + C' \frac{P_0}{A_0}$ with \bar{C} , C' as area and perimeter specific parameters to be extracted from measured C and $A_0 = b_0 l_0$, $P_0 = 2(b_0 + l_0)$
- measurement error sources:
 - electrical and intra-die (variation of C): ΔC
 - geometry (assuming width and length vary uncorrelated, but with the same absolute value Δb)
- propagation of errors (cf. P. Bevington, "Data reduction and error analysis for the physical sciences") => error range for

- the y-axis $\frac{\Delta \bar{C}}{\bar{C}} = \sqrt{\frac{\Delta C}{C} + \Delta b_0^2 \left(\frac{1}{b_0^2} + \frac{1}{l_0^2} \right)}$

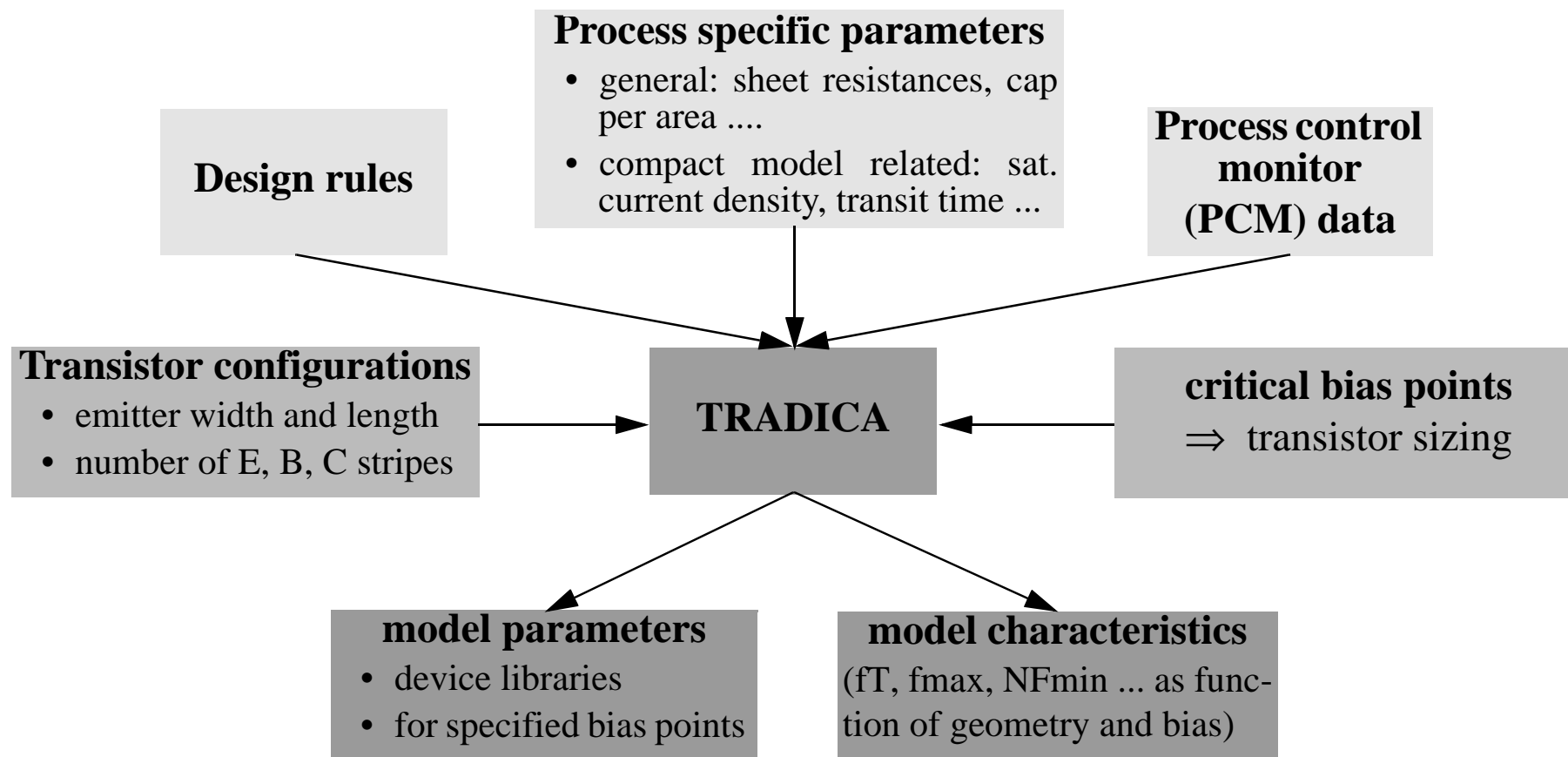
- the x-axis $\Delta \left(\frac{P_0}{A_0} \right) = 2\Delta b_0 \sqrt{\frac{1}{b_0^4} + \frac{1}{l_0^4}}$



- practical example see W. Kraus, ICCAP-Workshop 2002, Berlin, Germany

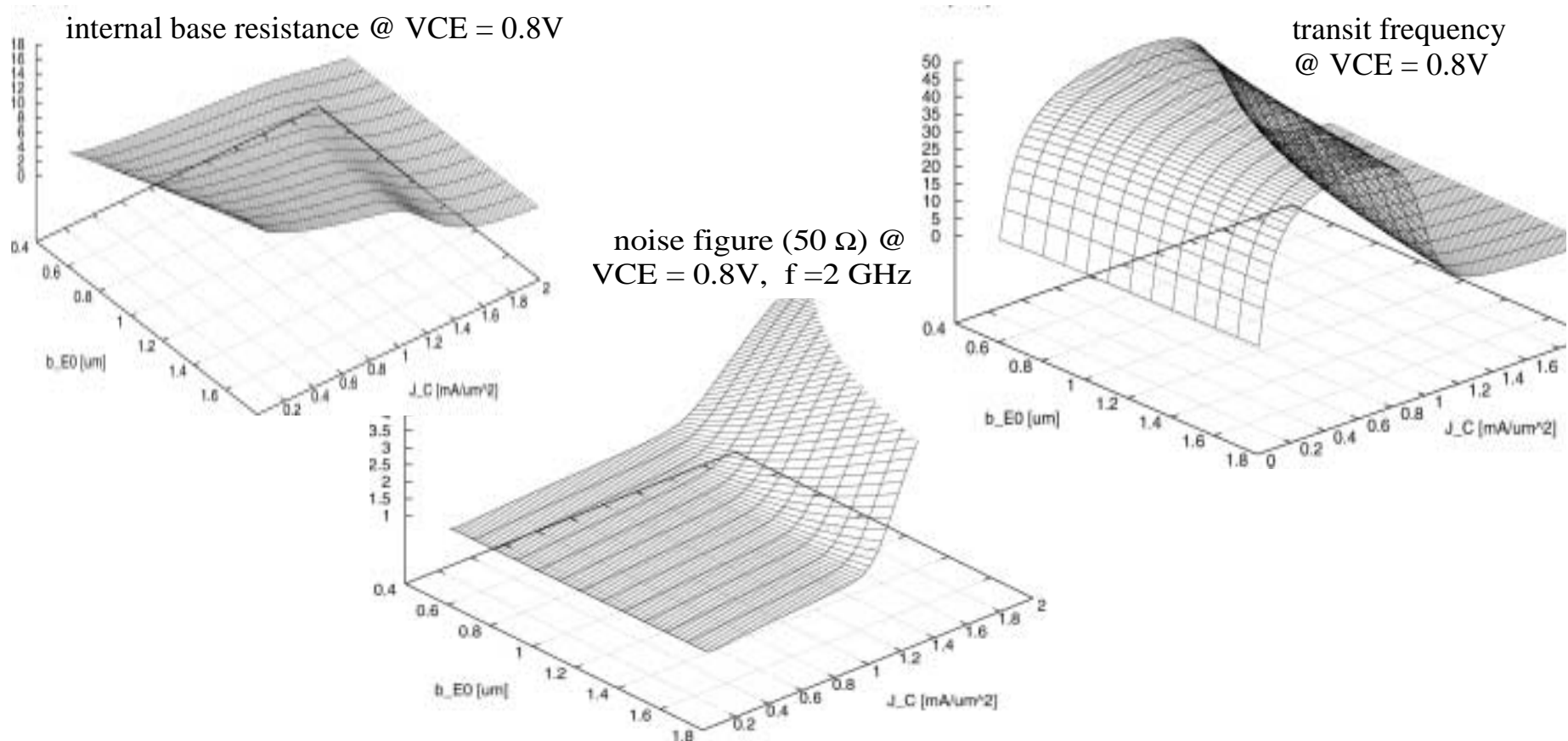
TRADICA overview

- Large variety of bipolar processes requires sophisticated geometry scaling equations that are difficult to integrate and maintain in large variety of (commercial) circuit simulators



Example

model parameters (base resistance, transconductance etc.) and model characteristics (transit frequency, noise figure etc.) can be quickly calculated and displayed as a function of *bias* and *geometry*



Example: fast *generation* of model parameter output for circuit simulators

... bias point information

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TRADICA VERSION 5.0                                07.06.2002

bias dependent vnpn transistor parameters      process:      (Example.DTA      )

bias point:  JC [mA/um^2] = 1.691   VCE [V] = .800   VSC [V] = 3.000   T [K] = 300.0
circuit: SG150                                (SGPM )          f [GHz] = .0 (for NF)
rhoCi [Ohm cm] = .064   (NCi [1/cm^3] =1.63E+17)   rhoSu [Ohm cm] = 6.13

configur.    Tf   CBE   CjCi   rBi   CCBx   rBx   rE   rCx   CCS   gm   fT   fmax   NF
(b 1 nE nB nC)[ps] [fF] [fF] [Ohm] [fF] [Ohm] [Ohm] [Ohm] [fF] [mS] [GHz] [GHz] [dB]
02*026 1 02S1 .7 13.0 .71 59.41 2.9 76.6 19.0 29.7 2.6 33.9 118.2 77.6 1.4
    
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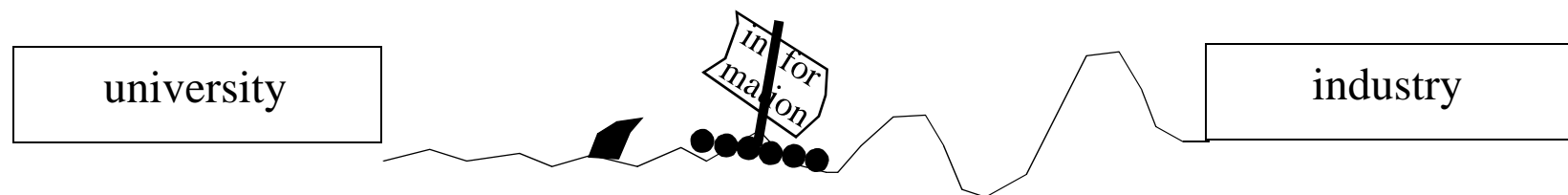
... model library

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* x          AEO= 1* .20* 2.67
* HICUM/ Level 2 / ELDO                                TRADICA V5.0
.SUBCKT N020261S02_01 3 2 1 9
Q      3      2      1      9      MOD
.MODEL MOD NPN level=9 TNOM= 26.85
+ c10=2.20E-32 qp0=4.66E-15 ich=5.82E+01 hjci=0.38 hfc=1.0 hjei=1.00
+ cjei0=2.91E-15 vdei=1.000 zeI= .400 aljei= 2.20
+ cjcI0=6.99E-16 vdcI= .850 zcI= .286 vptcI=3.50E+01
+ t0 =6.81E-13 dt0h= 7.500E-13 tbv1=8.000E-13
+ tef0=1.00E-13 gtfe= 1.00 thcs=3.00E-11 alhc=0.200 fthc=0.426
+ rci0=1.03E+02 vlim= 1.000 vpt= 15.00 vces= .130
+ latb=5.417E+00 latl= .443
+ ibeis=1.75E-20 mbei=1.0100 ireis=1.75E-14 mreI=2.0000
+ alit= .450 alqf= .220
+ favl= 1.000 qavl=8.74E-15
+ rbi0= 77.97 fgeo= .7227 fdqr0= .200 fcrbi= .00 fqi= .9543
+ ibeps=1.51E-20 mbep=1.0100 ireps=1.51E-14 mrep=2.0000
+ ibets=5.58E-16 abet= 40.00
+ cjep0=8.37E-16 vdep= .900 zep= .333 aljep = 1.20 ceox=9.35E-16
+ rcx= 29.68 rbx= 76.61 re= 18.991 ...
+ ibcxS=1.92E-15 mbcx=1.1000
+ cjcX0=2.25E-15 vdcX= .750 zcX= .407 vptcX=2.00E+00
+ ccox=5.89E-16 fbc= .024
+ cjs0=3.81E-15 vds= .793 zs= .250 vpts=1.00E+10
+ vgb= 1.170 alb=-3.00E-03
+ alces=4.00E-04 zetaci= 1.14 alvs=1.00E-03 alt0= 1.00E-03 kt0= 0.00E+00
+ zetarbi= .60 zetarcx= .09 zetarbX= .43 zetare= -.60
+ kf=2.66E+00 af=2.00E+00 krbi=1.00
.ENDS N020261S02_01
    
```

Role of model developer (and university)

- work *must*
 - have sufficient research (theory and experiment) contents to qualify for theses
 - not be service work competing with existing companies to avoid law suits
- implementation of results
 - for demonstration purposes only
 - *must not require* significant manpower (examples: GUI, coding in *several* simulators, ...)
 - cannot use costly EDA tools
- release/deployment *must not require*
 - significant maintenance (e.g., legacy issues, versioning effort, simulator integration verification...)
 - to be forced into legal obligations and responsibility for functionality other than for developed case
 - to be forced to disclose IP into public domain (in violation of existing laws for inventions)



- in contrast to the CMC-caused perception: serious work still needs to be paid for

Proposal for model development and "productization"

Issues

- CMC "approach" **does not work** for bipolar: no funding, too much politics, no common agenda etc.
- **development**: model developer (usually university) receives funding from interested companies and works on *company-specific* topics - consequences and disadvantage:
incoherent model and long-term maintenance issues → overall increase of support effort and cost
- **productization**: does not satisfy research criteria but required & causes significant effort and cost
→ consequence: model developer, e.g. university, cannot provide (sufficient) support

Solution

- only *companies with interest in a particular model* participate in model definition and *contribute to funding pool*
- model developer channels development results into **common** model

→ Advantages

- cost reduction through cost sharing (the larger the number of companies the smaller is the cost/company or the faster is the development and productization process)
- definition of and agreement on common goals is easier and faster compared to a heterogeneous group (such as the CMC) with interests in different model types and a mainly political agenda