A scalable compact model for InP DHBTs

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Outline

- Introduction
- Dedicated test structures
- Device Structure
- Model results
- Conclusions

Introduction

- III/V DHBTs are the fastest bipolar transistors with lab devices showing f_{max} > 1 THz
- Dedicated III/V compact models exist, however
  - usually based on SGPM core
  - either missing important physical effects (included in HICUM)
  - or lacking physics-based description and parameters allowing statistical modeling
- Modeling in III/V community often reduced to parameter fitting of single devices
  - inaccurate
  - limited bias and frequency range
  - no physics-based parameters

  => No truly physics-based geometry scalable models known to be in use

=> circuit optimization and process exploitation severely constrained

=> HICUM enables III/V circuit designers to make better use technology!

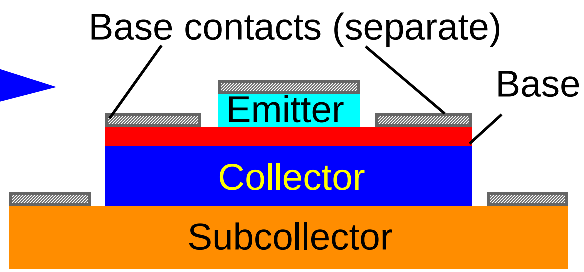
Dedicated test structures

Purpose: process and physics-based linearly independent determin. of EC elements

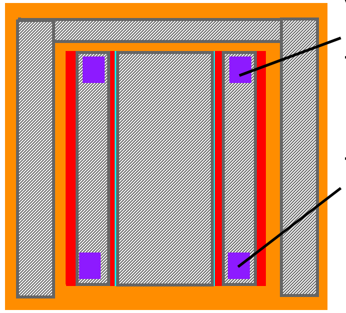
- Dedicated test structures common in SiGe, but usually only limited set (TLMs) used in III/V technology
- Several SiGe structures cannot be used in III/V technology => need for redesign

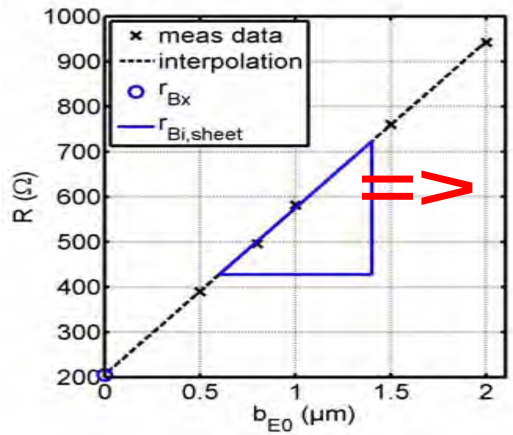
- Example: tetrode structure
  - extraction of R_{Bi} (R_{SBi}) and R_{Cx}
  - realized as walled emitter
- also realized:
  - R_{Bx} contact resistance
  - direct measurement of R_{Cx} and its components
  - thermal coupling structures
  - large-area and multi-finger junction capacitance structures
  - multi-finger transistors
  - PA verification circuits

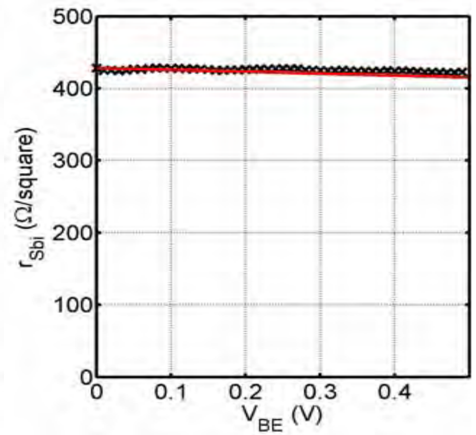
Cross-Section:



Top view:



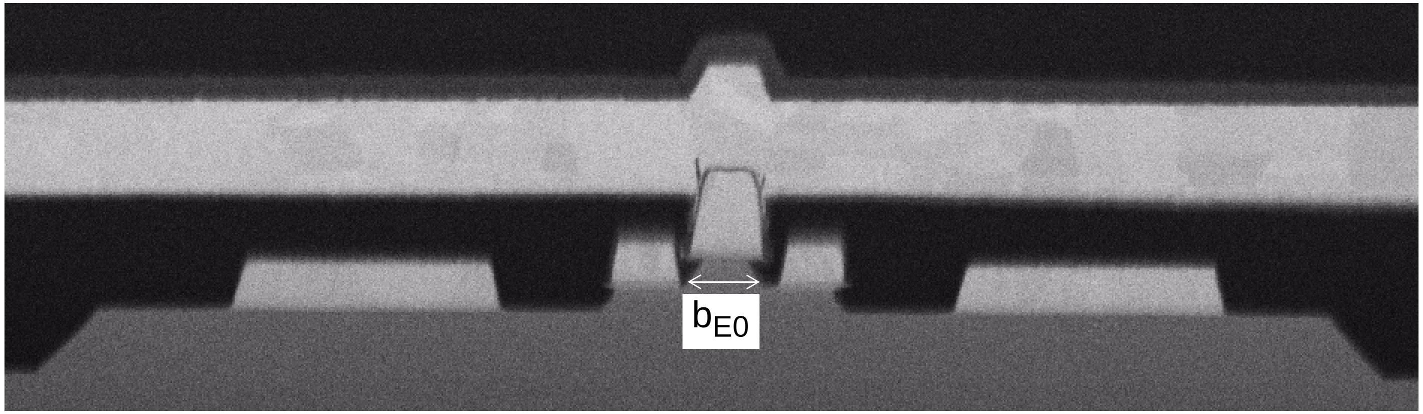


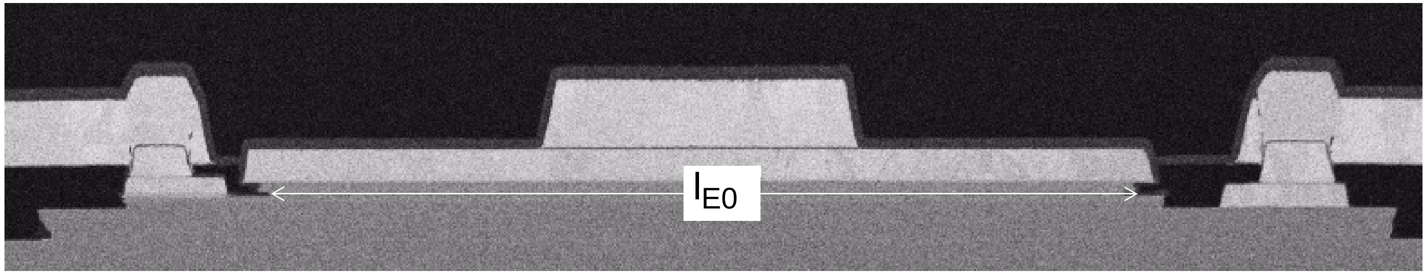


Device Structure

- Determination of *actual* vs. *drawn* device dimensions via FIB probe preparation and SEM/TEM pictures.

- Most important dimensions: emitter junction width (b_{E0}) and length (l_{E0})



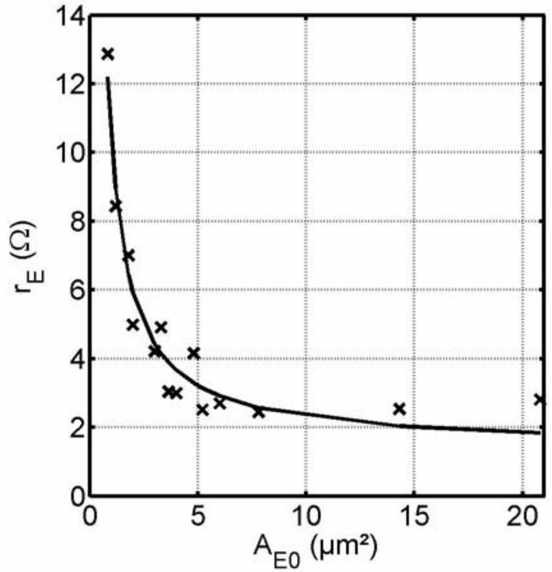


- Drawn dimensions differ strongly from actual dimensions (> 10%)
  - Can cause large deviations in effective electrical emitter area and external base resistance

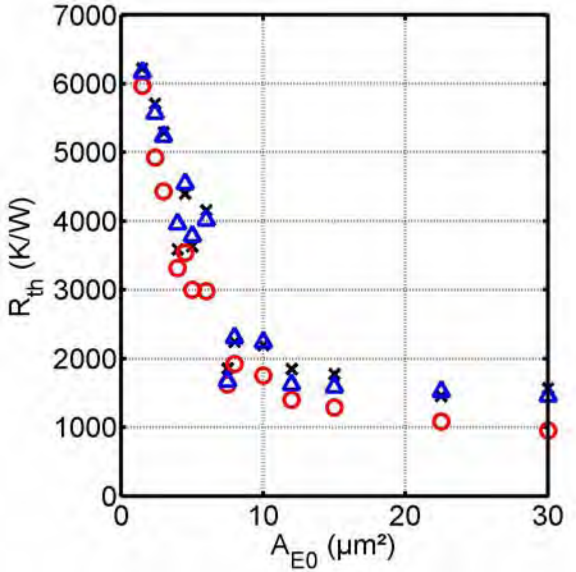
    => incorrect specific electrcial parameters (J, $\overline{C}$) and geometry scaling

Model results

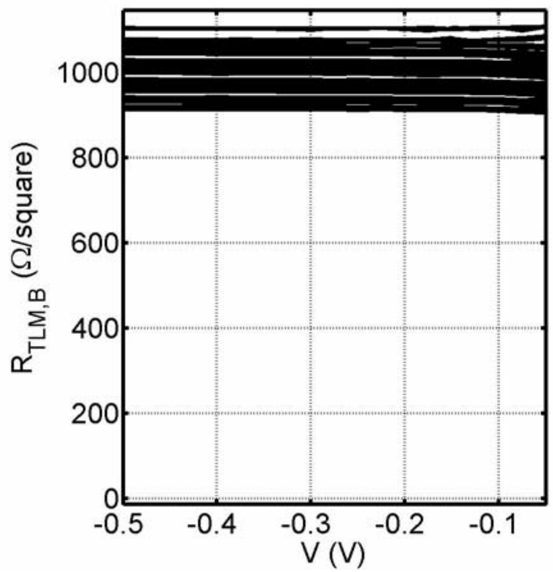
- good scalability with emitter *width and length* observed for most parameters



Extracted (x) and interpolated (line) emitter resistance



Thermal resistance from extraction (x), 3D thermal simulation (O) and geometry scalable model (^)

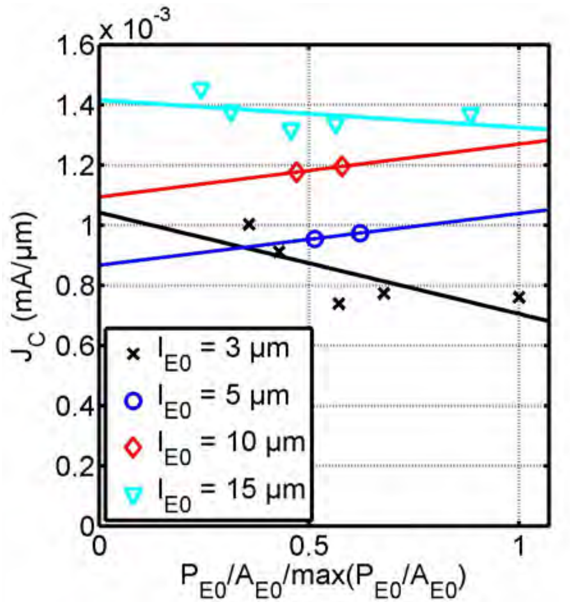


Variation of external base sheet resistance for wafer measured over 15 dies

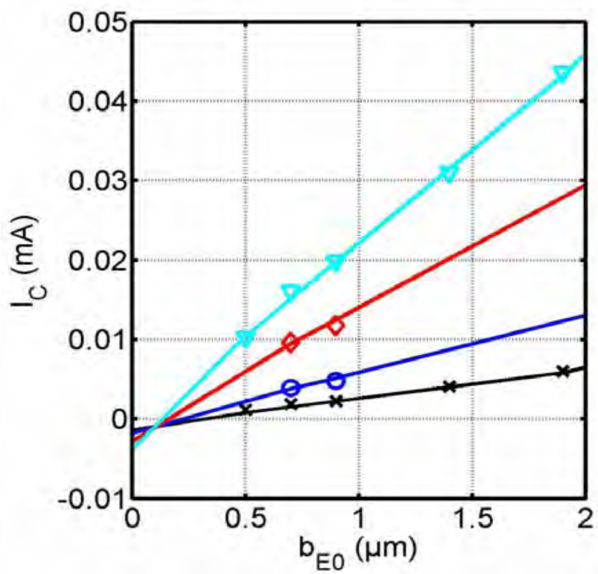
- issues
  - IBC essentially not scalable, IBE only in medium to high bias region
  - process variations (although influence on figures-of-merit comparatively small)

Current scaling

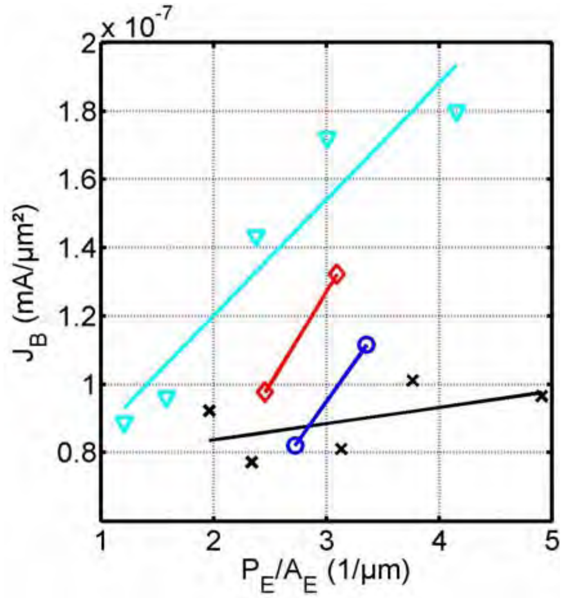
- standard method (P/A separation) ***does not work*** for available structures (identified cause: emitter edge current crowding, corner rounding in short devices)
- collector current scaling: $I_C = I_{C0} + I_{CA}A_{E0} + I_{CP}P_{E0}$ => $I_C = I_{CA}A_E + I_{CP}P_E$
- use long devices to maximize accuracy



Standard P/A separation for collector current, V_{BE} = 0.6 V



Best fit for collector current



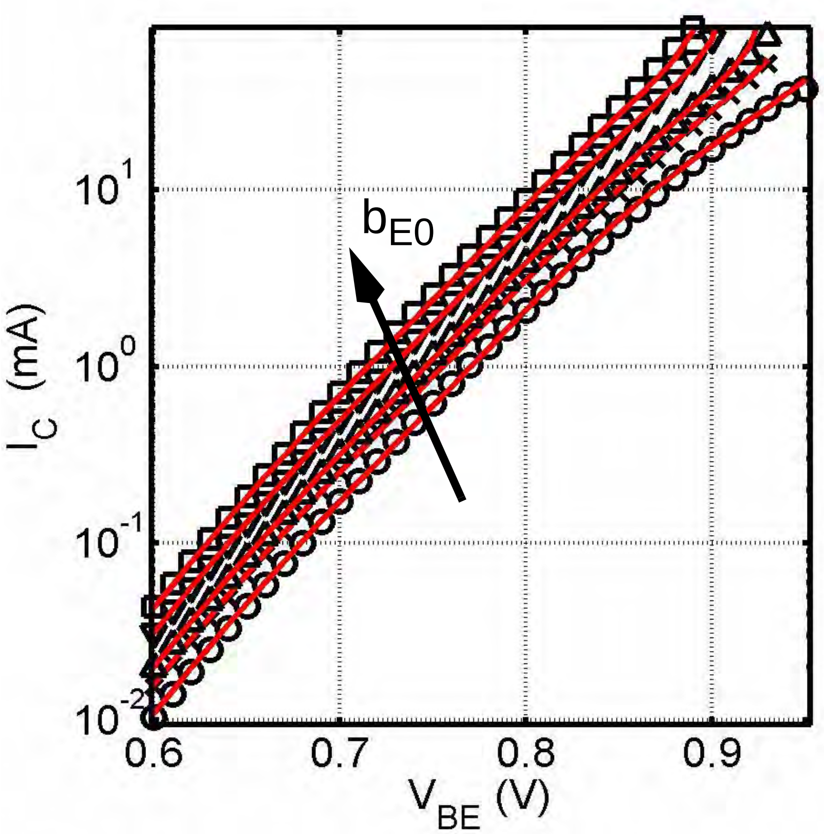
Standard P/A separation for base current, V_{BE} = 0.6 V

- Base current scales only in medium to high bias region

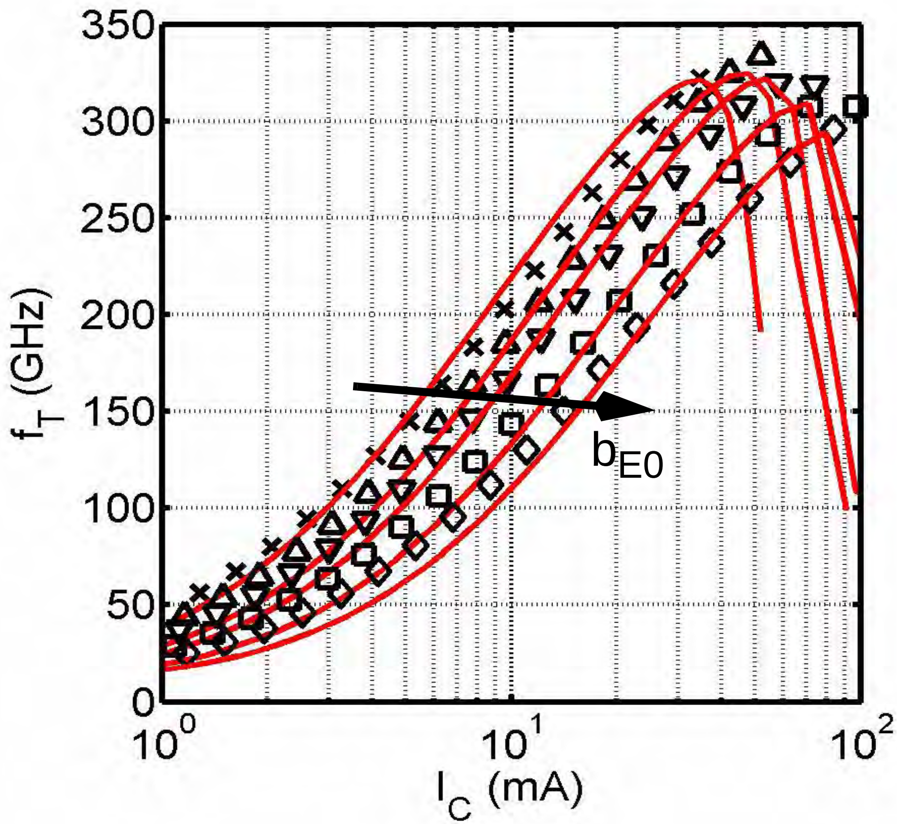
Geometry scaling: bias dependent characteristics

- Comparison of model results for transistors of nominal length 15 µm at 300K

Collector current at V_{BC} = 0



transit frequency at V_{BC} = 0



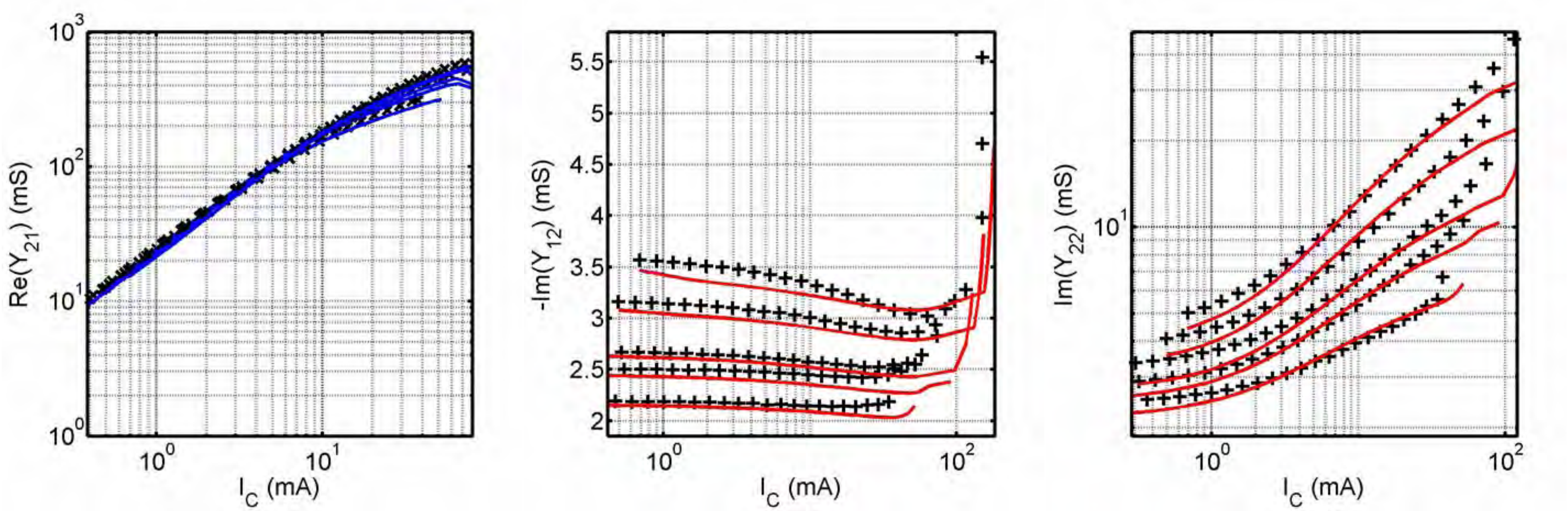
=> good agreement achieved for all devices

Geometry scaling: bias dependent characteristics

- Comparison of model results for transistors of nominal length 15 µm at 300K

y parameters at $V_{BC} = 0$

transconductance | current dependent BC capacitance | current dependent $Im(y_{22})$



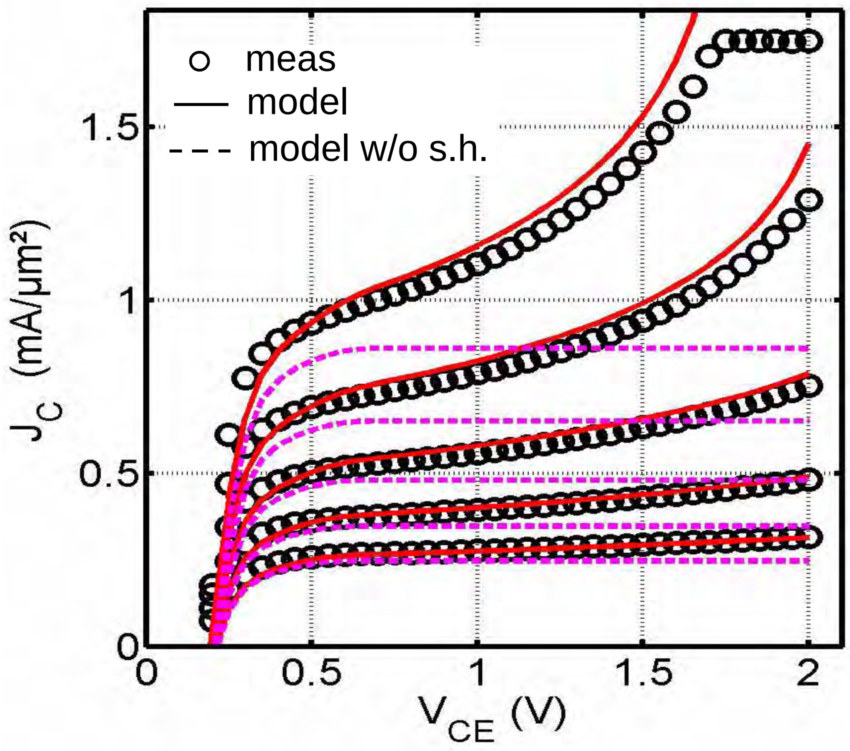
in all figures: b_{E0} = (0.5, 0.8, 1, 1.5, 2)µm

=> good agreement achieved for all devices

Bias dependent characteristics

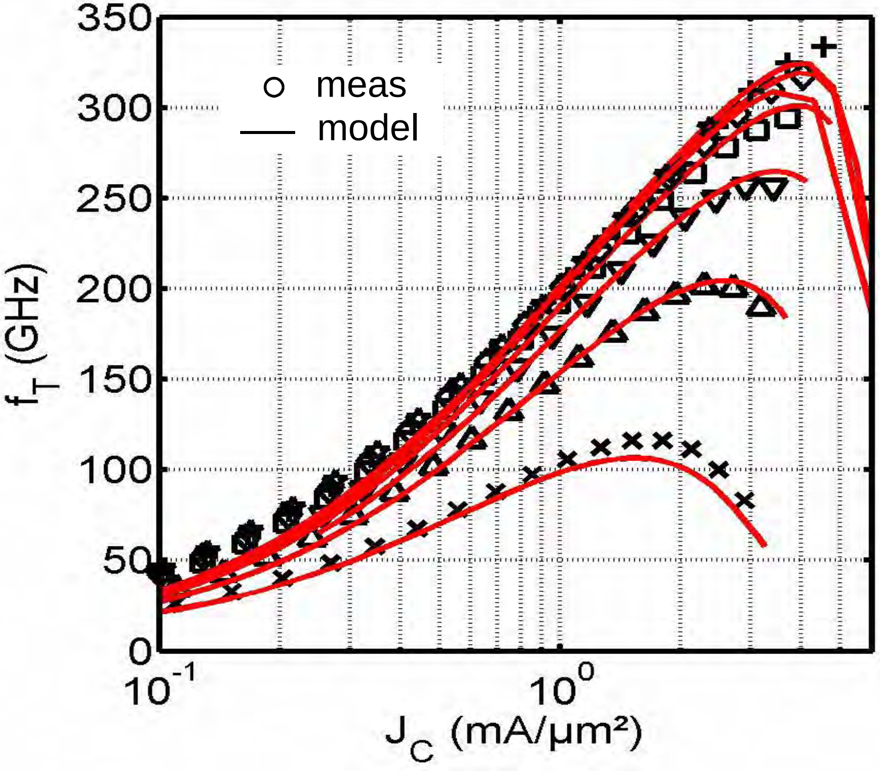
- Comparison of model results and measurement for selected device with $A_{E0} = 0.8x15\ \mu m^2$

output characteristics



V_{BE} = (0.8, 0.815, 0.83, 0.845, 0.86) V

transit frequency



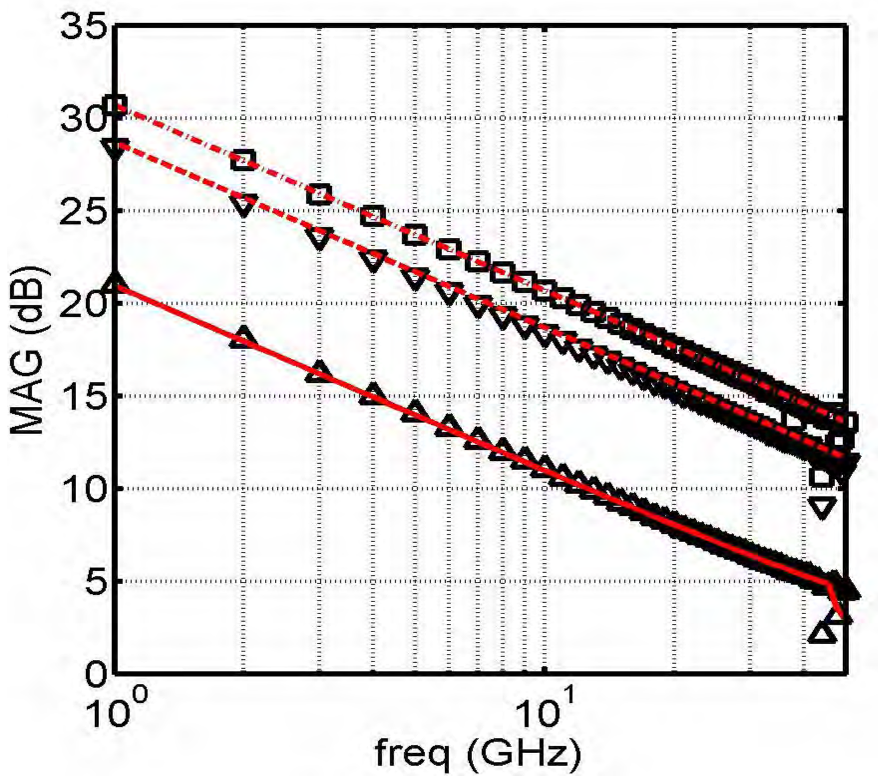
V_{BC} = (-0.25, 0, 0.1, 0.2 0.3 0.4 0.5) V

=> good agreement over wide current and voltage range

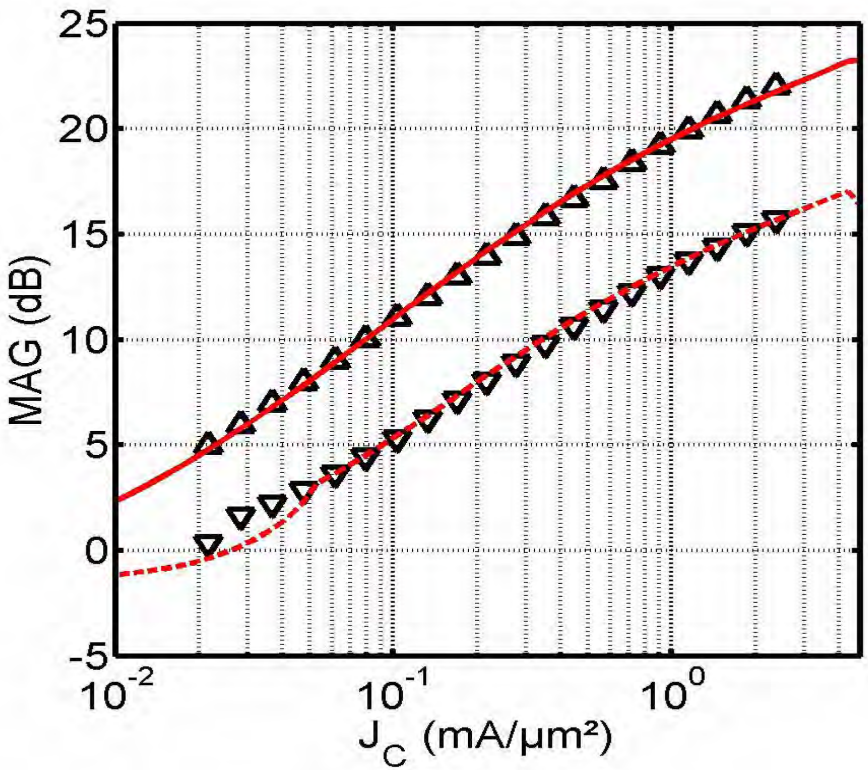
Power gain

- Comparison of model results and measurement for selected device with A_{E0} = 0.8x15 µm²

maximum available gain



V_{BC} = 0 V, JC = (0.1, 0.75, 1.5) mA/µm²



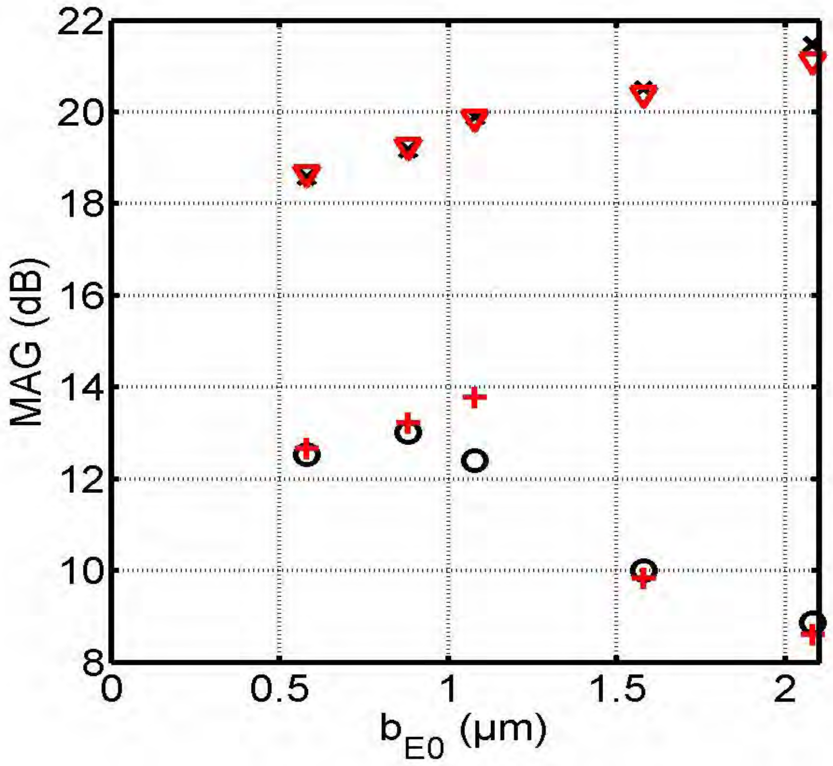
V_{BC} = 0 V, f = (10, 40) GHz

=> good agreement over frequency and bias

Scaling and power

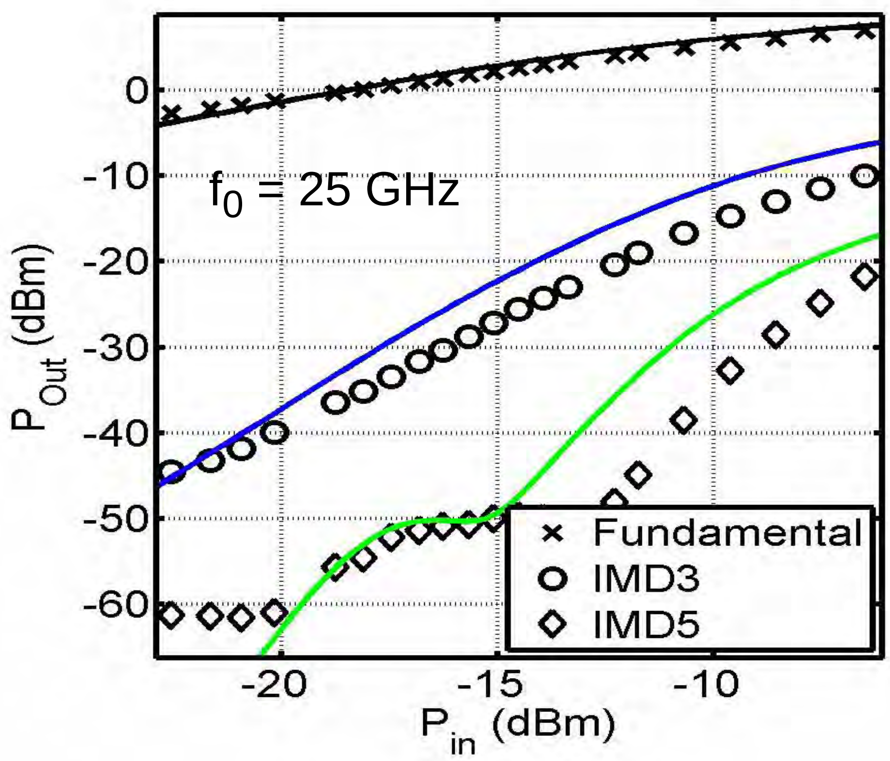
Comparison of model results and measurement

Mag vs. emitter width
l_{E0} = 15 µm



V_{BC} = 0 V, f = (10, 40) GHz

output power and IMD
A_{E0} = 0.8x15 µm²



V_{CE} = 1 V, J_C = 1 mA/µm²

=> good agreement over geometry and for large-signal operation

Conclusions

- A physics-based geometry scalable parameter determination methodology has been applied to InGaAs/InP HBTs
  - includes a complete set of test structures
  - allows process debugging
- (emitter) ***width** and length* scalable HICUM/L2 parameter sets have been extracted
  - enables circuit optimization
  - enables statistical modeling and circuit design
- good agreement between model and measurements over wide geometry, bias and temperature range (f up to 50GHz, limited by pad design)
- issues to be resolved
  - observed geometry scaling and bias dependence for I_{BC} does not follow expectation
  - shape of some y parameters vs. bias to be investigated
- future work
  - improved set of test structures (e.g. more length dependent devices)
  - pulsed AC measurements to obtain sufficient bias range
  - measure up to higher frequencies (110GHz)
  - improved procedures for extracting bias dependent model parameters