

# **2<sup>nd</sup> European HICUM Workshop**

**June 6/7, 2002**

at Dresden, Germany

Chair for Electron Devices and Integrated Circuits (CEDIC)

University of Technology Dresden / GWT, Germany

[http://www.iee.et.tu-dresden.de/iee/eb/eb\\_homee.html](http://www.iee.et.tu-dresden.de/iee/eb/eb_homee.html)

# Agenda

## Day 1

- 09:00 Schroter (CEDIC): Welcome and opening remarks
- 09:15 Scholz (IHP): introduction
- 09:25 Perraud (CAEN): introduction
- 09:35 Gerhardt (Alcatel): introduction
- 09:45 Selim (MentorGraphics): introduction
- 09:50 ALL: brief introduction

### Session I - Modeling

- 10:00 Schroter - Overview on HICUM status
- 11:30 ALL: discussion of model development priorities
- 12:30 Lunch (and information exchange)

### Session II - Parameter extraction

- 14:00 Ardouin (XMOD) – Overview on start-up and services
- 14:30 Berger (STM): „Extraction strategy for a single transistor geometry“

### Session II - Parameter extraction (cont'd)

- 16:00 Malorny (CEDIC) – „Improved Tf and fT determination“
- 16:30 Berkner (Infineon), "Performance comparison using SQ0- and Hicum-Model"
- 16:45 Break

### III. Model implementation, productization and support

17:15 Kraus (Atmel) - "Comparing HICUM V2.1 simulation results (ELDO, ADS, SPECTRE)"

17:30 Lavenir (STM) - "Status of the HICUM implementation in ELDO, SPECTRE, ADS, APLAC, HSPICE.."

18:00 Breakout Session (two groups)

A. Model implementation with demo:

Perraud (CAEN) – „HICUM in SPICE3F3“

B. HICUM development: most important modeling issues and prioritization

19:30 Dinner

## Day 2

### Session IV - Geometry scalable and statistical modeling

09:00 Schroter: "TRADICA V5.0 - Overview and demo"

10:00 Schroter: "Statistical modeling - existing methods, approaches and issues"

11:00 ALL: Discussion

- - technical issues and difficulties
- - suggestions for approaches, requirements
- - viable experimental approaches (PCM test structures, measurements...)
- - available EDA support and infrastructures ? ("circuit surfer", ...)

13:00 lunch

### Session V - Model release and "productization"

14:00 Schroter: "Lessons learned from HICUM productization..."

14:15 ALL: discussion on

- - how much support can be expected from the model developer ?
- - funding for model development and productization - possible approaches
- - are the CMC and its requirements of any use for bipolar models ?

15:00 Adjourn

## Purpose of this workshop

- clarification of questions regarding HICUM (and bipolar transistor modeling)
  - model formulation: physical background and limitations, mathematically
  - status: model development and availability
- model parameter extraction: issues and clarification
  - methods and overall procedure
  - test structures
  - presentation of available results and solutions
- a forum for "free" discussion and exchange of information
  - mostly parameter extraction related (= nature of company business)
  - is a common (not necessarily standardized) model parameter extraction methodology desirable ?
  - is a common set of test structures and measurement procedures desirable ?
  - model enhancement recommendations
- expectation from and role of the model developer (e.g. a university ...)
- workshop (and User's Meeting) vs. political meetings (such as CMC)

# Status of HICUM

in simulators

17 stage ECL ring oscillator ( $0.2 \times 1.7 \mu\text{m}^2$  transistors of a  $0.18 \mu\text{m}$  BiCMOS process)

simulator	tail current [mA]	TRAN t_stop [ns]	volt. swing [mV]	total delay [ns]	initial/DC solution time [s]	TRAN analysis time [s]	CPU
SPECTRE	0.056	4	196	1.79	0.5	32.76	Sparc5
ELDO	0.056	4	194	1.81	0.1	18.53	Pentium3
SPECTRE	3.6	2	196	0.307	0.07	47.68	Sparc5
ELDO	3.6	2	197	0.297	0.1	15.49	Pentium3

# Status of HICUM

(applications)

- directly related papers since last workshop:
  - M. Schroter, T.-Y. Lee and M. Racanelli, “A scalable model generation methodology of bipolar transistors for RF IC design“, PA workshop, UCSD, 2001; similar talk also at BCTM 2001.
  - M. Schroter, “The advanced compact bipolar transistor model HICUM - An overview”, IEEE Circuits and Devices Magazine, May 2002, pp. 16-25.
  - D. Berger, D. Celi, M. Schroter, M. Malorny, T. Zimmer, and B. Ardouin, “HICUM parameter extraction flow for a single transistor geometry”, accepted at BCTM, Sept./Oct. 2002.
  - M. Schroter, S. Lehmann, and H. Jiang, “HICUM/Level0 - a simplified compact bipolar transistor model”, accepted at BCTM, Sept./Oct. 2002.
- CMC meeting in 4/02: presentation see CEDIC web-site and this workshop  
[http://www.iee.et.tu-dresden.de/iee/eb/eb\\_homee.html](http://www.iee.et.tu-dresden.de/iee/eb/eb_homee.html)
- **if interest: HICUM User’s Meeting at BCTM 2002** on Sunday, Sept. 29, 7-9 pm in Monterey, CA
  - suggestions for topics and organization are welcome

## HICUM development (1/2)

Main target applications: advanced SiGe technology ( $f_T > 200$  GHz and LEC-HBT)

- main effects in (advanced) SiGe HBTs
  - improved physics-based collector model (incl. high-current effects, barrier effects, avalanche, current dependent BC capacitance)
  - high-frequency noise
  - high-frequency (single- two-tone) distortion
  - Low-Emitter Concentration (LEC) SiGe HBTs
- model hierarchy (in conjunction with TRADICA)
  - Level0: finish formulation, release Verilog-code for evaluation and simulator integration
  - Level4: variable multi-transistor model (for critical applications, e.g. pinch-in effect)
    - for both model levels: automatic parameter generation from Level2 by TRADICA (already available for Level0)
- predictive and statistical modeling:
  - existing predictive equations to be extended to advanced SiGe by incorporating explicit BC barrier dependence in transit time model
  - verify for various SiGe processes (high-frequency and circuit applications)
  - extend corner case generation to multiple target FoMs - needed ?

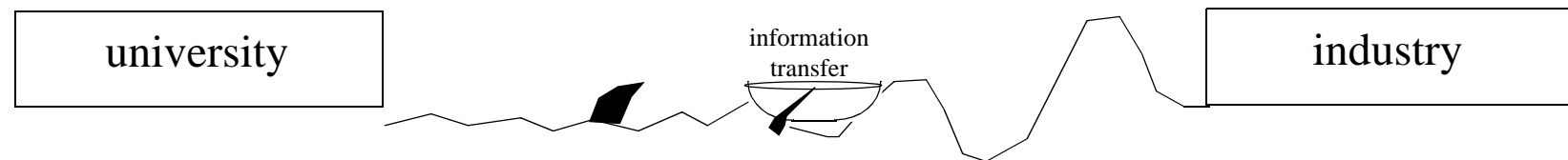
## HICUM development (2/2)

- parameter extraction
  - geometry scalable modeling:
    - continuous adaption to process development (extensions of existing and new methods)
    - extend user control during auto-extraction for HICUM/L0 and SGPM from HICUM/L2
  - single transistor procedure and implementation (for HICUM/L0)
  - tighter integration with TRADICA (optional), e.g., at XMOD, JazzSemi, ...
- thermal modeling
  - geometry scaling (single device), including junction isolation, deep trench and metallization
  - multi-transistor model with thermal coupling (s. DJW's BCTM/JSSC paper)
- related activities (partially as special cooperations = proprietary problems and solutions)
  - III-V HBTs
  - backend parasitics (for single device)
  - substrate coupling (geometry scaling for single device) using *fast* computation methods



## Role of model developer (and university)

- work *must*
  - have sufficient research (theory and experiment) contents to qualify for theses
  - not be service work competing with existing companies to avoid law suits
- implementation of results
  - for demonstration purposes only
  - *must not require* significant manpower (examples: GUI, coding in *several* simulators, ...)
  - cannot use cost-expensive EDA tools
- release/deployment *must not require*
  - significant maintenance (including, e.g., legacy issues, extensive versioning effort)
  - to be forced into legal obligations and responsibility for functionality other than for developed case
  - to be forced to disclose IP into public domain (in violation of existing laws for inventions)



# Proposal for model development and "productization"

## Issues

- CMC "approach" **does not work** for bipolar: no funding, too much politics, no common agenda etc.
- **development**: model developer (usually university) receives funding from interested companies and works on *company-specific* topics - consequences and disadvantage:  
incoherent model and long-term maintenance issues → overall increase of support effort and cost
- **productization**: does not satisfy research criteria but requires significant effort and cost  
→ consequence: model developer, e.g. university, cannot provide (sufficient) support

## Solution

- only *companies with interest in a particular model* participate in model definition and *create funding pool*
- model developer channels development results into **common** model

## → Advantages

- cost reduction through cost sharing (the larger the number of companies the smaller is the cost/company or the faster is the development and productization process)
- definition of common goals by all participating companies is obtained easier and faster compared to a group (such as the CMC) with interests in different model types and politics