HICUM/Level0 - A simplified compact bipolar transistor model

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Introduction

- motivation
  - circuit design: need quick evaluation of basic circuit functionality, partially based on "hand"/symbolic calculations
  - only few very critical transistors within a circuit usually require sophisticated and very accurate model
  - other devices (e.g. variable capacitors (varactors)) only need to make use of transistor model portions
  - parameter determination: sometimes required only for “single geometry transistor” (such as a discrete devices, many GaAs HBT processes) → insufficient information for physical geometry model

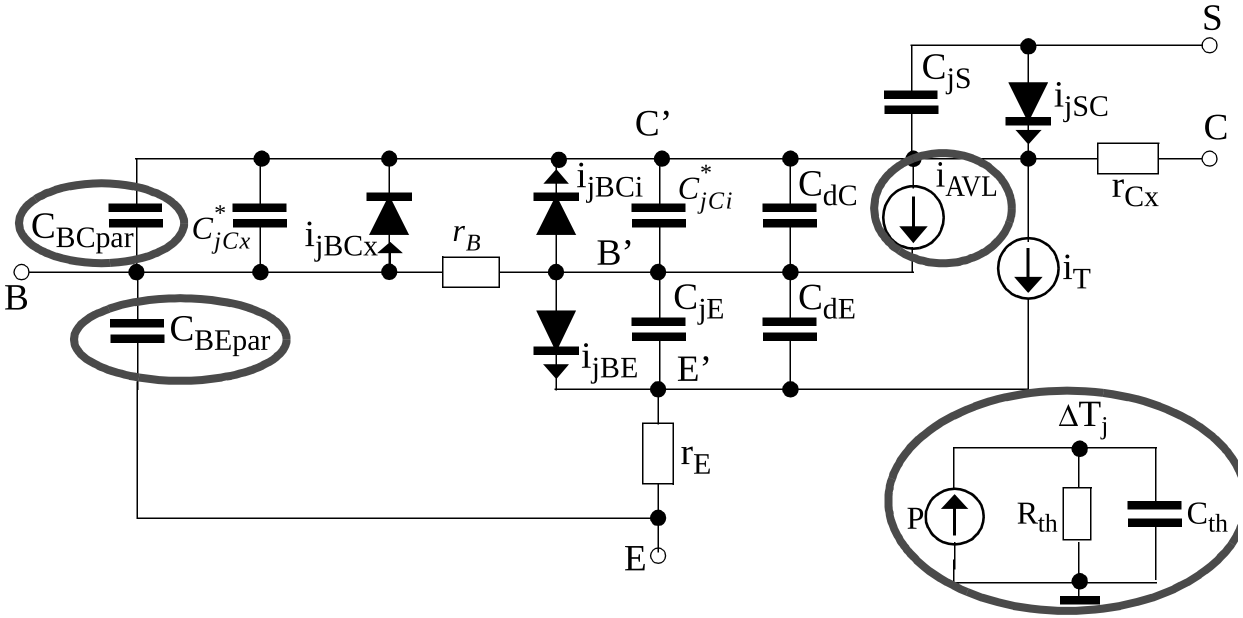
⇒ simple model (EC, equations, number of parameters): HICUM/Level0

- goals
  - keep complexity similar to SPICE-GP-model, but eliminate its most important deficiencies
  - parameter determination: insignificant extra effort (compared to HICUM/L2)
  - as physical as possible model formulation and parameters:
    - enable predictive and statistical design (e.g., for larger circuits)
    - provide modeling and design engineers with information on fundamental model limitations
  - reduce simulation time
  - enable evaluation, wide distribution and rapid simulator integration by "generic" implementation

Equivalent circuit

- keep similarity to the standard SGPM (which circuit designers are familiar with)

- additions to SGPM (in EC):
  - BC avalanche current
  - self-heating
  - parasitic (isolation) capacitances

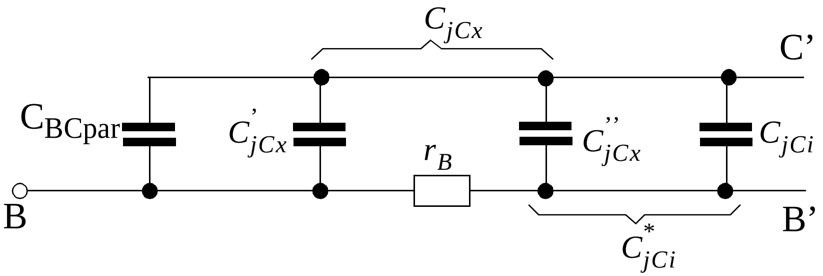


- most important assumptions (with HICUM/L2 as reference)
  - lumped base resistance element r_B
  - lumped BE depletion capacitance $C_{jE} = C_{jEi} + C_{jEp}$
  - less detailed (with respect to h.f. applications) partitioning of BC capacitance C_{BC}
  - no substrate transistor and substrate coupling network (can be added externally via subcircuit)
  - no BE tunnelling current and small-signal h.f. emitter current crowding

Model equations

depletion charges and capacitances

- BE depletion capacitance C_{jE}
  - HICUM/L2 equation with accurate limitation towards high forward bias
  - impact of missing C_{jEi} on GICCR is captured by non-ideality coefficient $m_{Cf} \cong 1 + \dfrac{h_{jei} C_{jEi,op} V_T}{Q_{p0}^*}$
- BC depletion capacitance C_{jC}
  - flexible partitioning of BC capacitance (depletion and isolation) across total base resistance:



  - parameters: C_{jCx0}, f_{BC} (= $\dfrac{C_{jCi0} + C''_{jCx0}}{C_{jC0}}$), [$C_{jCi0}$]
  - if C_{jCi0} is unknown (e.g., single device extraction)

    $$\Rightarrow C''_{jCx0} = 0 \quad , \quad C_{jCi0} = f_{BC} C_{jC0}$$

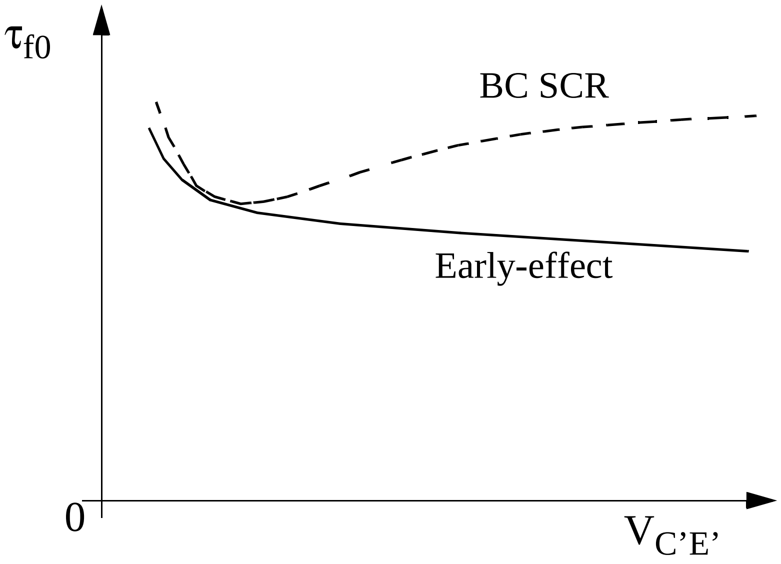
  - if C_{jCi0} is known (e.g., geometry scaling) $\Rightarrow C''_{jCx0}(f_{BC}, C_{jCi0})$
  - impact of C_{jCi} on GICCR ("forward" Early-effect) is captured by the parameter $V_{Ef} = \dfrac{Q_{p0}^*}{h_{jci} C_{jCi0}}$
  - collector punch-through effect included in both C_{jCi} and C_{jCx} (cf. HICUM/L2)

Minority charge and transit time

- simplified HICUM/L2 formulation without bias dependent geometry scaling (LATB=LATL=0)
- forward transit time: $\tau_f(I_{Tf}, V_{C'E'}) = \tau_{f0}(V_{C'E'}) + \Delta\tau_f(I_{Tf}, V_{C'E'}) \Rightarrow$ charge $Q_f = \int_0^{I_{Tf}} \tau_f \, di$

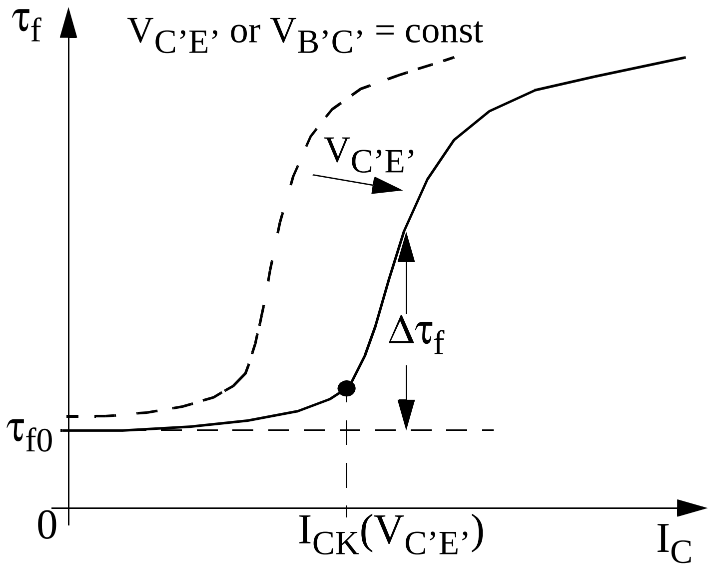
low-current component τ_{f0} :

Early-effect and transit time through BC-SCR



high-current component $\Delta\tau_f$:

additional charge storage in neutral E, B, C



- inverse component: $Q_r = \tau_r I_{Tr}$ with τ_r = const

Transfer current formulation

- simplification from GICCR:

$$i_T = \frac{i_{Tfl} - i_{Trl}}{1 + \Delta q_{hc}(i_{Tfl})}$$ with the low-current components

$$\begin{cases} i_{Tfl} = \dfrac{\boxed{I_S^*}\exp\left(\dfrac{v_{B'E'}}{\boxed{m_{Cf}}V_T}\right)}{q_{p,T}} \\ i_{Trl} = \dfrac{\boxed{I_S^*}\exp\left(\dfrac{v_{B'C'}}{\boxed{m_{Cr}}V_T}\right)}{q_{p,T}} \end{cases}$$

and ideality factors $m_{Cf} = \dfrac{i_{Tf}/V_T}{g_m}$ and m_{Cr}

- normalized hole charge includes bias dependent forward

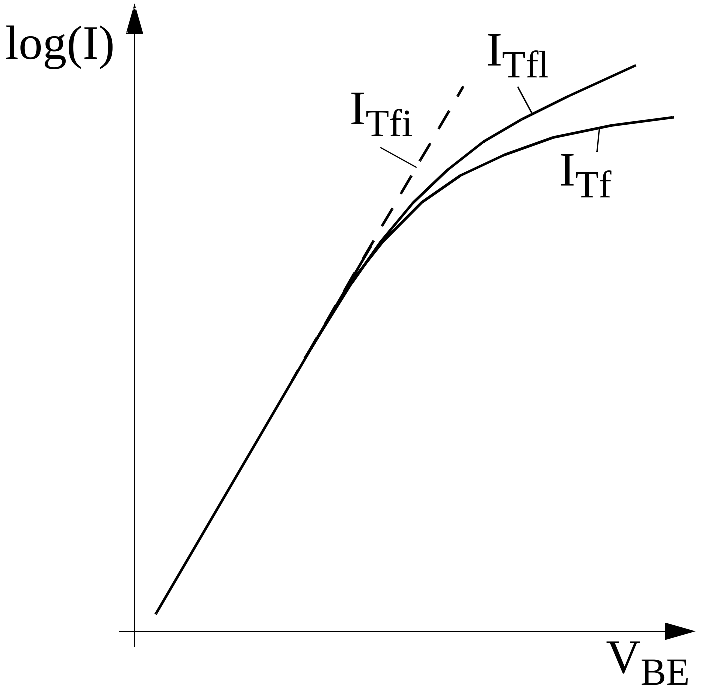
Early effect: $q_{p,T} = 1 + \dfrac{q_{jCi}}{\boxed{V_{Ef}}} + \dfrac{i_{Tfl}}{\boxed{I_{CKf}}} + \dfrac{i_{Trl}}{\boxed{I_{CKr}}}$ with parameters V_{Ef}, I_{CKf}, I_{CKr}

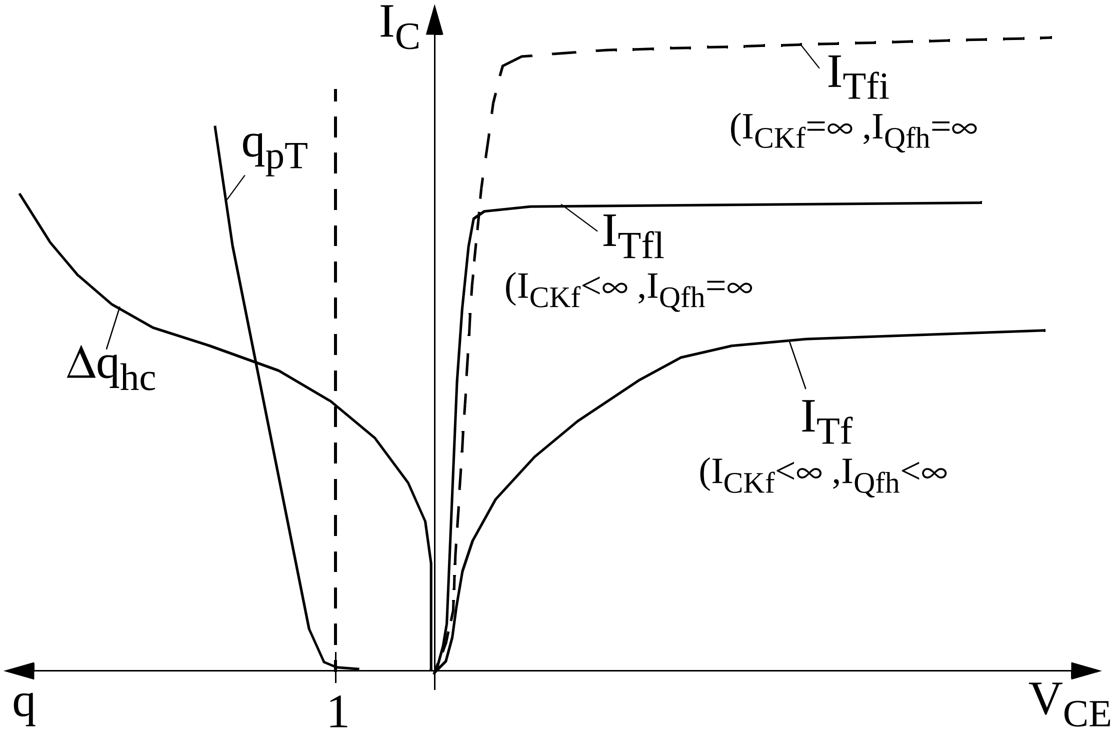
- simplified high-current correction, $\Delta q_{hc}(i_{Tfl}) = \dfrac{i_{Tfl}}{\boxed{I_{Qfh}}}\dfrac{w^2(i_{Tfl})}{q_{p,T}}$, with $w^2(i_{Tfl})$ from $\Delta\tau_f$

⇒ explicit equation for i_T using main formulation of high-current charge modeling

transfer current (cont'd)

visualization of equations and parameters





base current components

- back injection into emitter across *perimeter* and *bottom* BE junction are merged into a single diode:

$$i_{jBE} = \boxed{I_{BES}}\left[\exp\left(\frac{v_{B'E'}}{\boxed{m_{BE}}V_T}\right) - 1\right] + \boxed{I_{RES}}\left[\exp\left(\frac{v_{B'E'}}{\boxed{m_{RE}}V_T}\right) - 1\right]$$

- injection across internal and external BC junction:

$$i_{jdiode} = \boxed{I_{diodeS}}\left[\exp\left(\frac{v_{jun}}{\boxed{m_{jun}}V_T}\right) - 1\right]$$

with “diode” = {BCx, BCi} and “jun” = {BC’, B’C’}

- BC weak avalanche current

$$i_{AVL} = \boxed{k_{AVL}}\frac{I_{Tf}}{C_c^{1/z_{Ci}}}\exp\left(-\boxed{e_{AVL}}\,C_c^{\left(\frac{1}{z_{Ci}} - 1\right)}\right)$$

with $C_c = C_{jCi}(v_{B'C'})/C_{jCi0}$ and model parameters k_{AVL}, e_{AVL}

- injection across collector-substrate junction:

$$i_{jSC} = \boxed{I_{SSC}}\left[\exp\left(\frac{v_{S'C'}}{\boxed{m_{SC}}V_T}\right) - 1\right]$$

Base resistance

- split in bias independent external component, r_{Bx}, and bias dependent internal component, r_{Bi}

- internal component

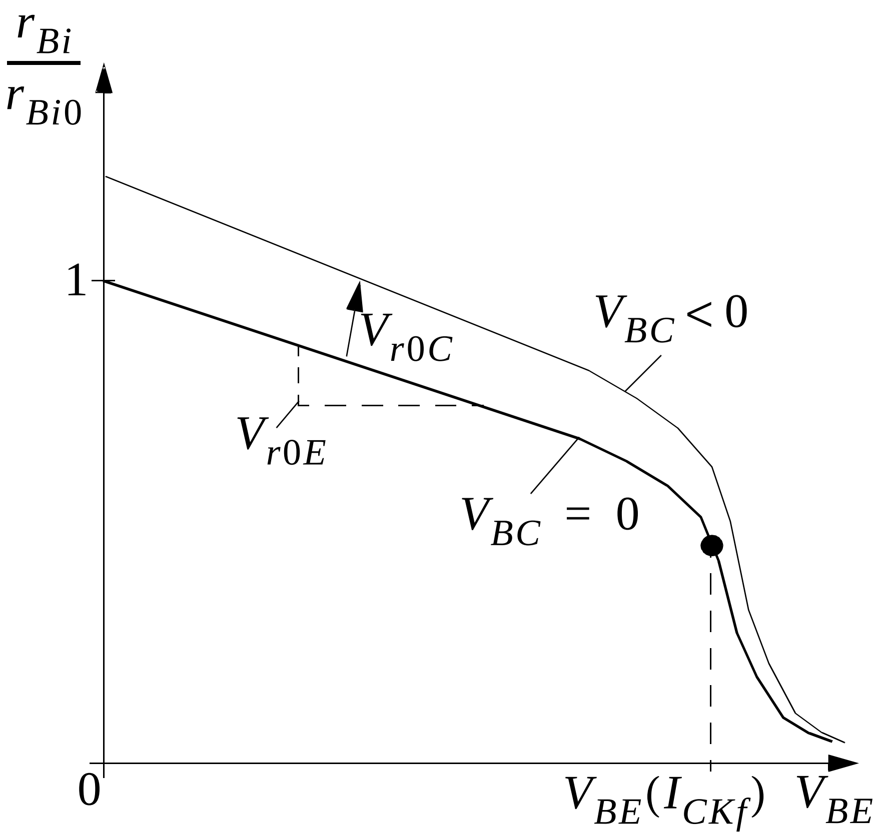
$$r_{Bi} = r_i \ \psi(\eta)$$

includes *both* conductivity modulation

$$r_i = \frac{\boxed{r_{Bi0}}}{1 + \dfrac{q_{jE}}{\boxed{V_{r0E}}} + \dfrac{\overset{*}{q}_{jCi}}{\boxed{V_{r0C}}} + \dfrac{I_{Tf}}{\boxed{I_{CKf}}} + \dfrac{I_{Tr}}{\boxed{I_{CKr}}}}$$

... *and* emitter current crowding

$$\psi(\eta) = \frac{\ln(1+\eta)}{\eta} \quad , \quad \eta = \boxed{\overset{*}{f}_{geo}} \frac{r_i I_{jBE}}{V_T}$$



Parameter extraction

(... and generation)

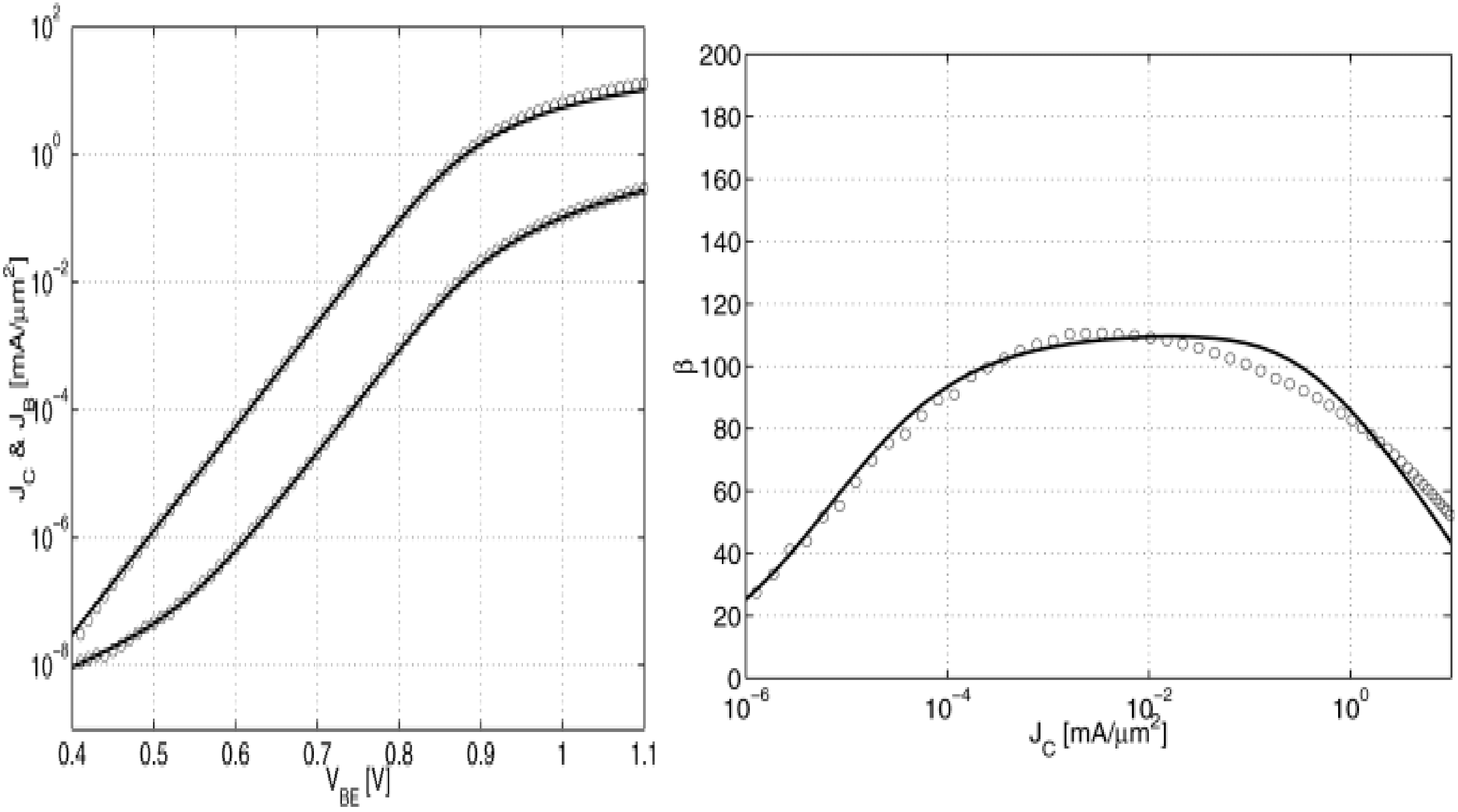
- geometry scalable model parameters can be generated by TRADICA from HICUM/L2 parameters
  $\Rightarrow$ **no extra effort for parameter extraction**

- single transistor geometry:
  - apply existing methods presented, e.g., in papers by
    - B. Ardouin et al. @ BCTM 2001
    - D. Berger et al. @ BCTM 2002
  - partially already implemented in *HICUM-Aperitiv* toolkit (XMOD Technology/Agilent)
  - can use or adapt many methods available for SGPM, except
    - transit time τ_f
    - BC avalanche current

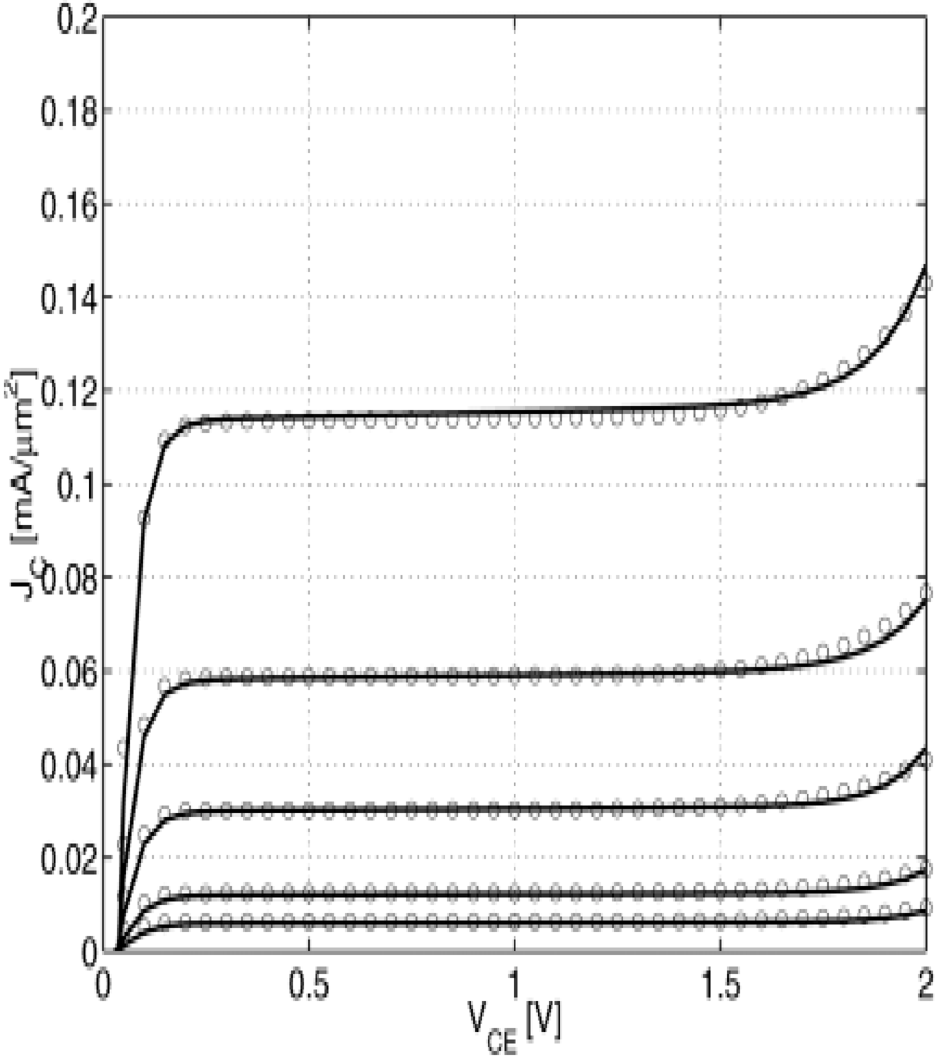
Experimental results

0.35 µm SiGe BiCMOS (high performance transistor version)

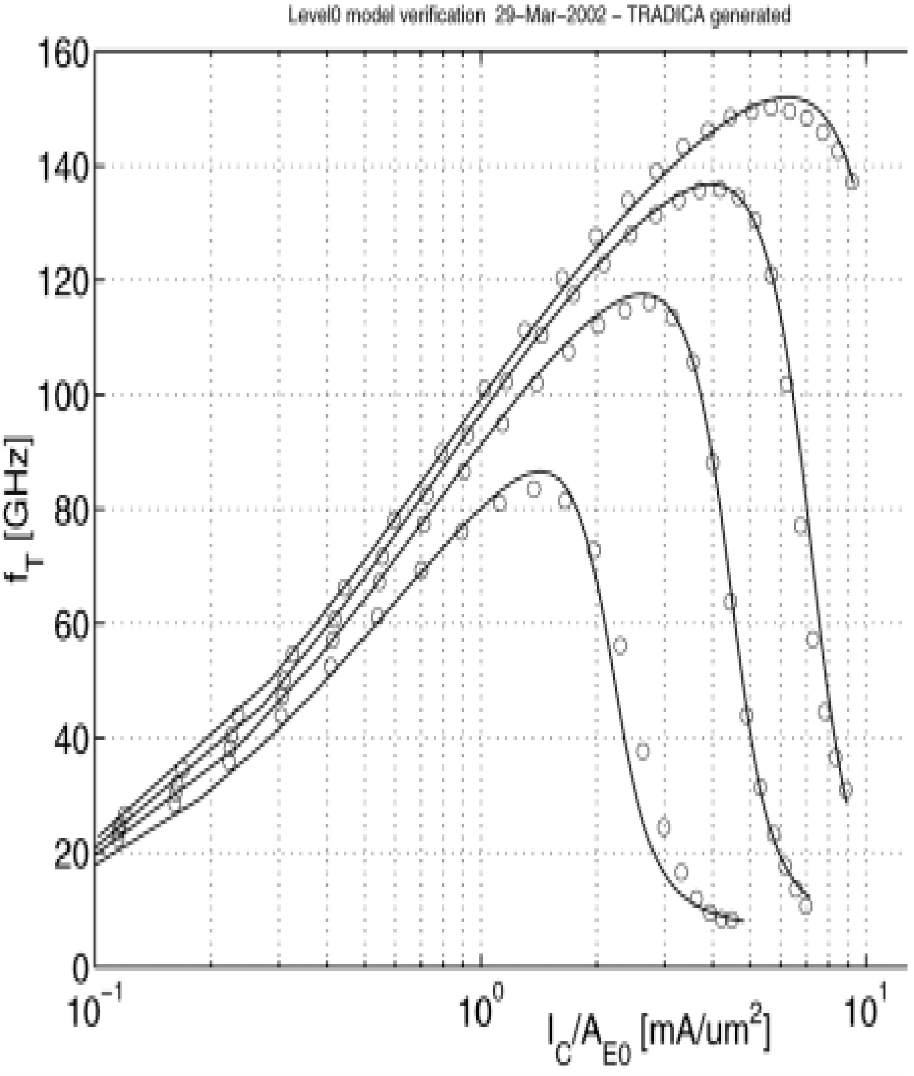
collector current current gain



output characteristics (I_B = const)



transit frequency



Implementation

- existing code implemented in Verilog-A ⇒ advantages:
  - easy model distribution
  - evaluation by others (via all major simulators) for relevant operation modes and circuits
  - easy implementation (once familiar with simulation system), since no need for derivatives
  - significantly reduces maintenance and support of compiled model integration through
    - symbolic generation of derivatives
    - (possibly even) automated code generation
    - customized test data generation by implementation party

- compiled model: implement HICUM/L0 as a separate model
  ⇒ full advantage of the speed improvement

⇒ approach can significantly reduce time to model deployment

Summary of model features

(and improvements with respect to the SGPM)

- derived from HICUM/L2 formulation (= accurate reference)
- simple equivalent circuit with the same topology as the SGPM
- improved transfer current equation:
  - bias dependent forward Early-effect
  - non-ideality coefficient (avoids ambiguities in parameter extraction for BJTs)
  - simple high-current/quasi-saturation correction
- improved transit time and minority charge model:
  - quicker and more reliable parameter extraction
  - significantly higher accuracy (based on HICUM/L2 formulation)
- internal base resistance: more accurate and physics-based description of both conductivity modulation *and* emitter current crowding.
- (Weak) avalanche breakdown in the base-collector junction.
- includes parasitic (bias independent) BE and BC capacitances
- self-heating (first-order network)
- NQS effects for i_T *and* Q_f as function of *bias*
- geometry scaling through automated parameter generation from HICUM/L2 (e.g., TRADICA)

  ⇒ no extra effort for parameter extraction

Conclusions

- HICUM/L0 is a compact model with simplicity of SGPM, but
  - eliminating its major deficiencies
  - clear (physical) meaning of equations, parameters, and definition of validity range limitations

- design point of view:
  - understandable
  - fast simulation
  - further quick simplifications for initial design phase / hand calculations

- parameter determination point of view:
  - single device parameter extraction
  - automated generation of geometry scalable parameters from HICUM/L2

- Verilog-A implementation enables rapid evaluation, wide distribution

HICUM/L0 is a step towards building a compact model hierarchy addressing the widely varying circuit application demands

Experimental results

SiGe BiCMOS process