3d European HICUM Workshop

A Geometry Scalable Parameter Extraction Method and Application to HICUM

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Introduction

- A scalable extraction methodology is described in order to obtain specific parameters for HICUM model. The goal is to offer more flexibility to circuit designers with respect to the choice of device configurations and sizes using HICUM scaling equation [1] as preprocessor in circuit simulators

- These specific parameters then can also be used as input parameters for TRADICA.

- Main of the scalable parameters are determined from long transistors with constant emitter length and variable emitter width (L>>W) to have significant P/A variation.

- The geometry independent parameters are extracted on one long transistor (L>>W).

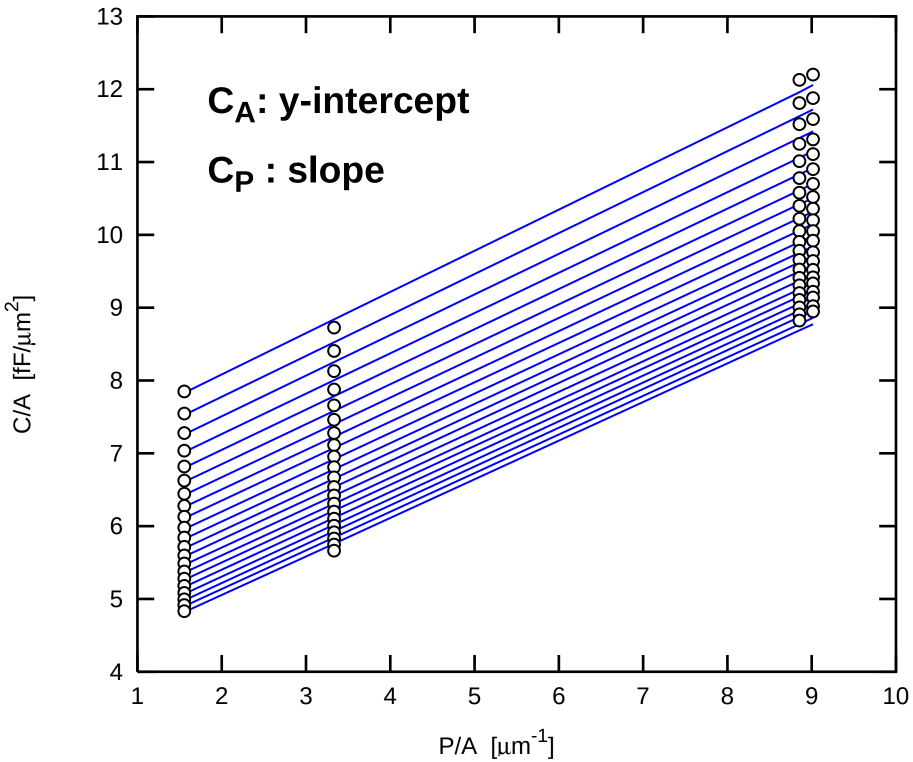
- Many methods used for the extraction of parameters for a single transistor [2] are employed to obtain the specific parameters. The only difference is the data (current densities, specific components, ...) to be treated.

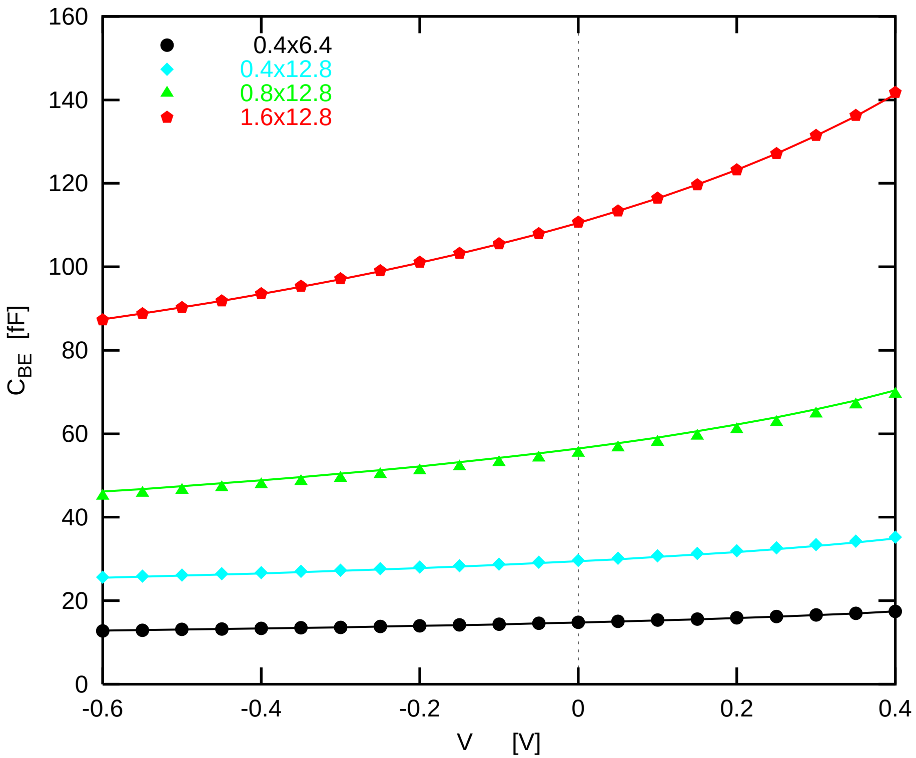
Specific parameters extraction flow

Step	Specific Parameter	Area	Transistors	Measurement
1	Bottom and periphery components of the CBE	real emitter	different widths same length	C(V) extracted from cold-S parameters
2	Bottom and periphery components of the CBC	drawn emitter (SIC)	different widths same length	C(V) extracted from cold-S parameters
3	Specific avalanche parameters	real emitter	different widths different lengths	I_B, $I_C(V_{CB})$ @ V_{BE}=0.7V
4	Effective emitter size (γ_C), specific parameters for I_C at low injection	real emitter	different widths same length	$I_C(V_{BE})$ @ V_{BC}=0V
5	Effective emitter size (γ_{BW}, γ_{BL}), specific parameters for I_B at low injection	real emitter	different widths different lengths	$I_B(V_{BE})$ @ V_{BC}=0V
6	Specific emitter resistance	real emitter	different widths different lengths	$I_C(V_{BE})$ @ V_{BC}=0V
7	Specific external collector resistance	real dimensions	specific test structures	
8	Specific internal and external base resistance	real dimensions	specific test structures	
9	Internal and perimeter components of τ_0	real and effective emitter	different widths different lengths	$f_T(I_C)$ @ V_{BC}=0V
10	Specific component of internal collector resistance	real emitter	different widths different lengths	$I_{CK}(V_{CE}$=cte)

Specific capacitances

- Calculation of parasitic capacitances Cp: back-end + oxide capacitances for all transistors.
- Extraction of total capacitances C_T using “cold-S” measurement.
- Extraction of specific capacitance using C_T - Cp



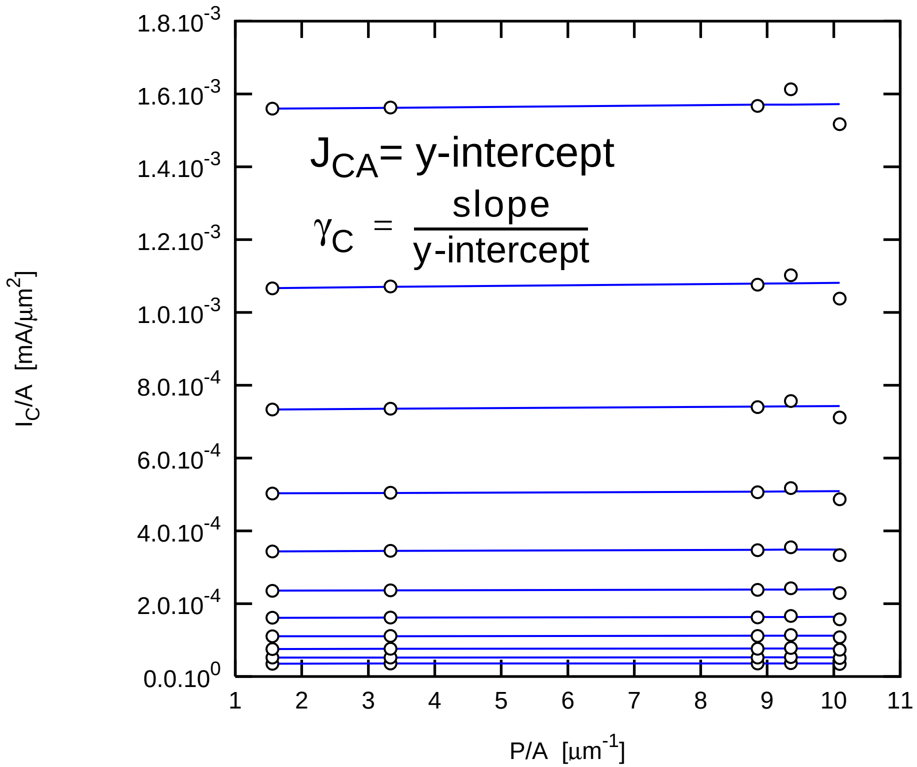


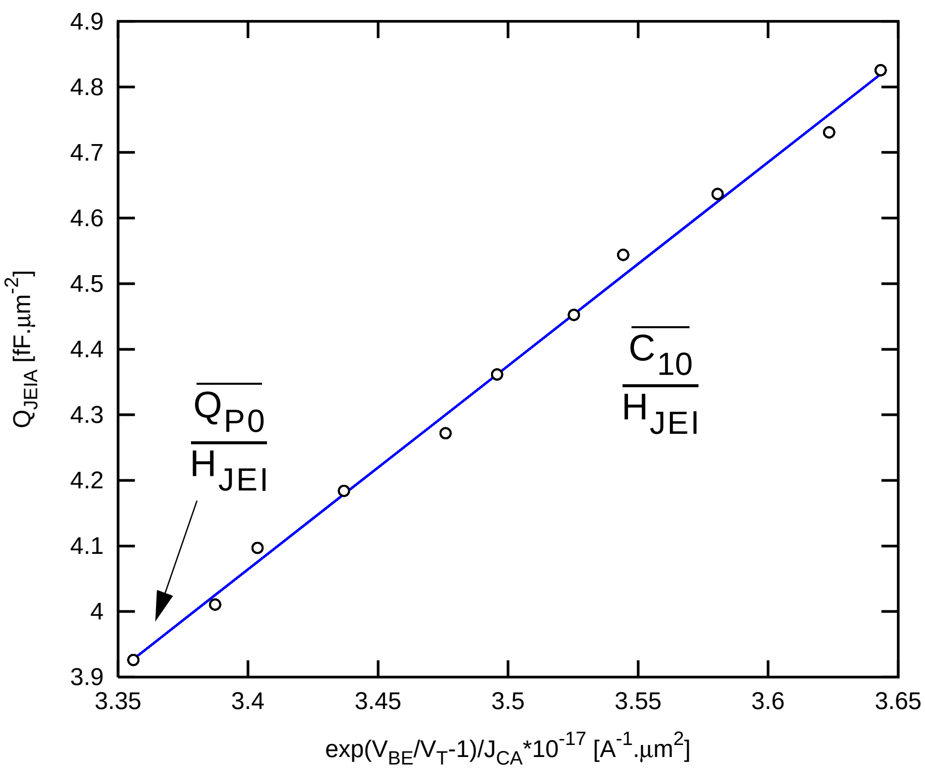
Transfer current parameters γ_C, C_{10}, Q_{P0} (1)

❒ **Definition of the effective emitter area**

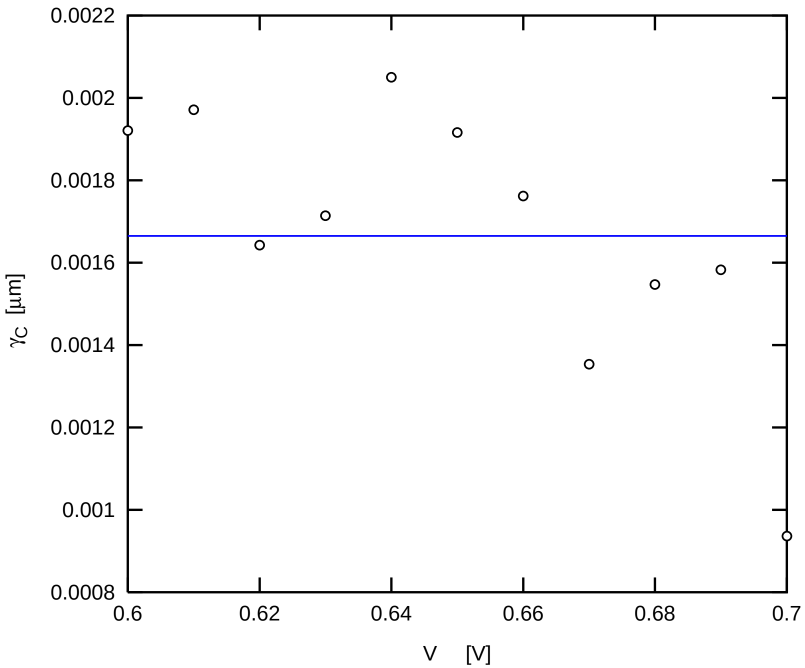
$$I_T = J_{CA} \cdot (W_E + 2\gamma_C) \cdot (L_E + 2\gamma_C) = \underbrace{J_{CA} \cdot A_E}_{\text{Area}} + \underbrace{J_{CA} \cdot \gamma_C \cdot P_E}_{\text{perimeter}} + \underbrace{4 \cdot \gamma_C^2 \cdot J_{CA}}_{\text{corner}}$$

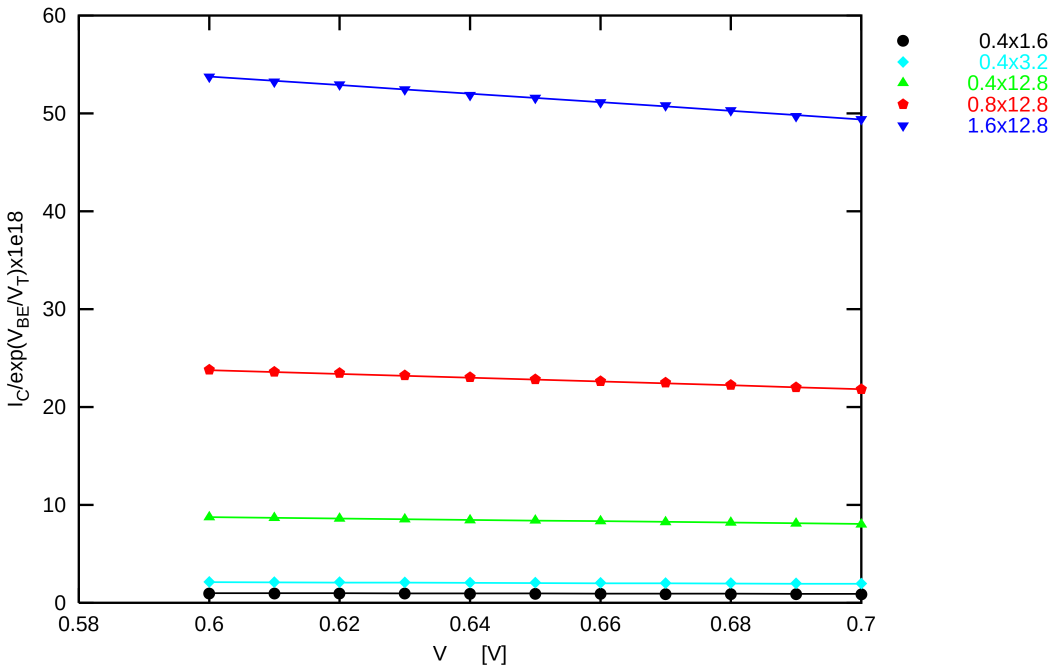
❒ **Extraction of the area extension γ_C (L_E>>W_E, W_E variable)**





Transfer current parameters γ_C, C_{10}, Q_{P0} (2)





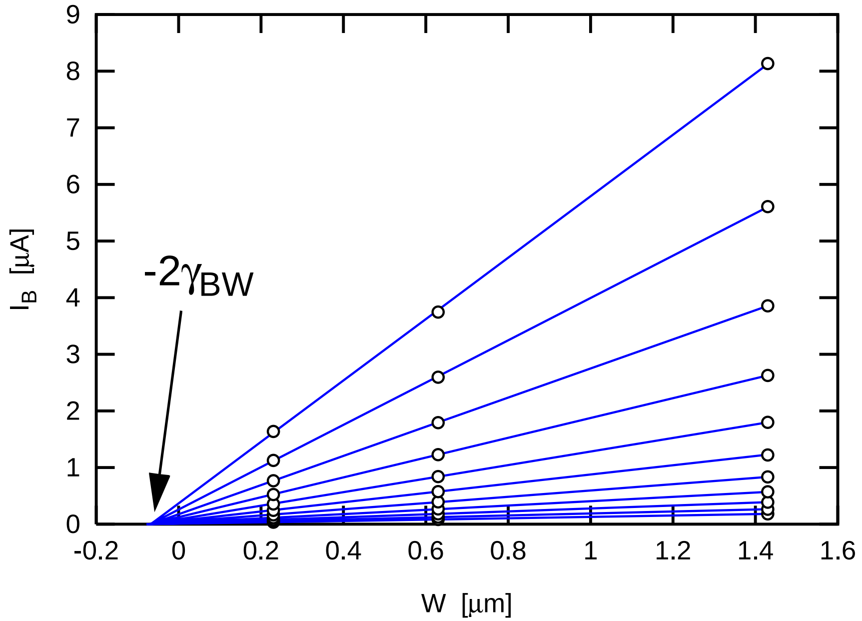
- **Dependence of γ_C with V_{BE} and with the real emitter size -> critical step**
  - Impact strongly the regeneration of model parameters
  - Impact strongly the extraction of specific parameters of the transit time at low current
- $\overline{C_{10}}$ **and** $\overline{Q_{P0}}$ **are extracted from J_{CA} using the same method than for the model parameter C_{10} and Q_{P0} [2]**

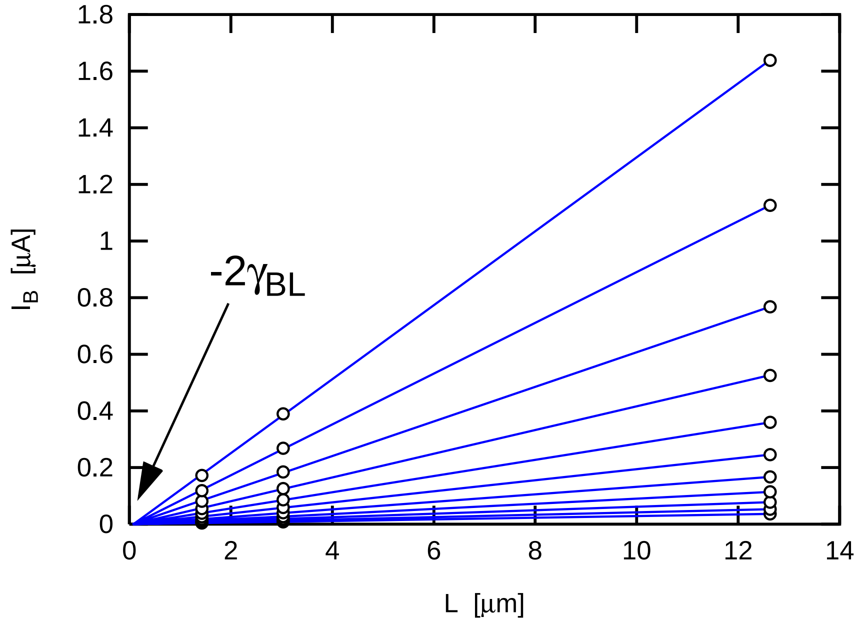
Specific parameters for the base current (1)

❒ **Definition of an effective area for the base current**

$$I_B = J_{BA}\cdot(W_E+2\gamma_{BW})\cdot(L_E+2\gamma_{BL}) = \underbrace{J_{BA}\cdot A_E}_{I_{BEI}} + \underbrace{2.J_{BA}\cdot\gamma_{BW}\cdot L_E + 2\cdot J_{BA}\cdot\gamma_{BL}\cdot W_E + 4\cdot\gamma_{BL}\cdot\gamma_{BW}\cdot J_{BA}}_{I_{BEP}}$$

❒ **Extraction of γ_{BW} and γ_{BL}**

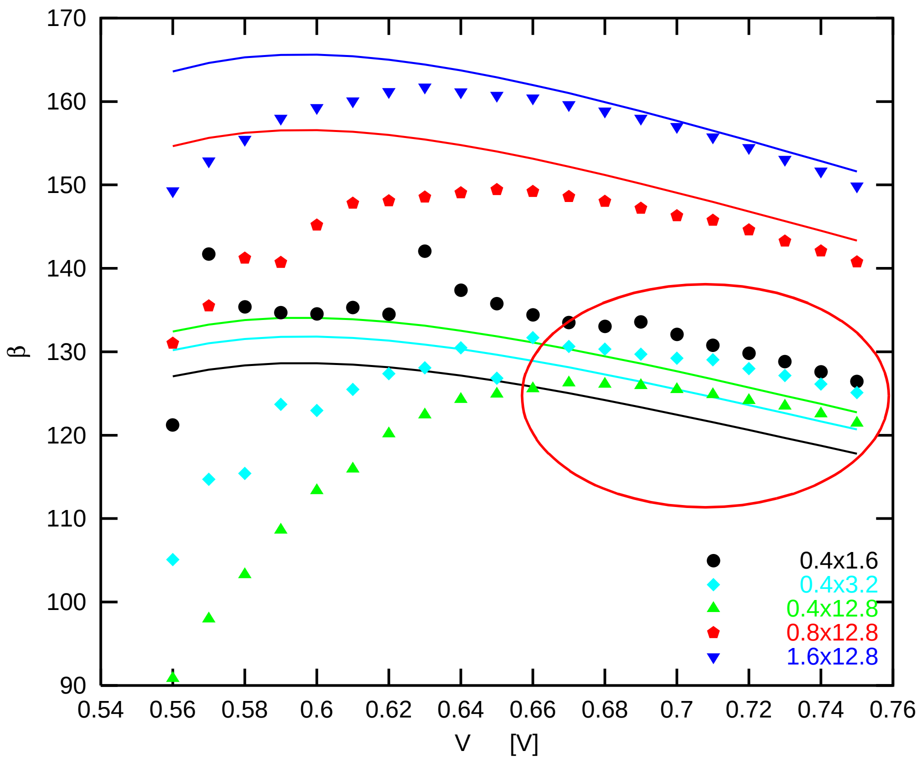




❒ **The base current density J_{BA} is deduced from** $\dfrac{I_B}{(W_E+2\gamma_{BW})\cdot(L_E+2\gamma_{BL})}$ **.**

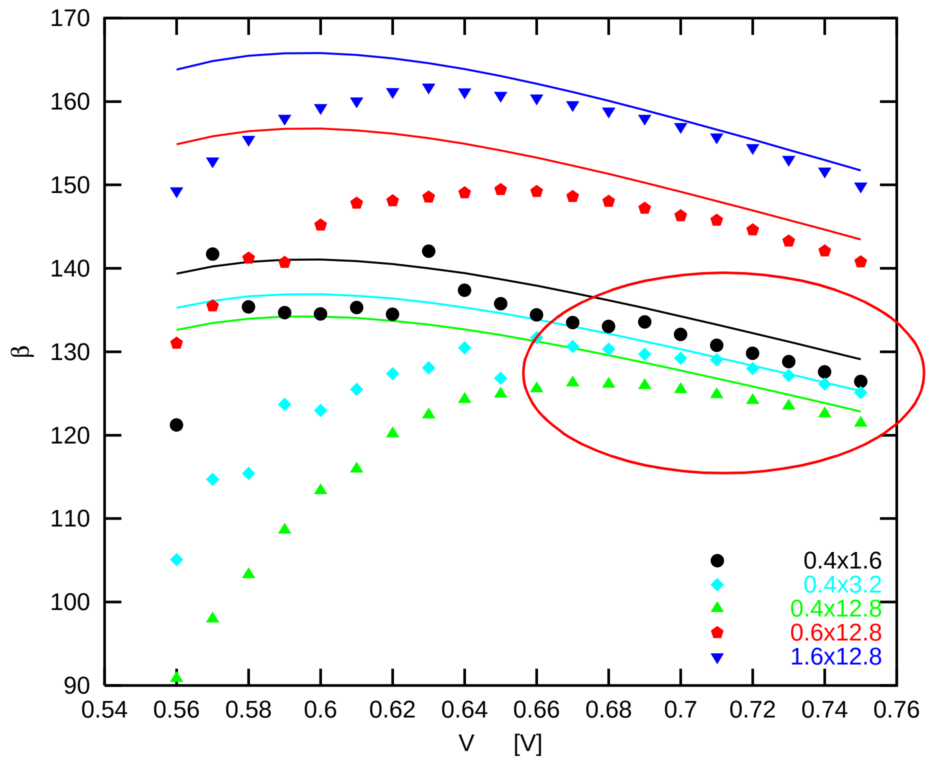
Specific parameters for the base current (2)

- J_{BEIS} and J_{REIS} are extracted on $J_{BA}(V_{BE})$ using the same extraction method than I_{BEIS} and I_{REIS}.
- Two γ_B on emitter length and width are needed



$\gamma_{BL}=\gamma_{BW}$

Wrong variation with L_E

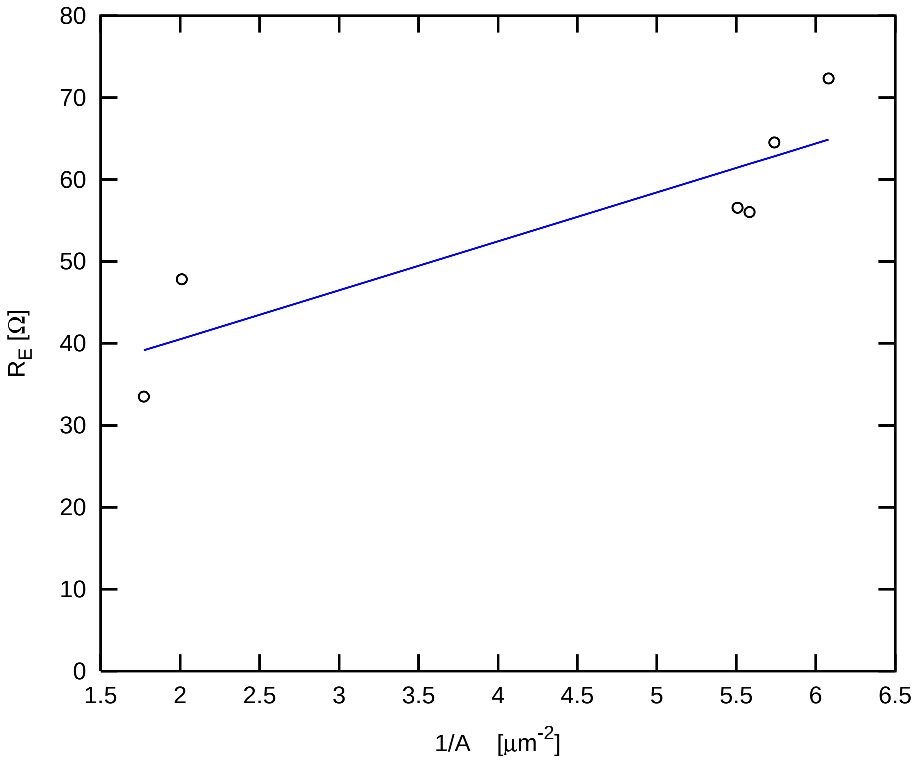


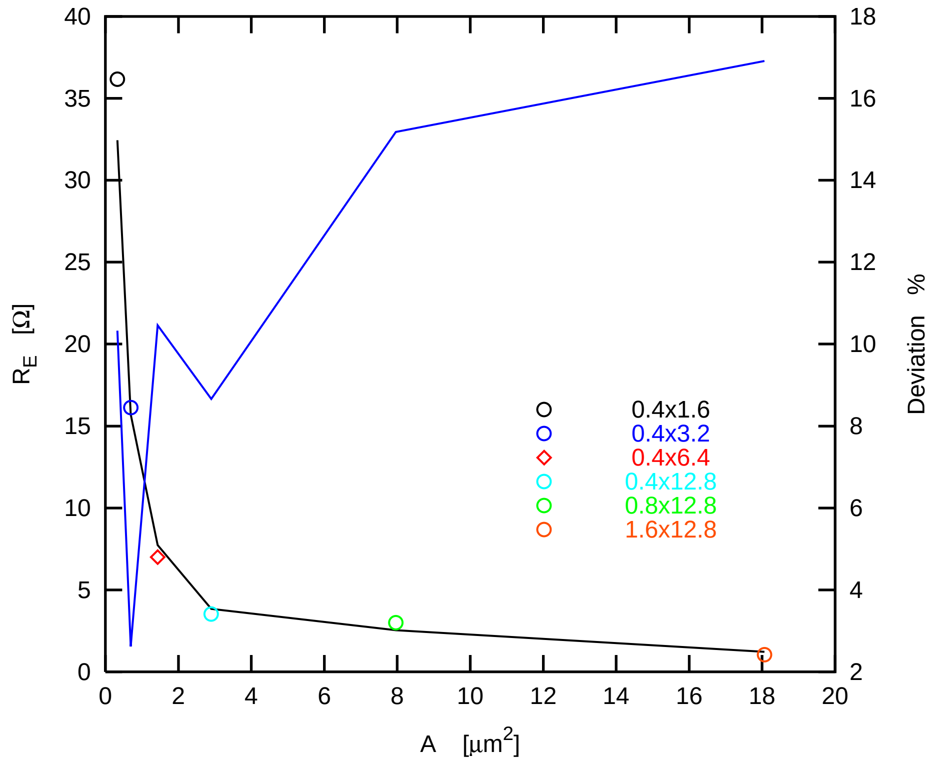
$\gamma_{BL} \neq \gamma_{BW}$

Right variation with L_E

Specific series resistances

- **Emitter resistance**





- **External collector resistance: calculation using layout and sheet resistances determined from specific test structure.**
- **External and internal base resistance: calculation using layout and sheet resistances from specific test structure.**

Transit time at low injection (1)

- **Geometry dependence only for τ_0 following [1]**

$$\tau_0 = \tau_{i0} \cdot \frac{A_E}{A_{Eff}} + \tau_{p0} \cdot \left(1 - \frac{A_E}{A_{Eff}}\right)$$

with A_E real emitter area and A_{Eff} the effective emitter area

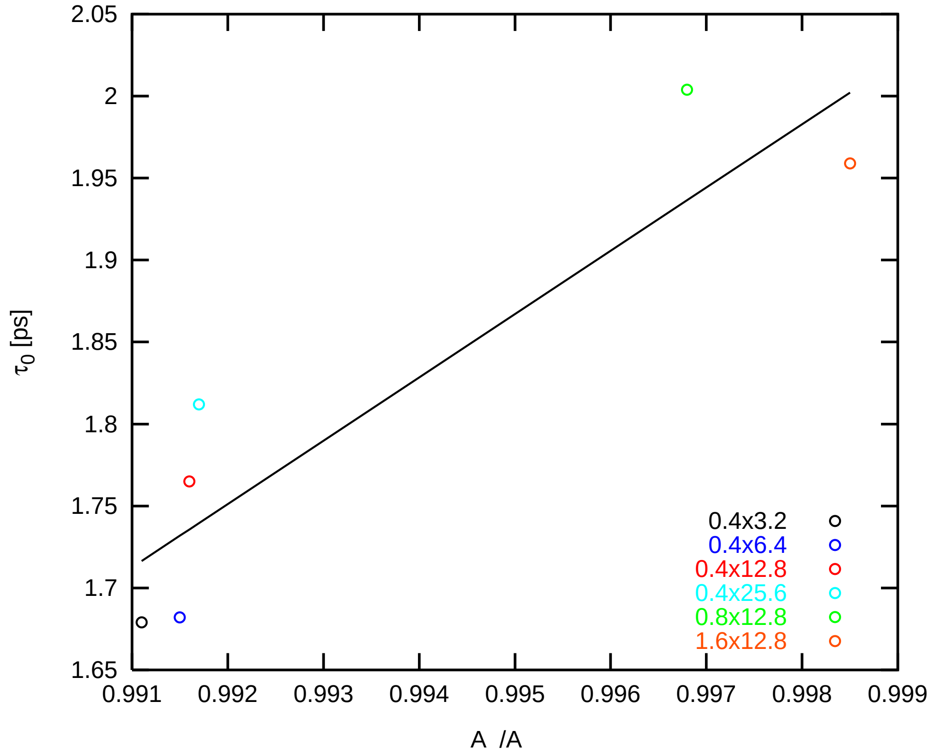
$$\Rightarrow \quad \tau_0 = \tau_{p0} + (\tau_{i0} - \tau_{p0}) \cdot \frac{A_E}{A_{Eff}}$$

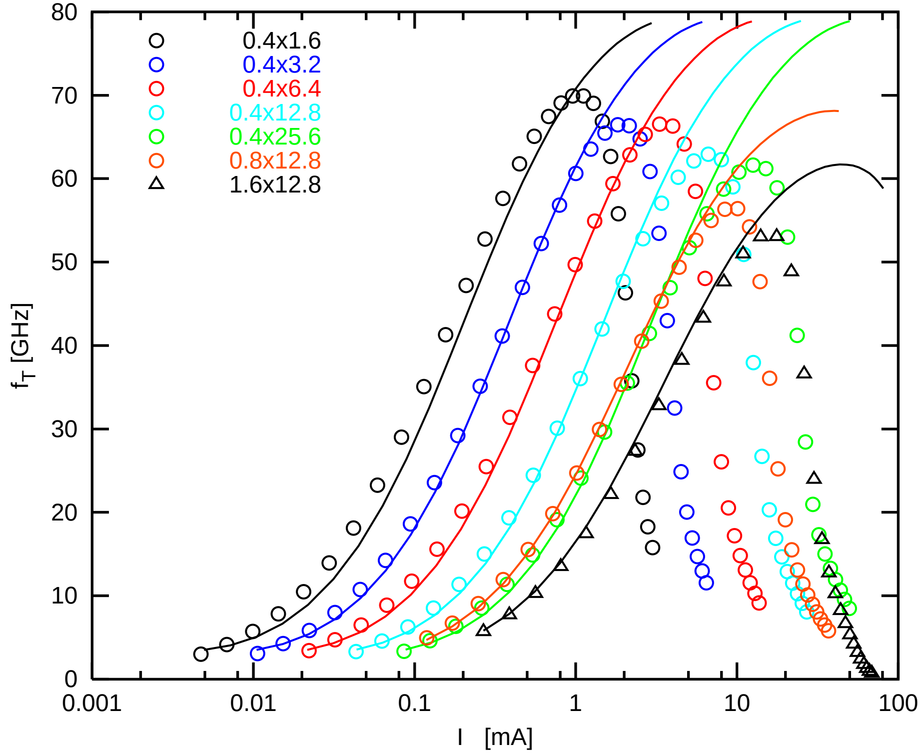
- **For each transistor with different L and W**
  - Generation of the model parameter set using the previous specific parameters
  - Determination of τ_0 using $\frac{1}{2\pi f_T} = f\left(\frac{1}{I_C}\right)$ curve at V_{BC}=0V ⚠ Always a critical step

- **Extraction of τ_{I0} and τ_{P0} using the $\tau_0 = f\left(\frac{A_E}{A_{Eff}}\right)$ curve (linear regression)**

- **Possible simultaneous optimization of τ_{I0}, τ_{P0}, a_{LJEI} and a_{LJEP} on $f_T(V_{BE}, V_{BC}$=0V) characteristics using transistors with different emitter widths and lengths.**

Transit time at mow injection (2)





- γ_C **determination can strongly impact the extraction of** τ_{0l} **and** τ_{0P}

Internal collector resistance and lateral scaling (1)

- The geometry dependence of the high current effects is taken into account through the critical current:

$$I_{CK} = \frac{V_{ceff}}{R_{CI0}} \cdot \frac{1}{\sqrt{1 + \left(\frac{V_{ceff}}{V_{LIM}}\right)^2}} \cdot \left[1 + \frac{x + \sqrt{x^2 + 10^{-3}}}{2}\right]$$

$$R_{CI0} = \frac{R_{KCI0}}{A_{Eff}} \cdot \frac{1}{fcs}$$

R_{KCI0} specific internal collector resistance

f_{cs} collector current spreading factor (lateral scaling)

$$f_{cs} = \begin{cases} 1 + \zeta_b & ,L_{E0} = W_{E0} \\ \dfrac{\zeta_b - \zeta_l}{\ln\left(\dfrac{1 + \zeta_b}{1 + \zeta_l}\right)} & ,L_{E0} \neq W_{E0} \end{cases}$$

with

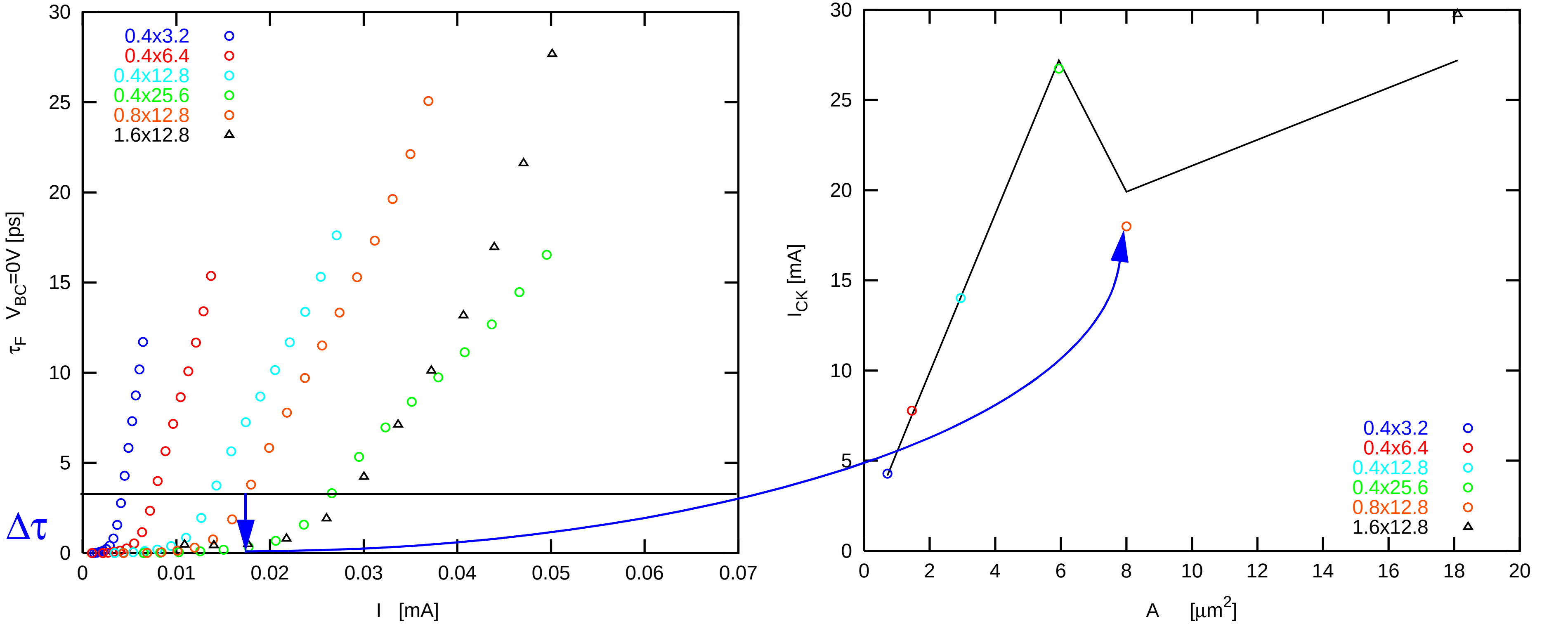
$$\zeta_b = \frac{DELC}{W_E} \qquad \zeta_l = \frac{DELC}{L_E}$$

$$DELC = 2 \cdot W_C \cdot \tan\delta_C$$

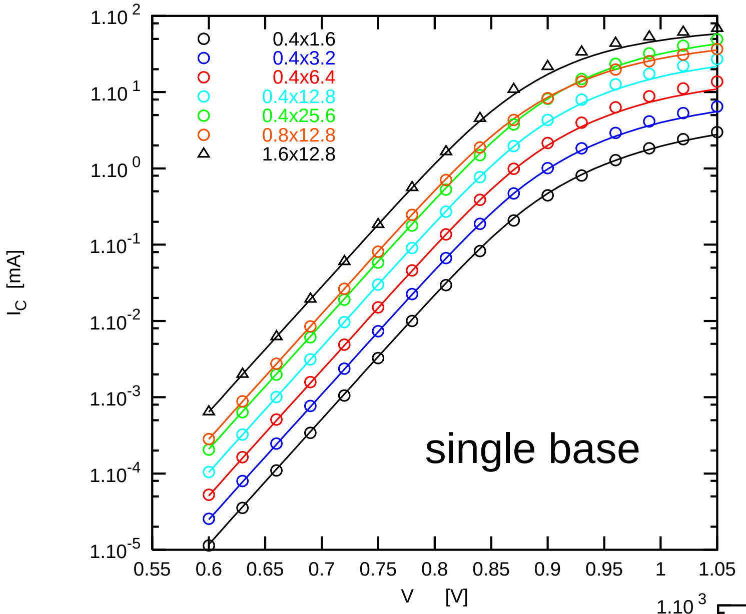
- Two specific parameters have to be extracted R_{KCI0} and DELC.

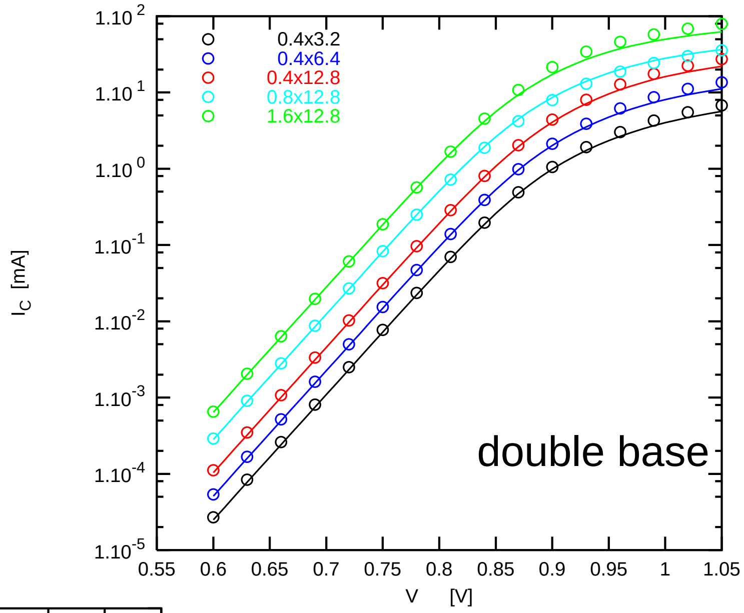
Internal collector resistance and lateral scaling (2)

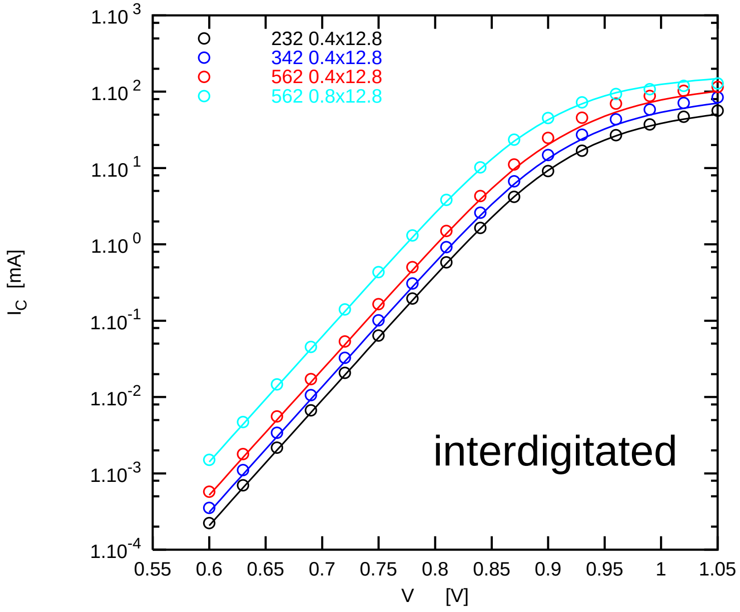
- Extraction of V_{LIM}, V_{CES} and V_{PT} on a single long transistor (L>>W)
- Using the transit time extracted previously for each transistor at V_{BC}=0V, determination of I_{CK} for each transistor.
- Optimization of R_{KCI0} and DELC on $I_{CK}(A_{Eff})$



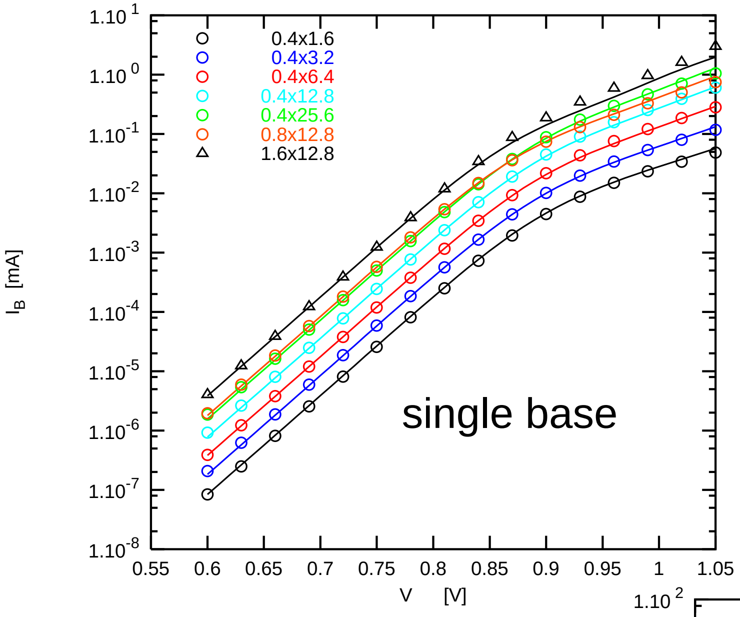
Some Results : collector currents

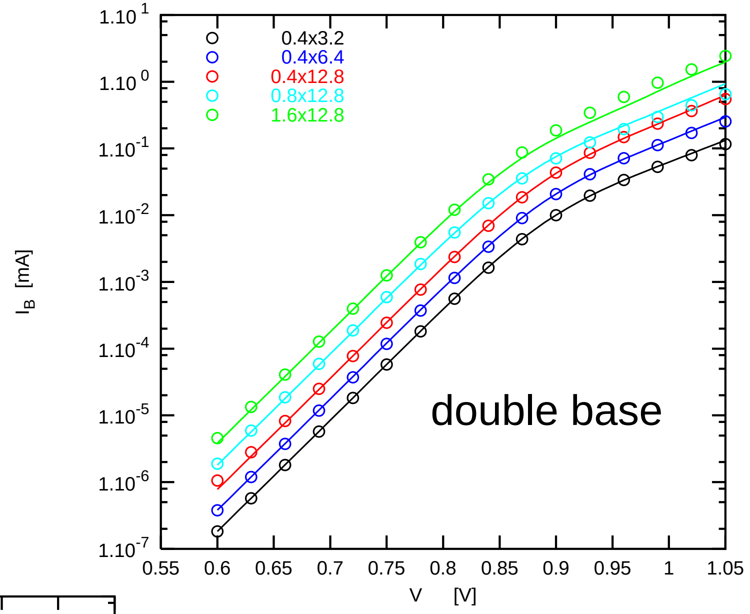


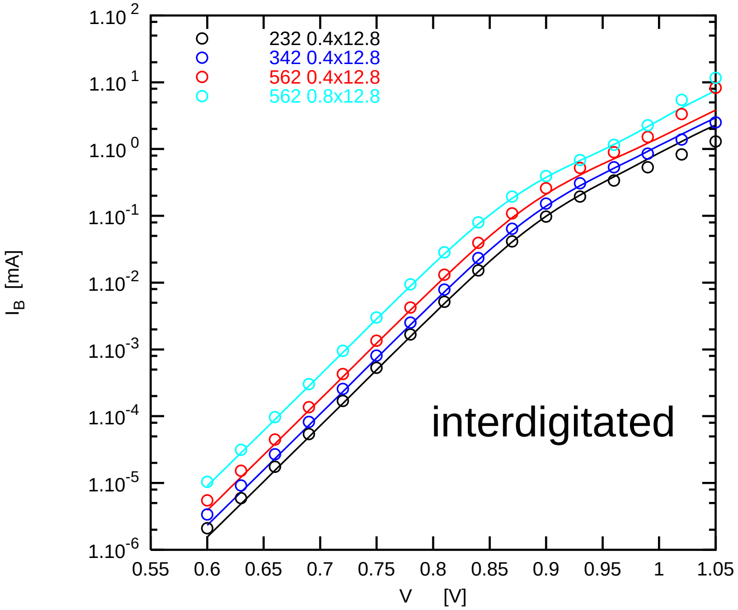




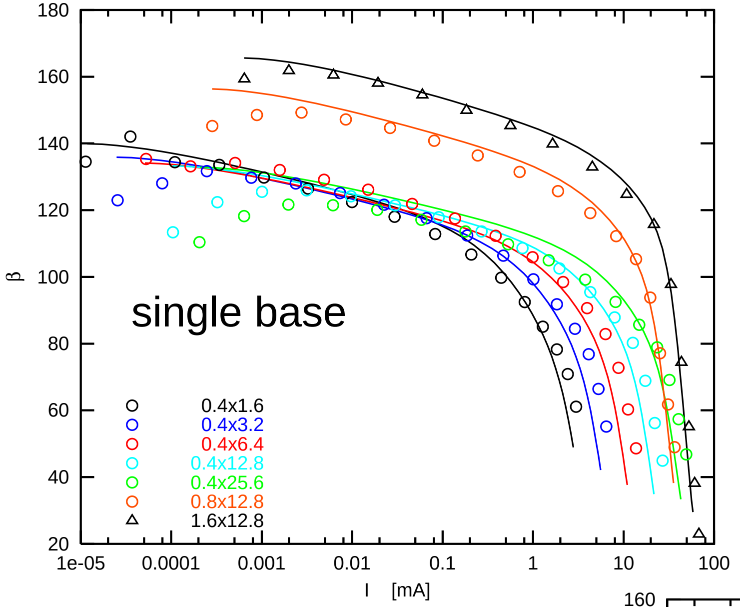
Some results: base currents

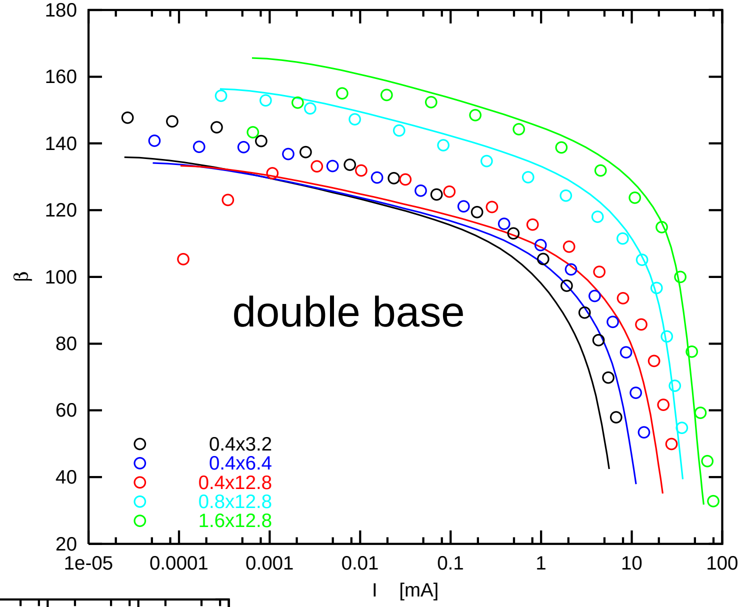


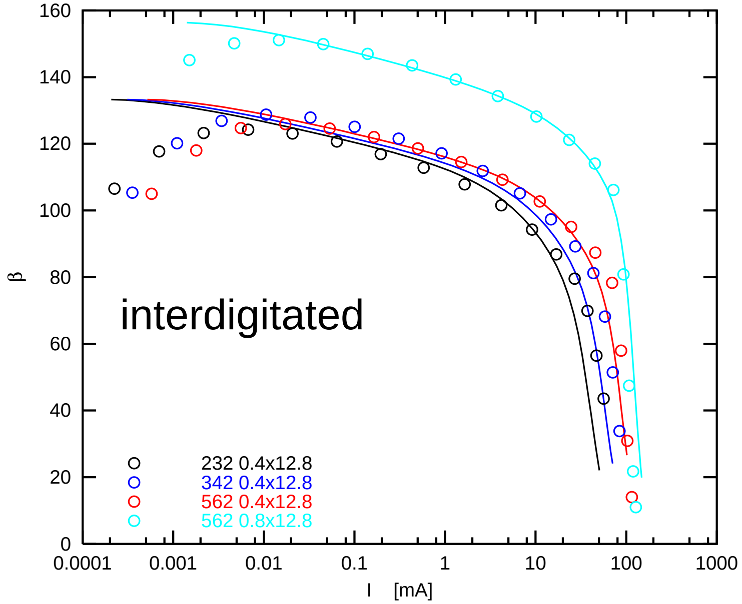




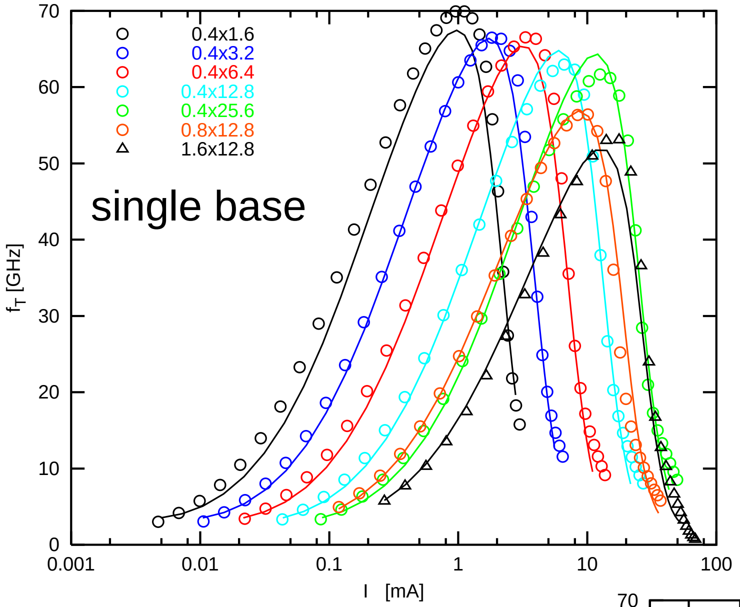
Some results: current gain

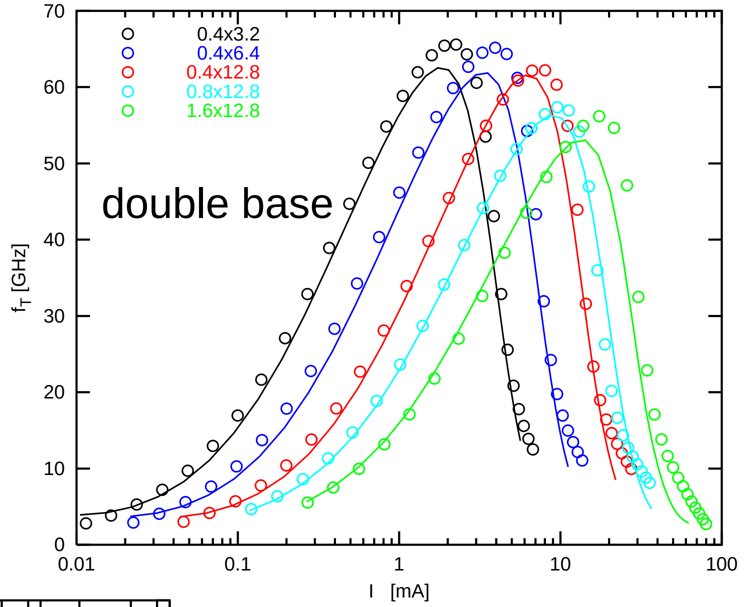


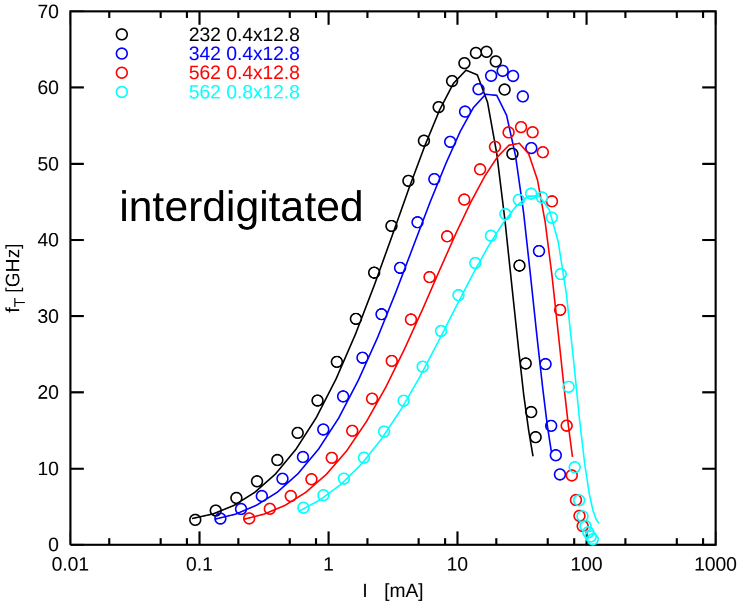




Some results: transit frequency







Summary

- **A scalable extraction methodology was presented allowing the regeneration of any transistor model card using these specific parameters and the appropriate scaling laws (TRADICA or pre-processor for circuit simulators).**

- **Main critical points**
  - The uncertainty of real emitter size make difficult the extraction of some specific parameter.
  - Two γ_B values needed to take into account the β dependence with L_E and W_E. Solutions?.
  - τ_F calculation from f_T is still not easy or not enough accurate.

- **These methods are in development and improvements are certainly possible.**

- **All comments and suggestions are welcome.**

- **References**

[1] M. Schröter, D.J. Walkey, “Physical modeling of lateral scaling in bipolar transistors”, IEEE J. Solid-State Circuits, Vol. 31, pp 1484-1491, 1996 and Vol. 32, pp. 171, 1998.

[2] D. Berger, D. Céli, “HICUM Parameter Extraction Methodology for a Single Transistor Geometry“, pp 116-118, BCTM 2002.