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Foundry Experience with HICUM and TRADICA

- temperature behavior
- model implementation

Improvements in RF measurements

- model validation with independent data
- RF test structures

temperature behavior

issue: bandgap design shows different results with SGPM & HICUM

- reason: OP in high current region
- checked by comparing Vbe vs T with Ic=const. on single BJT
- SGPM & HICUM similar for low current densities
- SGPM shows larger temperature effect on Vbe for high current densities
- additional check on bandgap core transistors done
- under way: measure realized circuit
- the following slides show impact of current density on temperature behavior

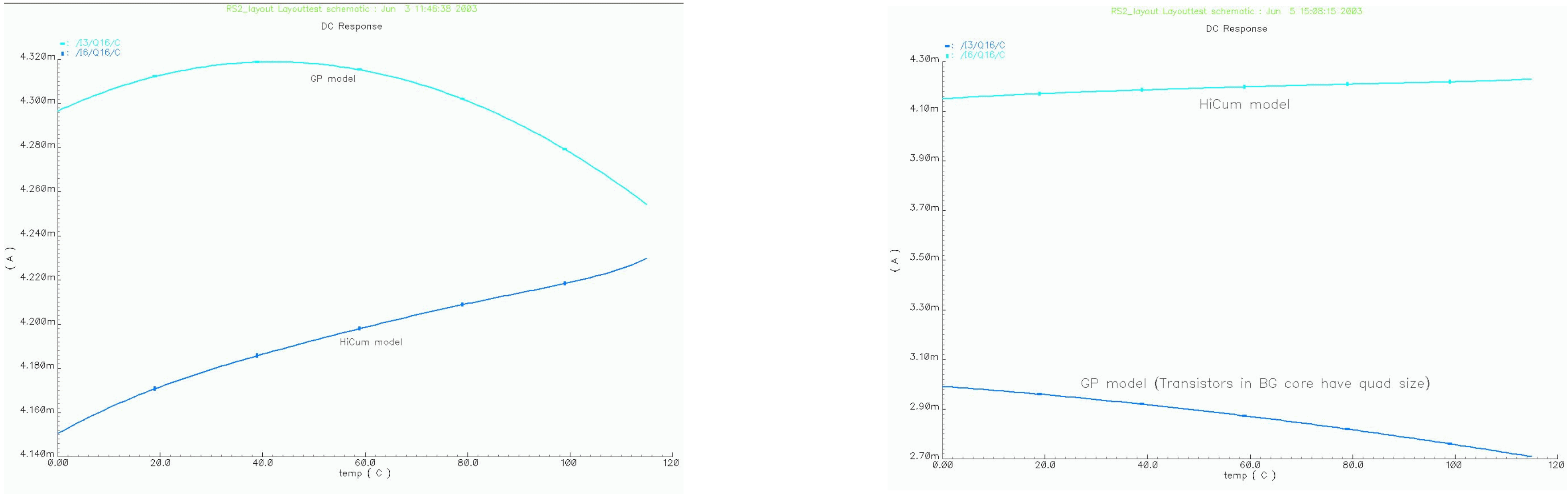

Fig. 1: collector currents of bandgap core BJTs
left : original design with SGPM (top), HICUM (bottom)
right: core BJTs with quad size with HICUM (top), SGPM bottom

Model implementation

Betreff: RE: ATmel HiCUM Models SiGe1 SiGe2

Hi Stephan,

In general we have found that the Hicum models are very good. Our main issue is with using the models in the transient simulator within ADS. The Hicum models in anything other than a very simple circuit fail to converge, and quiet often diverge within parts of a circuit to give erronious results.

It has lead us back to using the GP models for our transient sims. It would be very good if it were possible for you to put some pressure on Agilent as a foundry to help fix this issue. Please feel free to say that it is XXX

that is the customer and that we are very unhappy with the situation.

Hope all is well with you. And we will be releasing that engineering mask run soon!

Cheers

Alan

Improvements in RF measurements

The following 3 slides show the prediction capability of the TRADICA/HICUM approach by:

- **plugging an I(V)-,C(V)- and small signal based model into the simulation setup**
- **extrapolating that model to a different data domain**
- **measurement data are Large Signal S-parameters provided by AGILENT, Belgium**
- **frequency from 900MHz up to 20GHz covered**
- **the model existed before this measurements were available**
- **the model wasn't changed in any way**

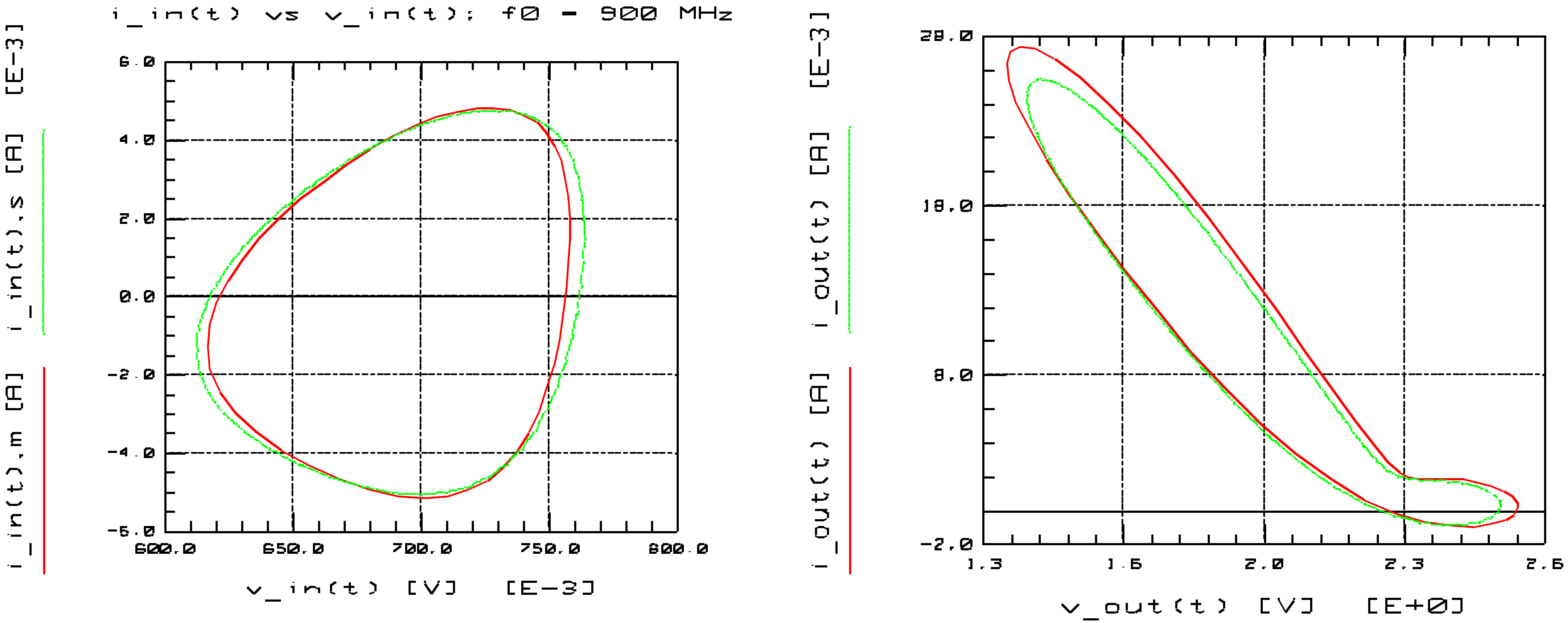

Fig. 2: current vs voltage waveforms, base (left) and collector (right)

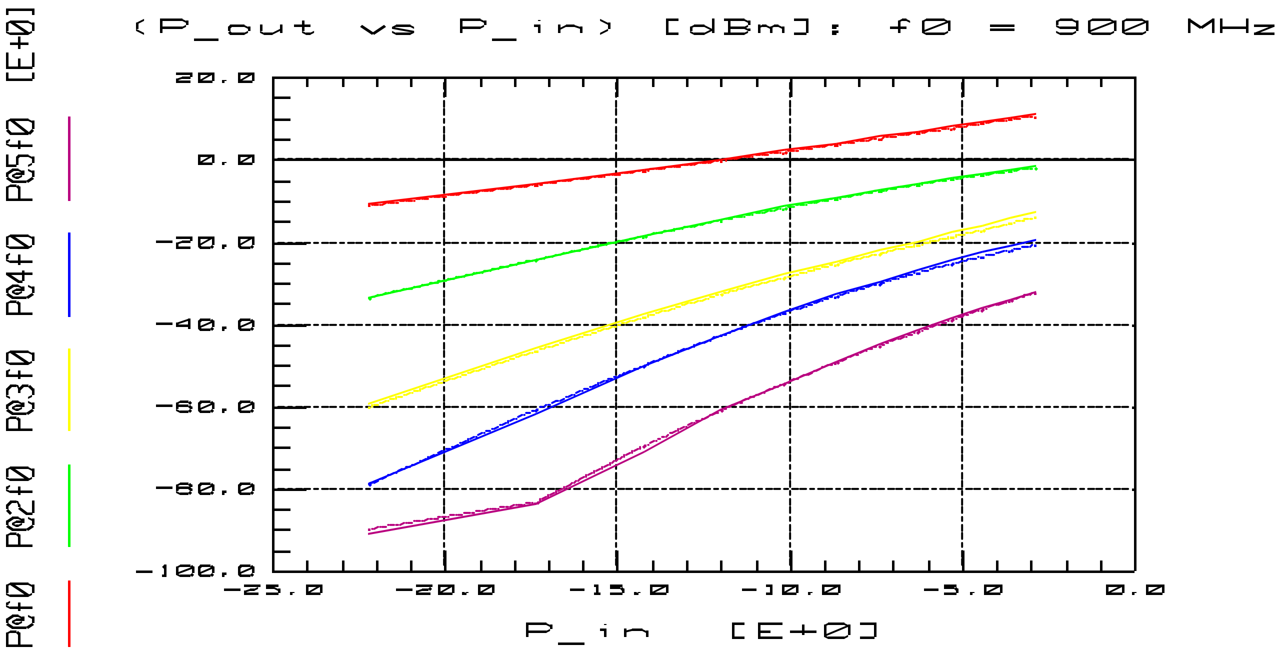

Fig. 4: Pout vs Pin; measurements have been cut for high input power

Improvements in RF measurements

Steps to improvement:

- investigate new deembedding methods, done
- investigate test structures

The following slides show first results of ground-shield test structures.

- under way: evaluation of scaling behavior
- if successfull, large impact on test structure design
  i.e. deembedding structures for every DUT size no longer needed

Shield-Based Microwave On-Wafer Device Measurements

Troels Emil Kolding, *Member, IEEE*

***Abstract*—This paper introduces a shielding technique for use with microwave on-wafer device characterization. This results in a shield-based test fixture, which offers many advantages compared to conventional structures. Among others, the test fixture offers full scalability and very low cost, high measuring accuracy, mitigation of leakage problems associated with lossy substrates, and a large measuring realism. The performance of the shield-based method is demonstrated with measurements on test structures fabricated in low-cost silicon processes.**

***Index Terms*—Analog integrated circuits, calibration, microwave measurements.**

I. INTRODUCTION

THE demand for improved on-wafer measuring and characterization techniques is still evident, although much research effort has been dedicated to this particular subject over the last two decades. A commonly used approach to enhance measuring accuracy is to combine two-port calibration performed with an impedance standard substrate (ISS) with an offline correction or deembedding technique. Several deembedding techniques have been proposed over the years, including open pad correction, three-step deembedding [1], [2], and full two-port correction [3].

Recently, a renewed interest in more accurate on-wafer measuring techniques has emerged due to the application of low-cost silicon processes at radio and microwave frequencies. Low substrate resistivity and characteristics of aluminum metallization are of primary concern when conducting microwave device measurements directly on the die or wafer [4], [5]. Furthermore, a characteristic of low-cost processing is that devices usually display low performance per area, e.g., for inductors, capacitors, and MOSFETs. This implies that the used test fixture must fit very large devices, often on the order of 50–400 μm. With large devices and test-fixture gaps, the parasitics of available in-fixture standards become very significant. Consequently, traditional deembedding approaches often lead to large systematic offsets and overestimation [6]–[8]. To accommodate this effect, several new techniques have recently been adopted including on-wafer *in situ* calibration [9] and compensated deembedding [7], [10]. With standard test fixtures, these techniques show promising results when applied to silicon technologies. However, fundamentally speaking, a higher performance gain can be achieved by mitigating imperfections rather than employing post correction.

In this paper, a shield-based test fixture is proposed that alleviates many of the concerns associated with low-resistivity substrates. The technique was first introduced in [11] and later expanded upon in [12]. In this paper, the features of the shield-based test fixture are detailed and several measuring results are presented, showing good agreement with theoretical and practical predictions. The technique offers: 1) full scalability and very low cost; 2) high measuring accuracy; 3) mitigation of leakage problems associated with lossy substrates; and 4) a large measuring realism.

II. SHIELD-BASED TEST FIXTURE

The basic design goal of the test fixture is to prevent the signal pads from coupling to the substrate. As shall be seen, such measures result in several important advantages. For circuit designs, RF improved pads have previously been suggested that employ variations of shielding techniques [13], [14]. However, the test fixture presented here is optimized for on-wafer measuring performance and further extended to multiport measurements. The isolation of the test-fixture signal pad is achieved by extending a grounded shield below the signal pad, as illustrated in Fig. 1(a). The shield is connected to the ground pads to ensure an accurate on-wafer reference. Although the illustration is made for a ground–signal–ground (GSG) probe, the method is compatible with other types of probes, e.g., ground–signal (GS) and ground–signal–ground–signal–ground (GSGSG), as well.

Note that the shield-based structure is not directly compatible with processes where layout rules dictate that all metal layers be employed in the pad layout. However, since: 1) such rules are associated with large-scale yield and 2) the structure is fundamentally compatible with basic silicon processing, most foundries are willing to fabricate the shield-based fixtures. In fact, RF designers commonly break layout rules in order to achieve adequate microwave pad performance. However, a possible concern is that the absence of metal layers in the center pad may lead to a height difference between ground and signal pads. Common pad design rules for on-wafer probing imply that the height difference between pads should not exceed 0.5 μm [15]. As of this writing, no problems have been observed in practice, although up to five metal layers have been excluded from the signal pad. Further, the required amount of skate is usually on the order of 50–60 μm for aluminum-based pads [5], which, in practice, effectively mitigates the problem. As to facilitate good contact reliability, at least two top metal layers should be incorporated in the signal pad structure. Further, alignment marks should be placed on the die in order to facilitate consistent skate.

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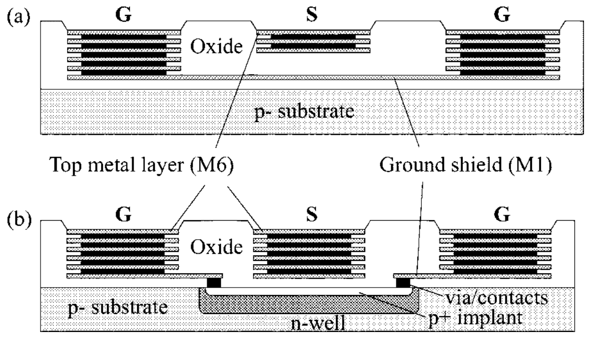


Fig. 1. (a) High-performance and (b) layout rule-compliant shield-based contact pads.

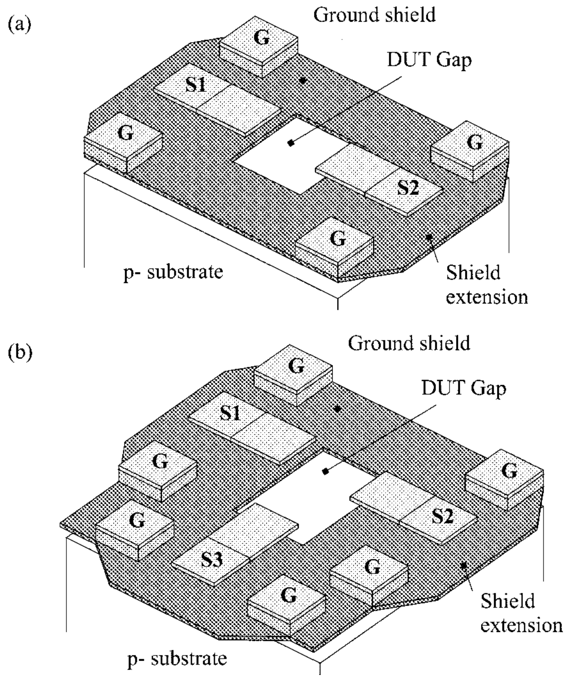


Fig. 2. Shield-based GSG test fixtures minded for: (a) two- and (b) three-port DUT measurements.

For processes where the suggested bending of layout rules cannot be accepted, it is possible to fabricate a compliant structure, as shown in Fig. 1(b). The structure uses a p+ implant under the signal pad, which is connected to the ground pads. With this approach, all metal layers are used in the signal pad layout. An n-well should be used to isolate the grounded area as much as possible from the device-under-test (DUT). Note that the performance of this pad design is much less than for the similar structure in Fig. 1(a). First, the parallel input capacitance is larger and, second, the p+ implant introduces higher resistive loss, which reduces the quality factor of the parallel input characteristic. However, compared to conventional pad structures, a performance gain is still available.

In Fig. 2(a) and (b), the shield-based structure is extended to two- and three-port measurements. An important consideration is to ensure a low-loss common ground among all ports. Besides fulfilling a basic requirement for all multiport measurements, this also facilitates an accurate ground connection for the DUT and the underlying substrate. In order to terminate fringing fields, a shield extension of approximately 2–3 times the pad height should be used in conjunction with all signal pads. For processes where low-resistivity tungsten is used as the bottom metallization layer, it is advisable to include a second metal layer for lowering the loss of the ground shield. An exception is the area directly below signal leads where a reduced vertical distance would result in an undesired increase in parallel coupling. Further, a smooth transition between pads and input leads is desirable. Input leads should only be drawn in one or two of the top metal layers in order to reduce the susceptibility toward oxide variations.

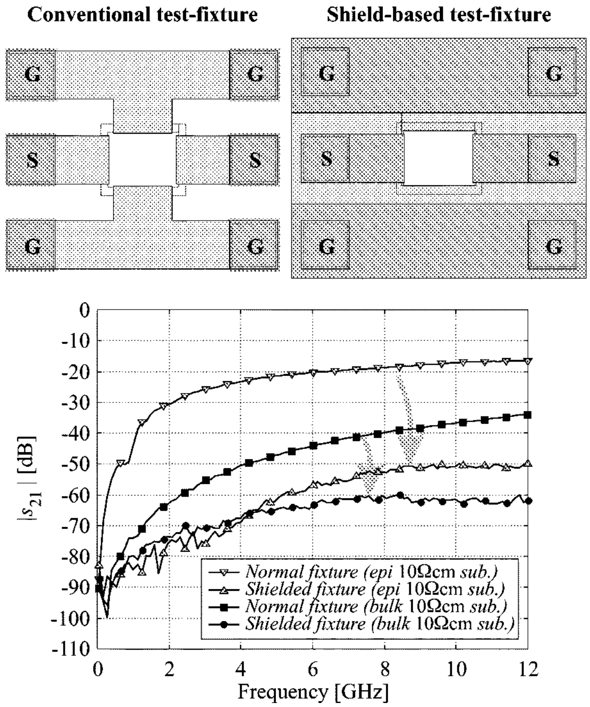
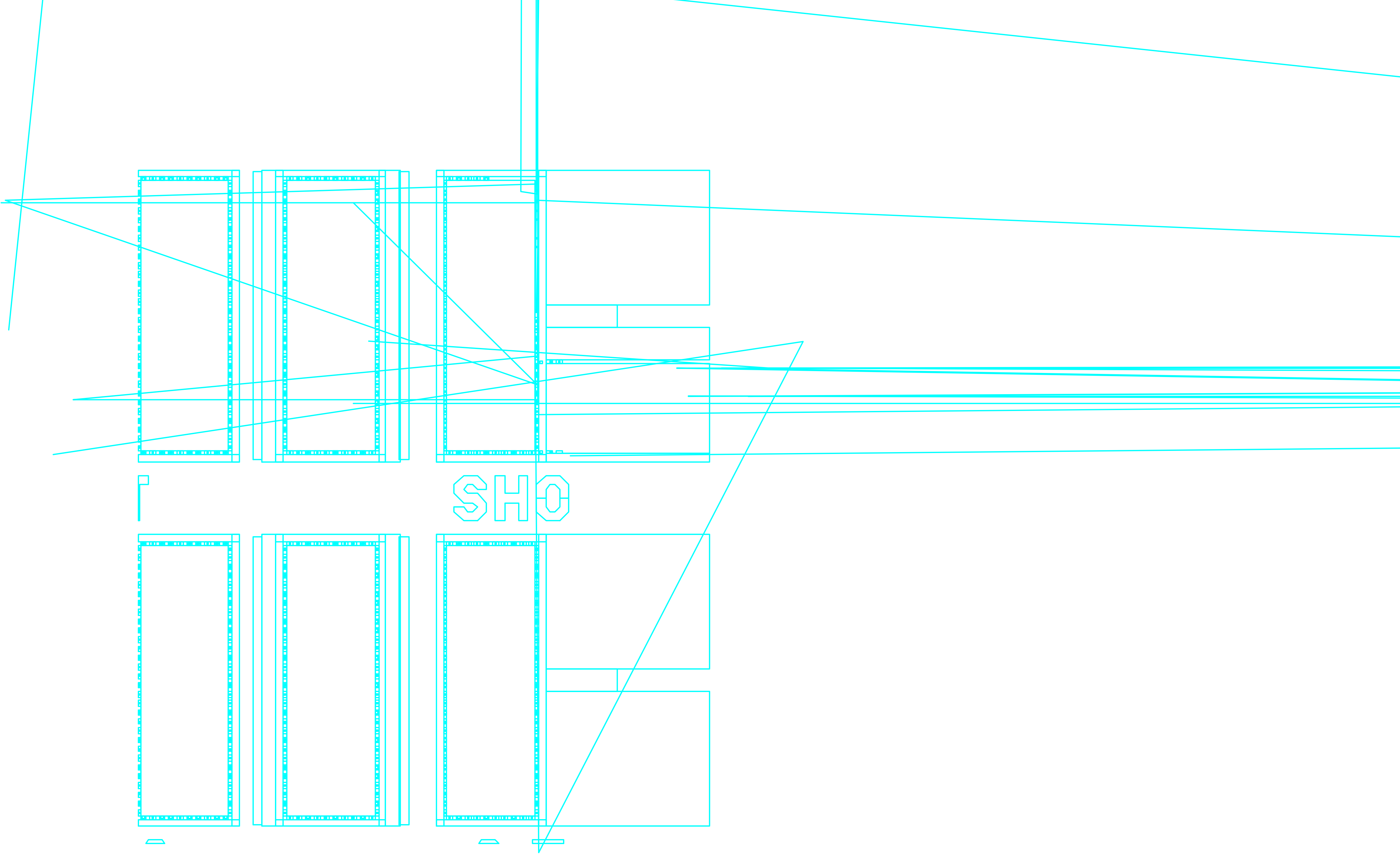


Fig. 3. Reduction in forward coupling by adding ground shield.

III. FEATURES OF SHIELD-BASED TEST FIXTURE

To demonstrate the capability of the shield-based test fixture, several experiments have been conducted. The most important obstacle to achieving scalable low-cost measurements is the forward coupling of conventional test fixtures. As has been previously demonstrated, this coupling is due to the low resistivity of the silicon substrate and not direct fringing [16], [5]. Hence, the forward coupling is effectively reduced by isolating the signal path from the substrate and making all input ports refer to an accurate common ground. This is effectively demonstrated in Fig. 3, where conventional test fixtures are compared to shield-based test fixtures for two different low-resistivity silicon processes. The bulk process uses dummy patterns and shallow-trench isolation to achieve a fair performance even without the ground shield. However, for many device measurements, a coupling level around −30 dB cannot be neglected and the introduction of the ground shield gives a desirable performance improvement. For the epitaxial process, the coupling is inferior and may even dominate the intrinsic coupling of many devices. Although the improvement of applying shielding is most evident for highly doped substrates, a visible forward coupling reduction is also possible for other common silicon processes.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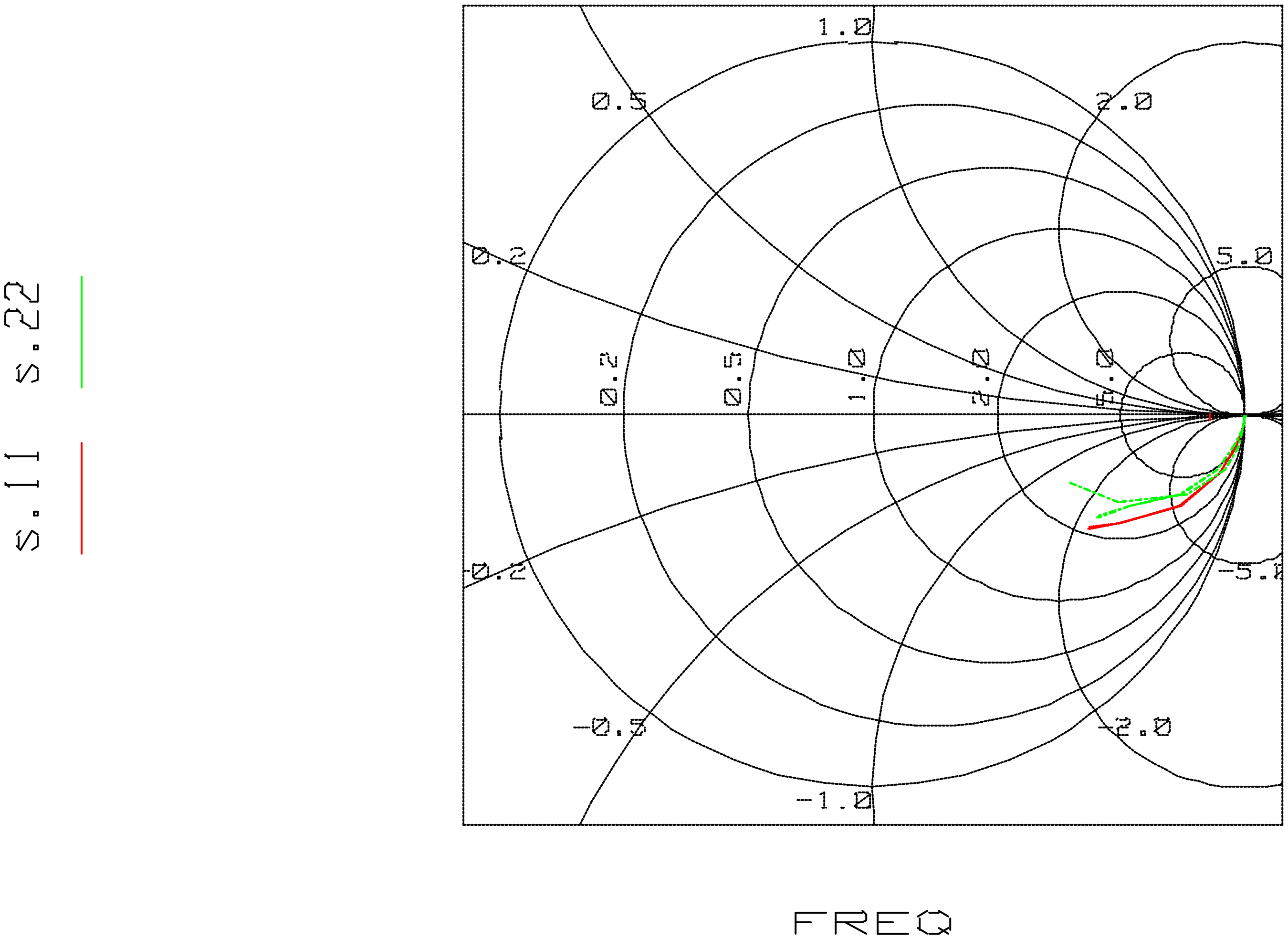
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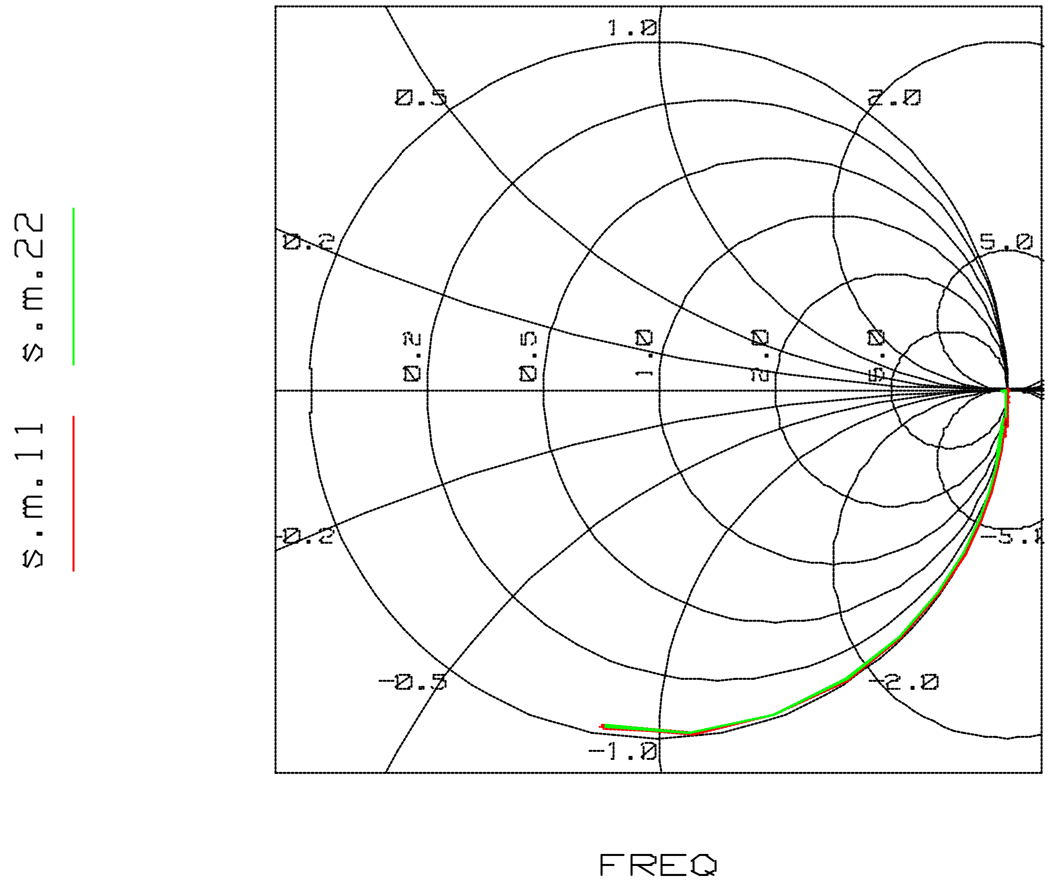

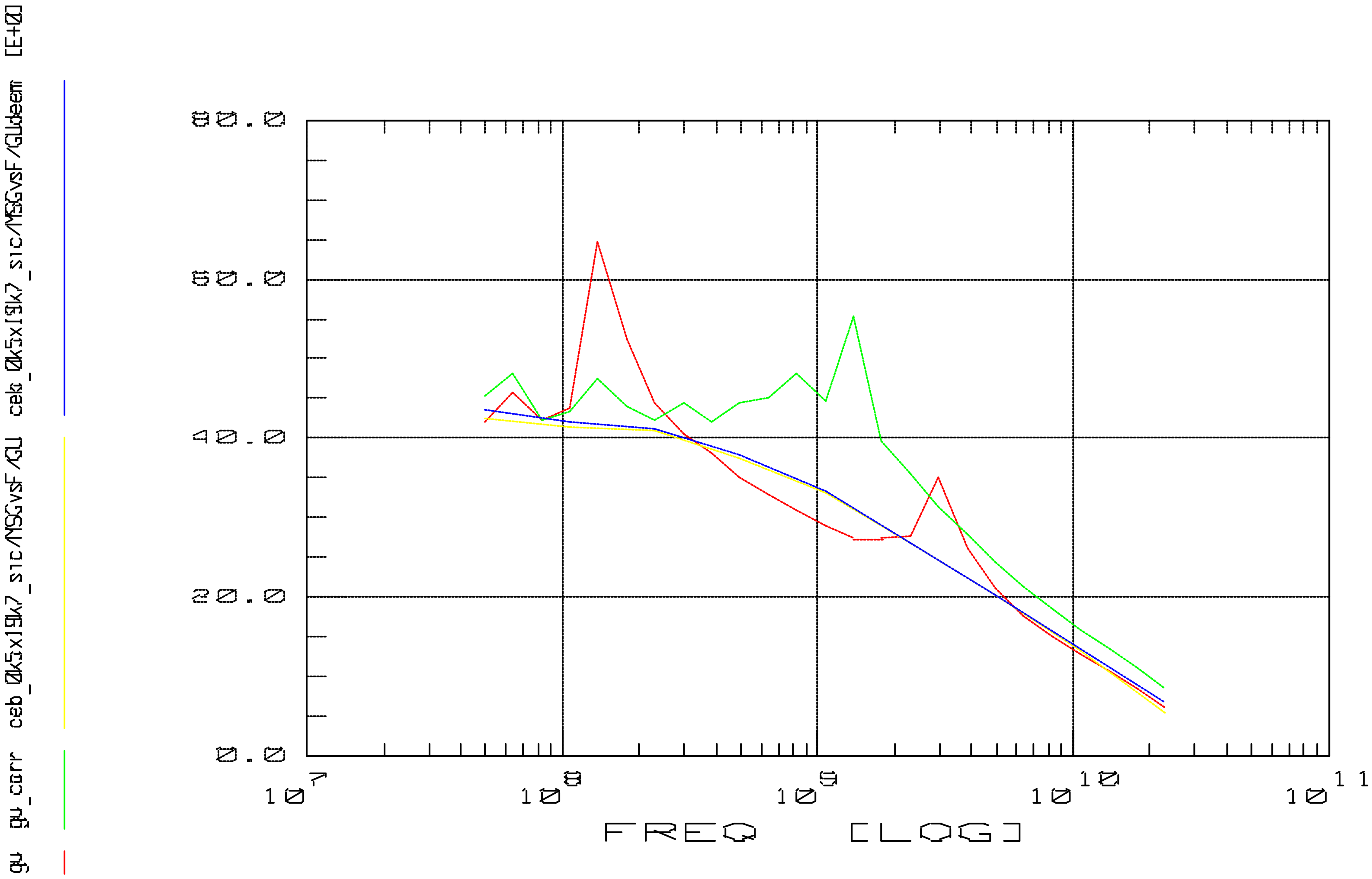
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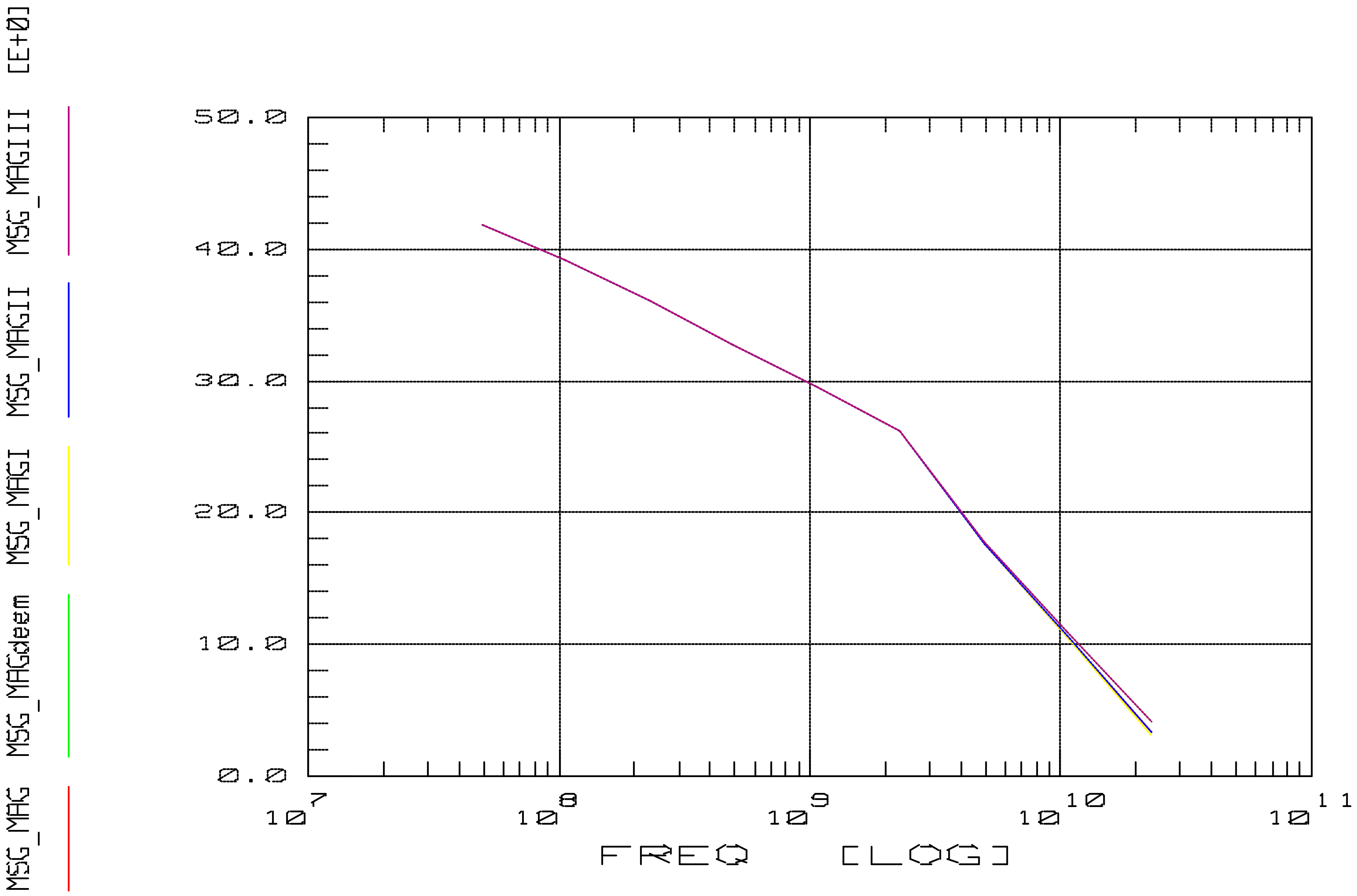
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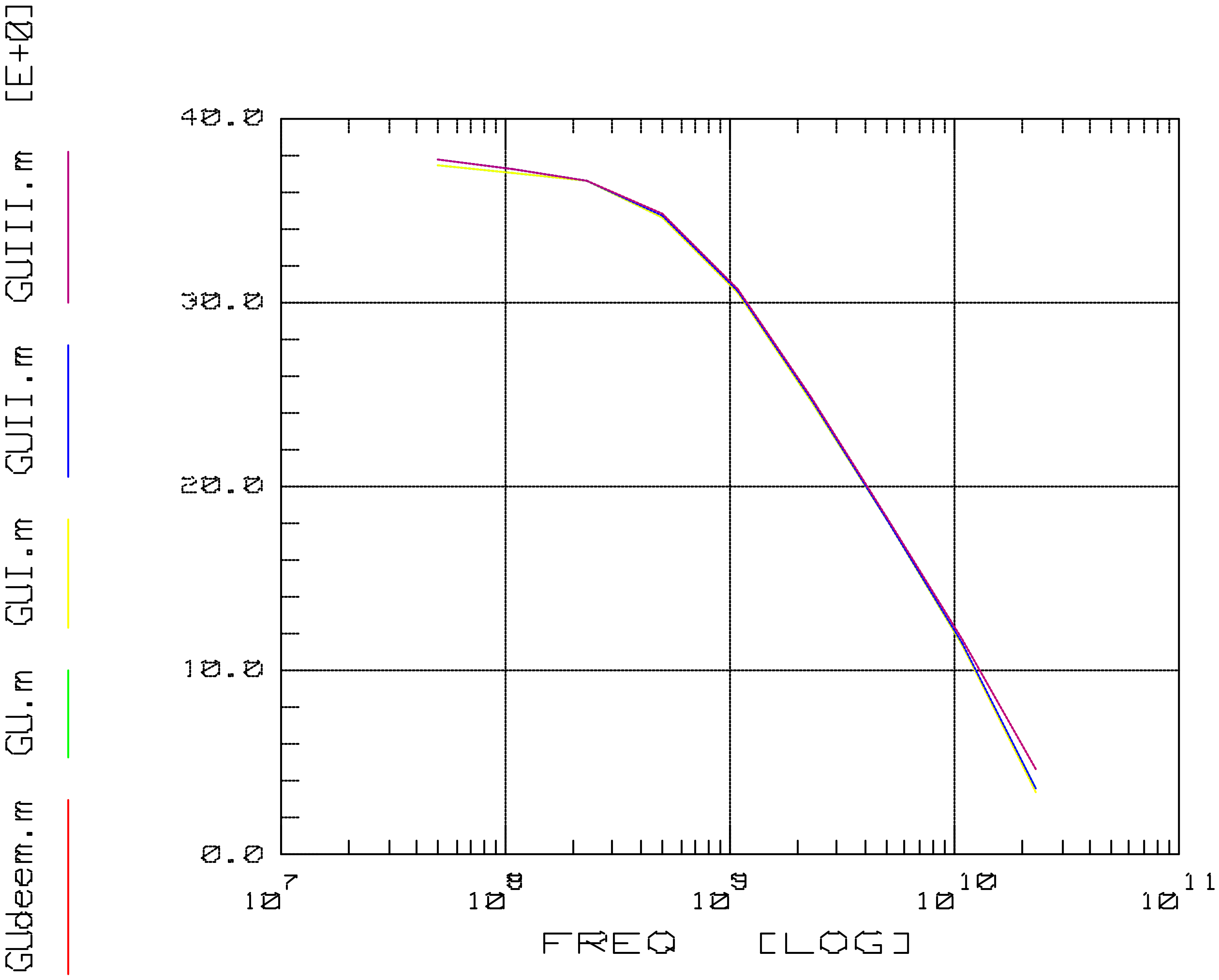
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