

3^d European HICUM Workshop

June 16/17, 2003

Dresden, Germany

Chair for Electron Devices and Integrated Circuits (CEDIC)

University of Technology Dresden / GWT, Germany

http://www.iee.et.tu-dresden.de/iee/eb/eb_homee.html

Workshop location: GWT, Chemnitzer Str. 48b, 01187 Dresden

About this workshop ...

- a forum for "free" discussion and exchange of information
 - between users and developers
 - model enhancement recommendations
 - model implementation and availability
 - industry meets students
- discussion of HICUM (and bipolar transistor modeling) related questions
 - overview on model development (physical background, limitations...)
 - model support issues
- model parameter extraction: issues and clarification
 - methods, methodologies (e.g. is a common model parameter extraction procedure desirable ?)
 - test structures (e.g. is a common set of test structures desirable ?)
 - presentation of available results and solutions by users and developers
 - measurement issues, equipment requirements and options
- expectation from and role of model developer at a university ...
- this workshop vs. political meeting (CMC)
- location for European WS: alternation between Dresden and Bordeaux ?

Status of HICUM

Overview

- HICUM/Level2: migration to version 2.2
- simulator implementation and support (issues)
- documentation (new features & corrections)
- related activities (in conjunction with TRADICA)

HICUM version 2.2 - List of major improvements

- already available in some simulators (although version 2.1)
 - parameter MCF
 - separate thermal node for thermal coupling (recommendation to EDA companies)
- physics-based extensions
 - add parameter ACT in IT temperature equation: $(T/T_0)^{ACT}$ rather than $(T/T_0)^3$ in IS and C10
 - replace VD(T) smoothing towards high T by physics-based smoothing
 - parameter for splitting CEOX between external and perimeter base node
 - recommendation to EDA companies:
 - include correlated noise (IB - IC) - for III/V HBTs
 - flags for turning on/off: self-heating, vertical NQS effects, lateral NQS effects (C_{rBi})
- numerical/implementation
 - output conductance: replace numerical derivative by analytical derivative
 - bug fixes in series expansion of current spreading function at (very) small LATL, LATB
 - bug fixes (substrate transistor equations, limiting numbers, hyperbolic smoothing, ...)
 - drop CJCI (QJCI) in AC (DC,TR) lateral current crowding equation for rBi*
- manual
 - improvements, documentation of new features of v2.2

HICUM version 2.2 (cont'd)

optional improvements - decision based on user feedback and demand

- physics-based extensions
 - base current:
 - extension to model increase at high forward bias (due to collector barrier effect)
 - separate T dependence for E recombination velocity (or poly) component or nonlinear current gain vs. T ?
 - use nonlinear T dependent bandgap $EG(T)$
 - also as HICUM parameters ? (to guarantee same results across simulators)
 - split CJS into bottom and perimeter portion in equivalent circuit
 - T dependence of HJEL, HJCI, HFE, HFC
 - parameter for splitting IBETS between external and perimeter base node
- numerical/implementation
 - improve s.h. derivatives (problem: this is handled differently in simulators; also, model compilers will take care of derivatives in future)
 - avoid $I_{TF} = 1E-30$ (and possible overflow) in ICCR code
 - simplify QJC and CJC formulation at punch-through (e.g. linearize CJCI @ high forward bias)
- user suggestions (update):
 - temperature dependence of RTH (via thermal conductivity)
 - normalization of QP to $Qp0$

FAQs

- how is the Early-effect being modeled in HICUM ? $V_{Af} = I_{Tf} \left(\frac{dI_{Tf}}{dV_{CB}} \Big|_{V_{BE}} \right)^{-1} \approx \frac{Q_p}{h_{jci} C_{jCi}} @ \text{low } J_C$
- where is the bias dependent internal collector resistance ?
 r_{Ci} is included in the minority charge formulation = impact on
 - DC characteristics via GICCR
 - dynamic behavior via the transit time (as time constant)
- self-heating:
 - cause for divergence for (strong) s.h. ? s.h. is a positive feedback mechanism => inherently unstable => stability depends on implementation and circuit measures (e.g., ballast resistance)
 - there should be no impact on f_T due to the large thermal time constant (make sure to have $R_{TH} C_{TH} \gg \tau_{elec}$)
- a kink in IC-VCE ... is associated with
 - the minority charge formulation at **hard** saturation (can be eliminated if desired, but costs effort for developing a physics-based formulation, its implementation and test); possible workarounds: (i) use larger VDCI parameter, (ii) linearized CJCI(VBC) at high forward bias (code change along with version 2.2)

FAQs (cont'd)

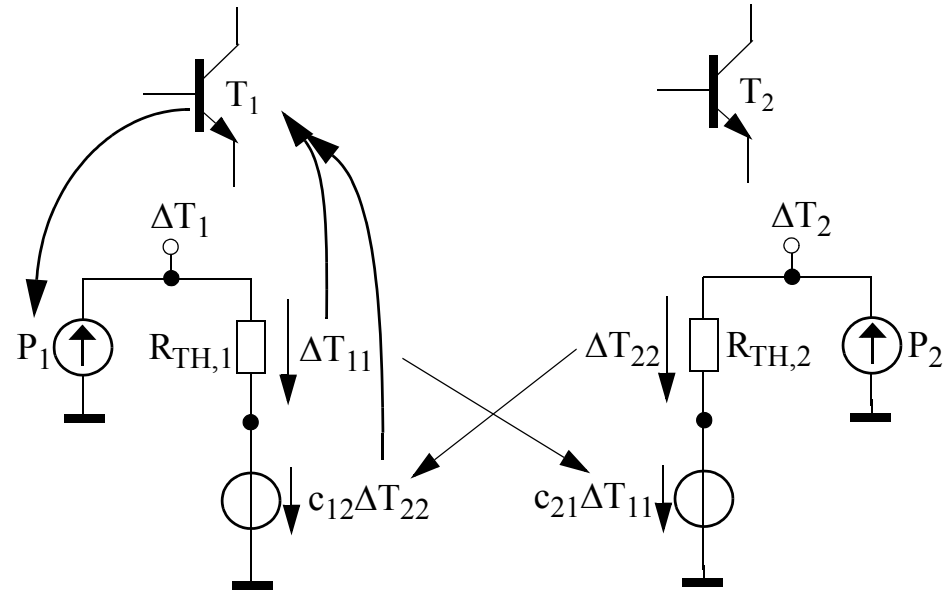
how to use the additional thermal node ?

- interaction between 2 heat sources

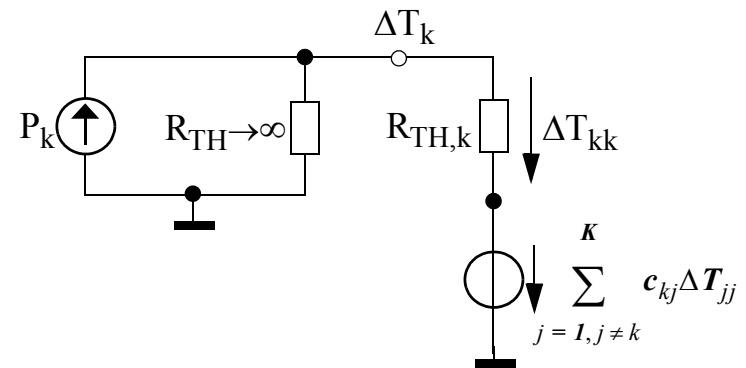
$$\begin{aligned} \Delta T_1 &= R_{TH,1} P_1 + c_{12} \Delta T_{22} \\ \Delta T_2 &= c_{21} \Delta T_{11} + R_{TH,2} P_2 \end{aligned}$$

with the thermal coupling coefficients

$$c_{12} = \frac{R_{TH,12}}{R_{TH,2}}, \quad c_{21} = \frac{R_{TH,21}}{R_{TH,1}}$$



- realization in a compact model using the externally accessible thermal node: VCVS approach



Development

- predictive and statistical modeling (in conjunction with TRADICA)
 - improved predictive equations:
 - now including correlations between PCMs => in progress
 - application to advanced SiGe processes (verification of critical 1D equations based on DEVICE)
 - verification for actual process data: industry partners
- main effects in (advanced) SiGe HBTs ($f_T > 200$ GHz and LEC-HBT)
 - improved physics-based collector model
(incl. high-current effects, barrier effects, avalanche, current dependent BC capacitance)
 - 3D GICCR theory and application to compact model element definition
 - high-frequency noise component decomposition
 - high-frequency (single- and multi-tone) distortion
 - Low-Emitter Concentration (LEC) SiGe HBTs
- III-V HBTs (AlGaAs, InGaAs, InP)
 - non-stationary transport => impact on transit time and transit frequency
 - geometry scaling (in conjunction with TRADICA)

Development - Related activities

- model hierarchy (in conjunction with TRADICA)
 - Level0: finished formulation v1.0, released Verilog-code for evaluation and simulator integration
 - Level4: variable multi-transistor model for critical applications
- parameter extraction
 - geometry scalable modeling:
 - continuous adaption to process development (extensions of existing and new methods)
 - tighter integration with existing tools (at, e.g., XMOD, Atmel, JazzSemi, ...)
 - integration in TRADICA (required for predictive modeling)
 - single transistor procedure and implementation (for HICUM/L0)
- modeling of effects common to all devices (in conjunction with TRADICA)
 - thermal modeling (geometry scaling of thermal resistance and impedance network elements)
 - geometry scaling: parasitic backend elements, substrate coupling network elements
using *fast* computational methods
- design of benchmark circuits
 - bandgap reference => verifying temperature behavior of model
 - LNA, PA, mixer, ... (LNA, BGR on Infineon test chip with kind support of P. Brenner)

Related activities (cont'd)

- most recent publications:

- [1] P. Sakalas, M. Schroter, P. Zampardi, H. Zirath, and R. Welser, "Microwave Noise Sources in AlGaAs/GaAs HBTs", IEEE International Microwave Symposium, Seattle (WA), pp. 2117-2120, 2002.
- [2] D. Berger, D. Celi, M. Schröter, M. Malorny, T. Zimmer, and B. Ardouin, "HICUM parameter extraction flow for a single transistor geometry", IEEE BCTM, Monterey (CA), pp. 116-119, 2002.
- [3] M. Schroter, H. Jiang, S. Lehmann and S. Komarow, "HICUM/Level0 - a simplified compact bipolar transistor model", IEEE BCTM, Monterey (CA), pp. 112-115, 2002.
- [4] M. Schröter, „Compact bipolar transistor modeling - Issues and possible solutions“, WCM, Proc. International Nano-Tech Meeting, San Francisco (CA), pp. 282-285, Feb. 2003.
- [5] R. Wittmann, J. Hartung, W. Tränkle, H.-J. Wassener, and M. Schroter, "RF Design Technology for Highly Integrated Communication Systems", DATE 2003, Munich, pp. -, March 2003.
- [6] M. Schroter, "Overview on the HICUM bipolar transistor model", invited Tutorial at the Modeling Workshop of the Fabless Semiconductor Association (FSA), San Jose (CA), Sept. 2002.
- [7] M. Schroter, "Compact device modeling for RF circuit design", invited Tutorial at the IEEE International Electron Devices Meeting (IEDM), San Francisco (CA), Dec. 2002.
- [8] P. Sakalas, M. Schroter, W. Kraus, and L. Kornau, "Modeling of SiGe power HBT intermodulation distortion using HICUM", accepted for ESSDERC 2003.
- [9] M. Malorny, M. Schroter, D. Celi, and D. Berger, "An improved method for determining the transit time of Si/SiGe bipolar transistors", accepted for BCTM 2003.

- HICUM User's Meeting at BCTM: replaced by general Compact Modeling Workshop

- CMC meeting in 12/02: see CEDIC web-site (http://www.iee.et.tu-dresden.de/iee/eb/eb_homee.html)

Availability of HICUM/Level2 V2.1 in Circuit Simulators

(Please contact simulator vendor for details and the latest status of availability)

<i>simulator</i>	<i>first release</i>	<i>latest release</i>	<i>comments</i>
ELDO-RF	10/99	9/02	ELDO v5.8_1.1 (AMS 2002.1) with externally accessible thermal node
SPECTRE-RF	10/99	11/01	<ul style="list-style-type: none"> • version > 446.100.70 with HICUM2.1 • (10/99: CNXT ref = HICUM2.0)
ADS	7/00	2/02	(combined with ICCAP); also, first version ADS2003
Smart-SPICE	11/00	11/00	can be combined with UTMOST
APLAC	10/01	10/01	APLAC 7.62a; new release upcoming in 03
HSPICE	2/01	2/02	version 2001.2 with HICUM2.0; AURORA compatible
MicrowaveOffice	03/03	03/03	HICUM/Level0 (for III-V HBTs)
Xpedion	in progress		
SPICE3F5	4/02	4/02	reference simulator

Apache NSpice, HSIM: code sent as per request

- Various (other) proprietary simulators (ASX (IBM), TEKSPICE...)
- Verilog-A version of model code; also, possibly stand-alone kit enabling coupling with other tools

Model support issues

demand for model support exceeds resources => need funding for full-time engineer

- simulator implementation
 - commercial simulators
 - lots of questions (some people do not seem to read the documentation)
 - model testing and verification of correct implementation => CEDIC (?) to certify quality of model implementation
 - company specific interfaces => will not support any of those anymore (but rather wait for model compilers)
=> these are main issues (license donations as compensation for effort and time are suitable in few cases only)

Note: effort and cost for commercial implementation is as large as for development

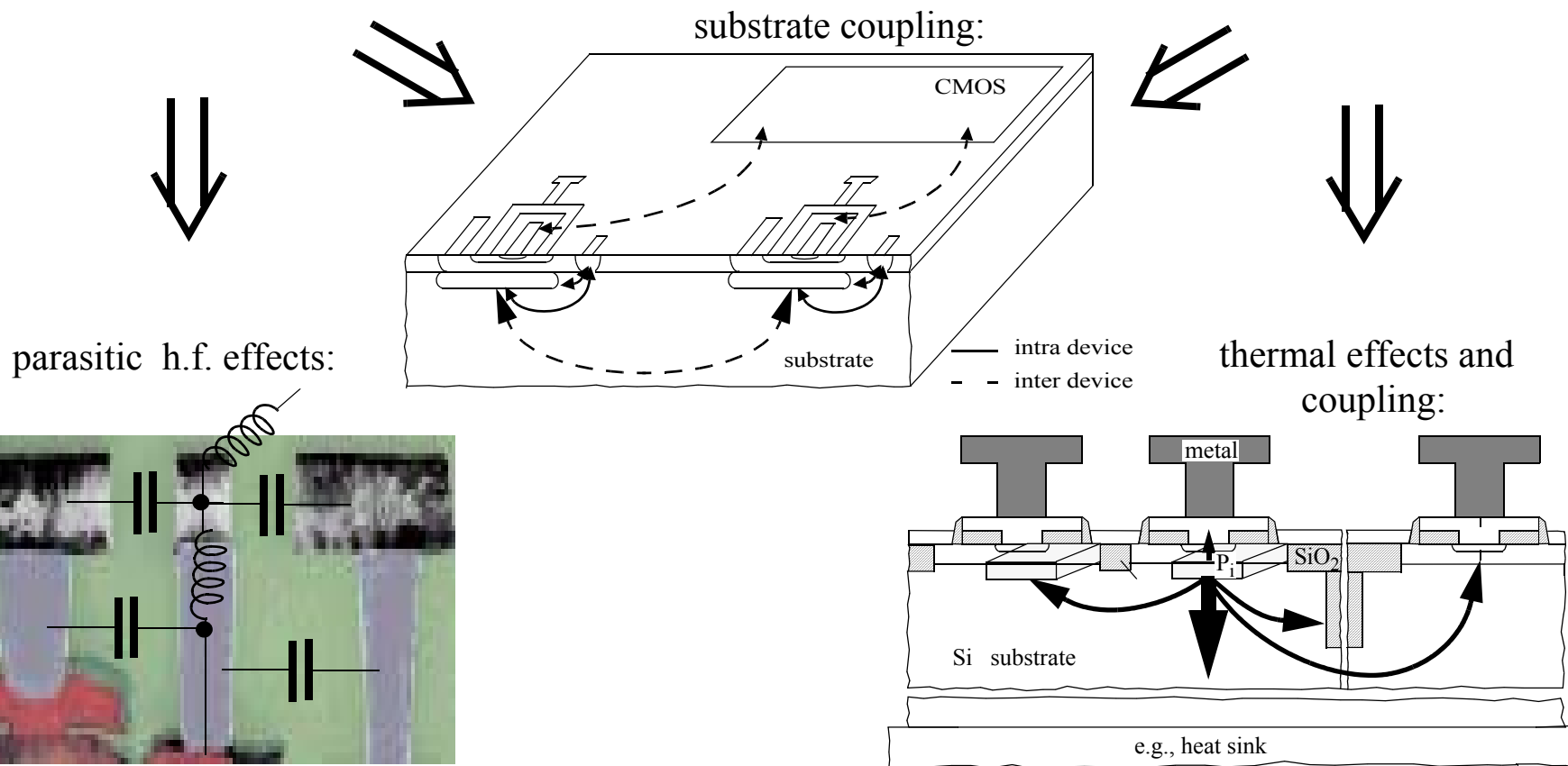
- internally required code development
 - DEVICE (to avoid licensing and platform compatibility issues)
 - Verilog-A for distribution and model compilers
 - development tool, e.g. MATLAB, but probably migration to TRADICA (needed anyway) or stand-alone kit
 - MNA stand-alone kit (for linking model to extraction tools) => requested by some customers
 - symbolic tool for derivatives (e.g., MAPLE) => will be dropped once model compilers are available
=> will focus on DEVICE, Verilog-A, TRADICA [, stand-alone kit]
- parameter extraction
 - should a tool developed at CEDIC be made (publicly) available ?
If yes, it needs to be commercialized in order to be able to pay for support and updates !!
=> XMOD approach seems to be the most suitable path
- circuit designers => pay for EDA tools => pass on portion of fees for model support ...

TRADICA development

Improvements towards critical applications: Trends in Communication Systems ...

higher frequencies (Broadband)

higher integration (SoC)



... effects have impact on circuit performance (noise, linearity/ACPR, ...) and modeling
 ⇒ need accurate modeling for reducing design iterations and cost

TRADICA development

- technology modeling (complete model kit generation)
 - fast computational methods for calculating geometry dependent
 - thermal resistance
 - substrate resistance
 - backend parasitics
 - integration of passive device model generation
 - planned: integration of MOS model (depends on interest and funding)
- model hierarchy
 - Level4: automatic parameter generation from Level2
 - for distributed electrical EC => finished (without cell interconnect yet) and under test
 - for distributed electro-thermal EC => under construction
 - Level0: automatic parameter generation from Level2 available
- parameter extraction
 - conversion from HICUM/Level2 to: SGPM (available), VBIC (planned), MEXTRAM (desired ?)
 - implementation of generic building blocks:
 - flexible definition of procedure by user
 - add-on of GUI provides graphical capability (also targeted for education purposes)
 - automated extraction from DEVICE simulation

TRADICA development

- predictive modeling towards concurrent engineering
 - automated DEVICE runs and extraction of technology specific parameters
 - planned: GUI for improved DEVICE input (depends on interest and funding)
 - implementation of predictive analytical equations (in progress)
- circuit modeling and design aid
 - analytical equations for circuit FoMs (results on CML, ECL already developed)
 - development of sizing criteria for all devices (in progress)
- statistical modeling
 - internal DoE and RSM procedures (very fast when using TRADICA internal models)
 - in design system in conjunction with, e.g., CircuitSurfer
- link to other tools
 - DEVICE (in progress)
 - circuit simulators using a generic interface (in progress)
 - integration into design system (in progress) => see separate slide

Integration of TRADICA into Cadence Design Framework

transistor specification in schematic capture:

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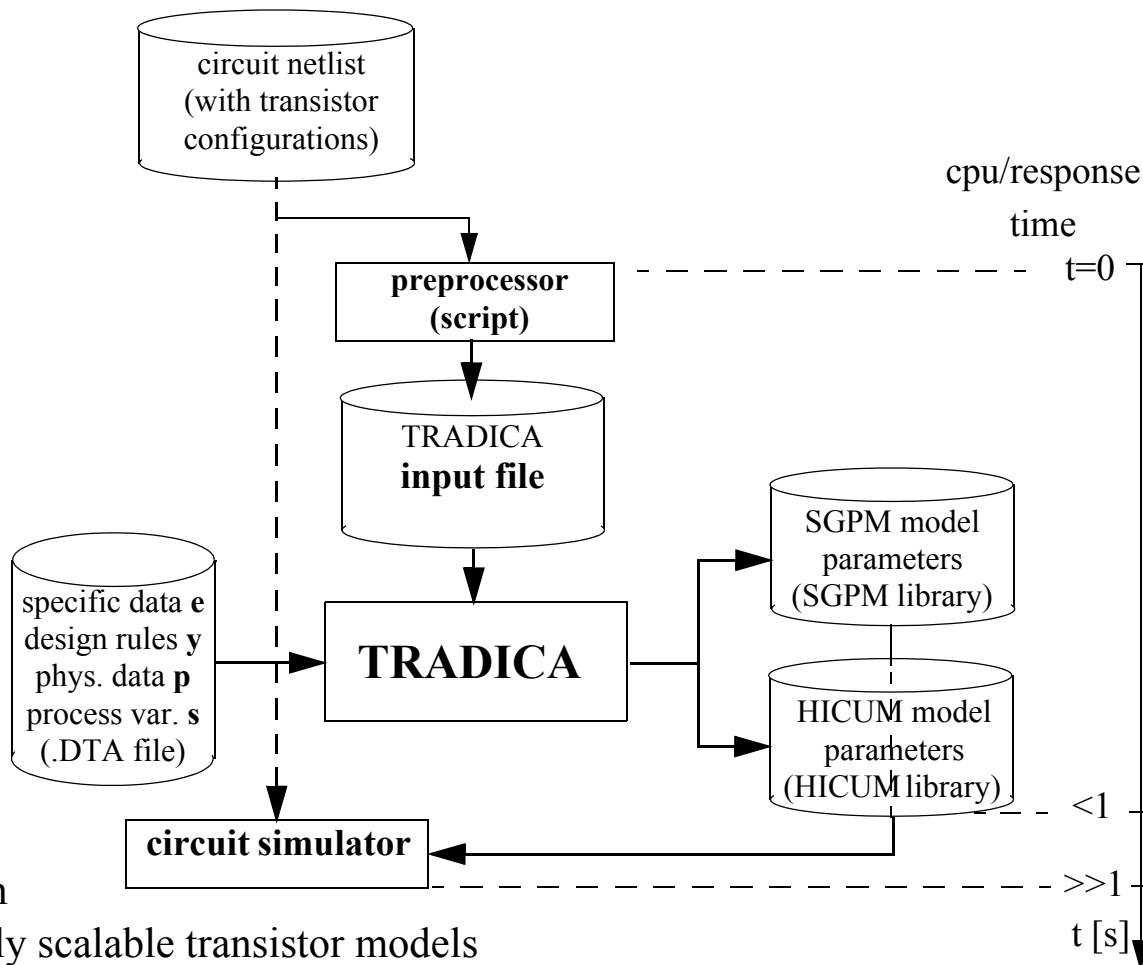
Q5
emitter width [μm]: 1.0
emitter length [μm]: 20.0
number of emitters: 2
number of bases: 1
number of collectors: 2
collector location: side
parallel devices: 1
contact sequence: CEBEC
    
```



Benefits:

- statistical and matching simulation
- circuit optimization via consistently scalable transistor models
- parameter transfer via single "technology" file (xxxx.DTA)

⇒ significant enhancement of functionality for design at reduced maintenance effort for foundry



Discussion session

- existing solutions - summary: what works well and what doesn't
- missing procedures (suggestions/priorities for development)
- geometry scaling issues
- test structure issues
- case studies

Proposal for model development and "productization"

Issues

- CMC "approach" **does not work** for bipolar: no funding, too much politics, no common agenda etc. (fees=\$240k, Berkeley=\$80k, what is the remaining money of \$ 160k being used for ?)
- **development**: model developer (usually university) receives funding from interested companies and works on *company-specific* topics - consequences and disadvantage:
incoherent model and long-term maintenance issues → overall increase of support effort and cost
- **productization**: does not satisfy research criteria but requires significant effort and cost
→ consequence: model developer, e.g. university, cannot provide (sufficient) support

Solution

- only *companies with interest in a particular model* participate in model definition and *create funding pool*
- model developer channels development results into **common** model

→ Advantages

- cost reduction through cost sharing (the larger the number of companies the smaller is the cost/company or the faster is the development and productization process)
- definition of common goals by all participating companies is obtained easier and faster compared to a group (such as the CMC) with interests in different model types and politics

Issues from model developer point of view

- work *must*
 - have sufficient research (theory and experiment) contents to qualify for theses
 - not be service work competing with existing companies to avoid law suits
- implementation of results
 - for demonstration purposes only
 - *must not require* significant manpower (examples: GUI, coding in *several* simulators, ...)
 - cannot use cost-expensive EDA tools
- release/deployment *must not require*
 - significant maintenance (including, e.g., legacy issues, extensive versioning effort)
 - to be forced into legal obligations and responsibility for functionality other than for developed case
 - to be forced to disclose IP into public domain (in violation of existing laws for inventions)

