

Modeling and scaling of III-V  
HBTs using HICUM and  
TRADICA

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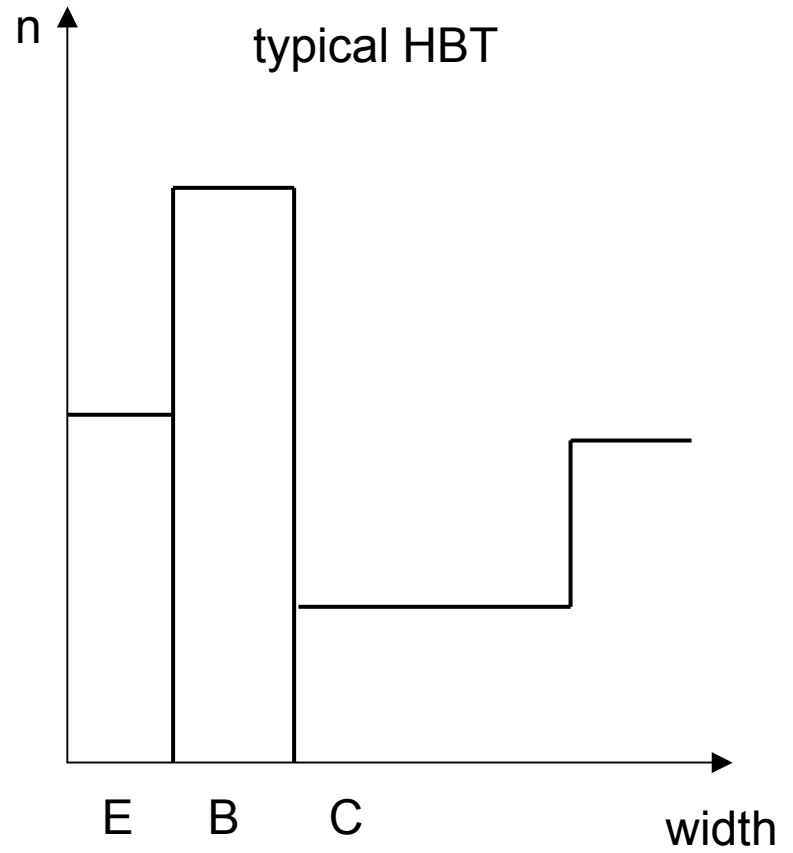
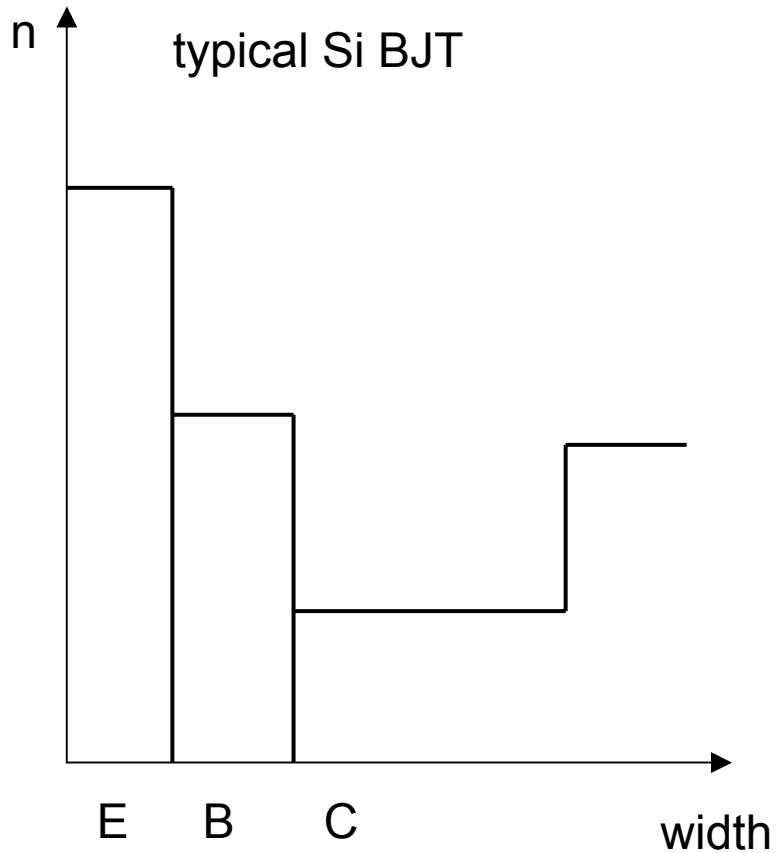
# Situation

- Increasing demand for power amplification at high speeds
- Pure silicon devices limited by material characteristics and design principles
- Trend goes towards hetero-structure devices (HBTs)
- Introduction of silicon-germanium transistors (already implemented in modern BiCMOS-technologies)
- Search for alternative materials (e.g. gallium-arsenide)
- Silicon technologies covered by the modeling community very well
- Need for accurate models describing differences in physics and geometry of HBTs

# Advantages of HBTs

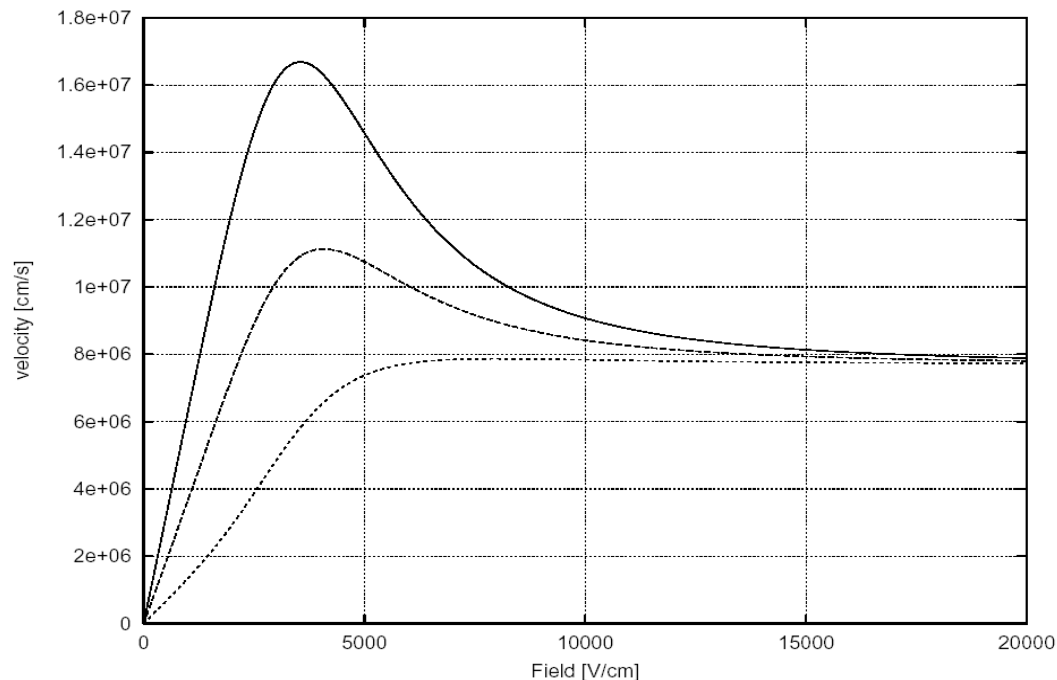
- Higher carrier mobility (Si:  $\sim 1.3\text{cm}^2/\text{Vs}$  GaAs:  $\sim 5.0\text{cm}^2/\text{Vs}$ )
- Different bandgaps of emitter and base material (current gain controlled not only by doping concentration)
- Implementation of a “build-in-field” in the base layer by doping AND compositional grading
- Velocity overshoot effects in the base-collector SCR increase transistor speed
- Well controlled layer growth and composition due to molecular beam epitaxy technology
- Simple geometry of mesa-HBTs compared to typical silicon transistors

# Doping profiles

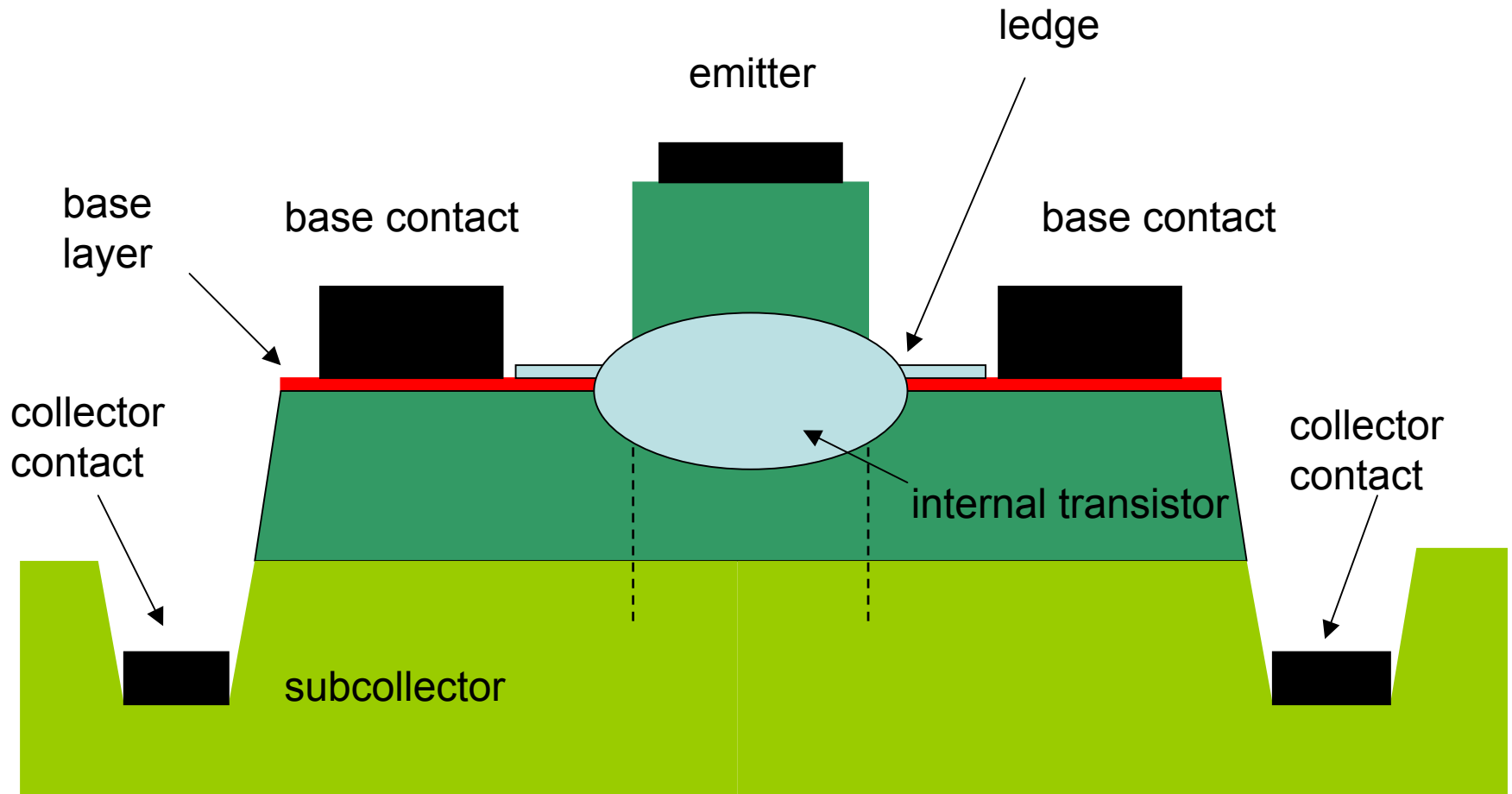


# Disadvantages of HBTs

- Lower thermal conductivity
- Lower integration density (technology development far behind silicon)
- Actual wafer sizes 150mm (6")
- Non-monotonic velocity-field characteristics

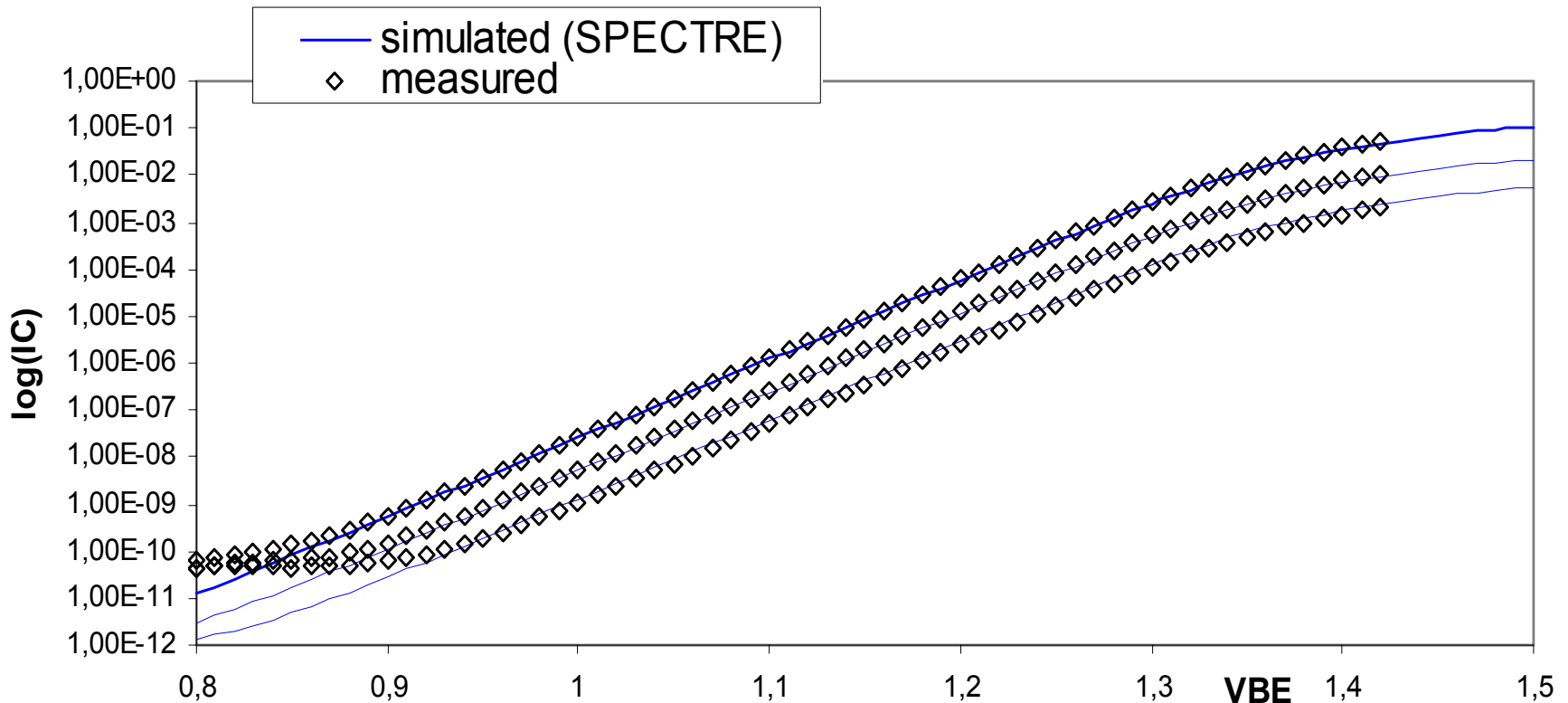


# mesa-HBT cross section



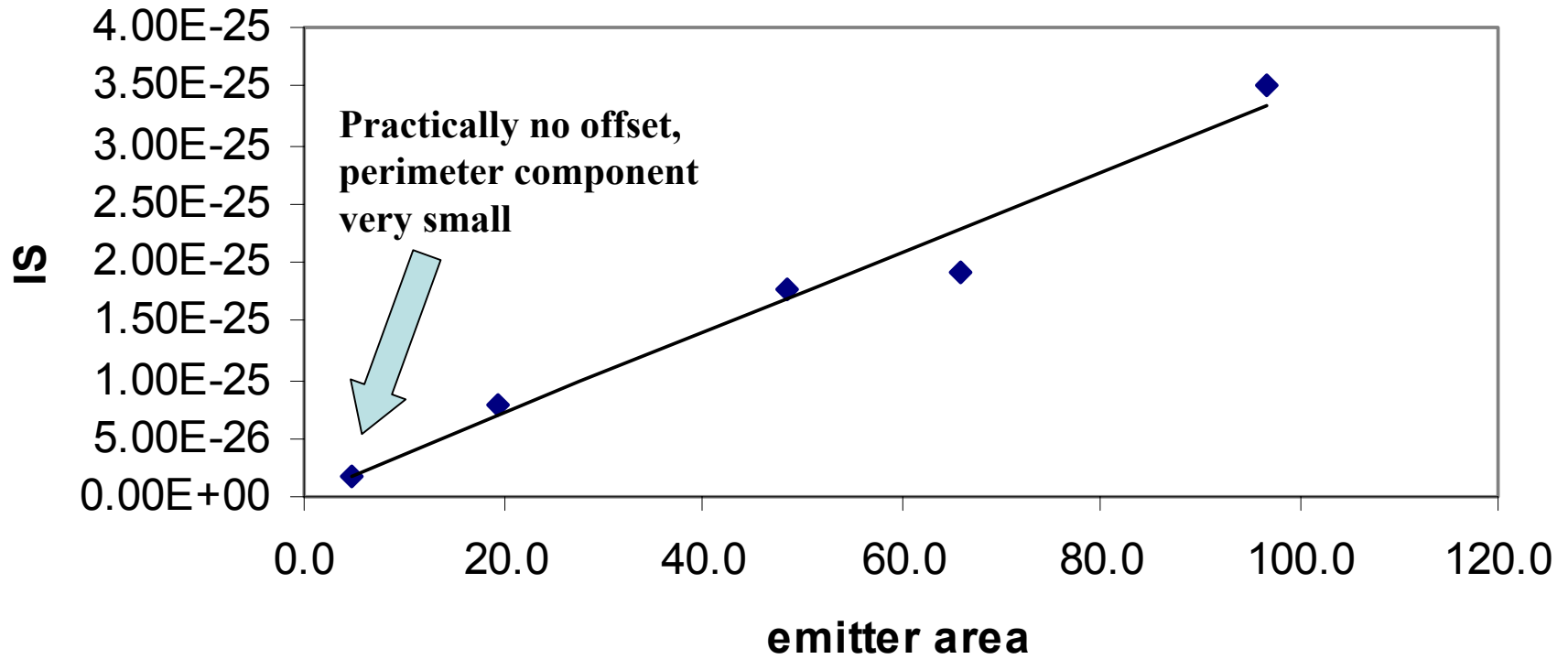
# Gummel characteristics verification

**IC vs. VBE measured and simulated for different emitter areas**



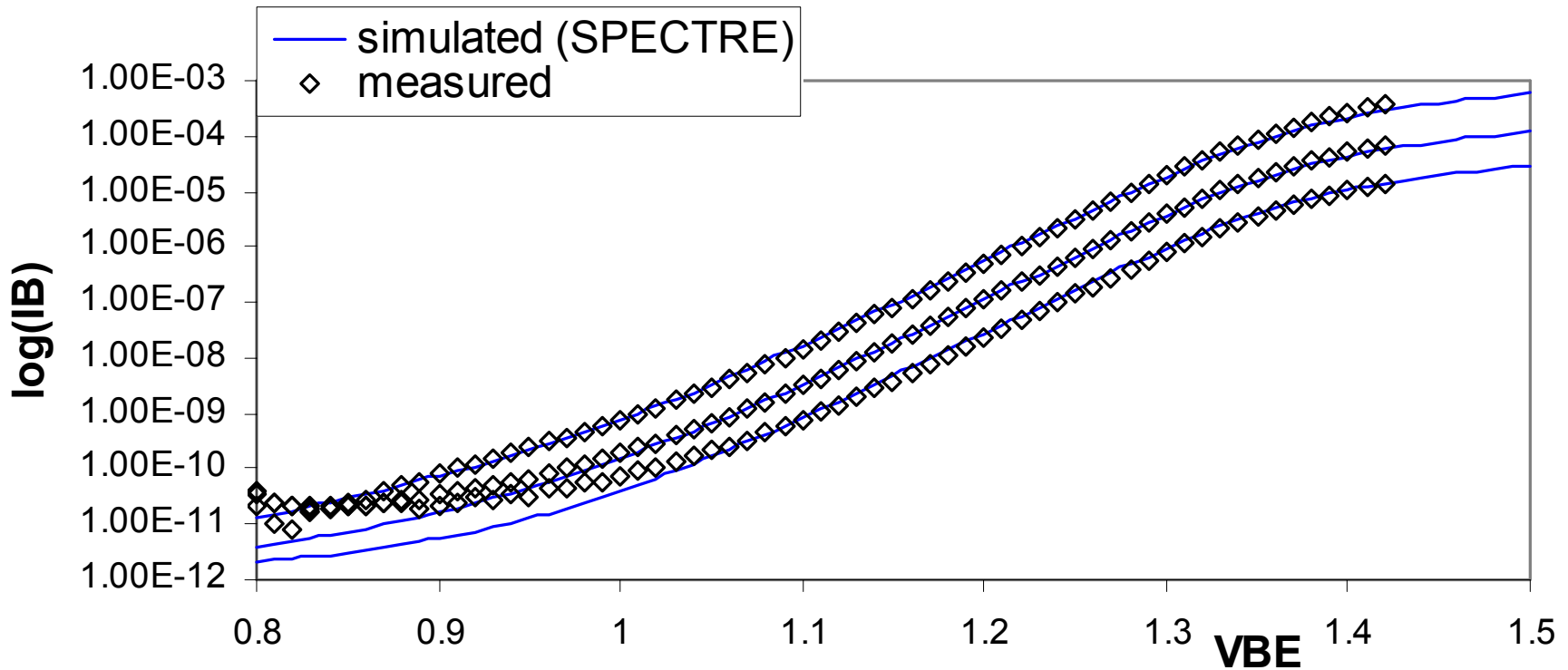
# Collector current scaling

## geomtry scaling of transfer current $I_S$



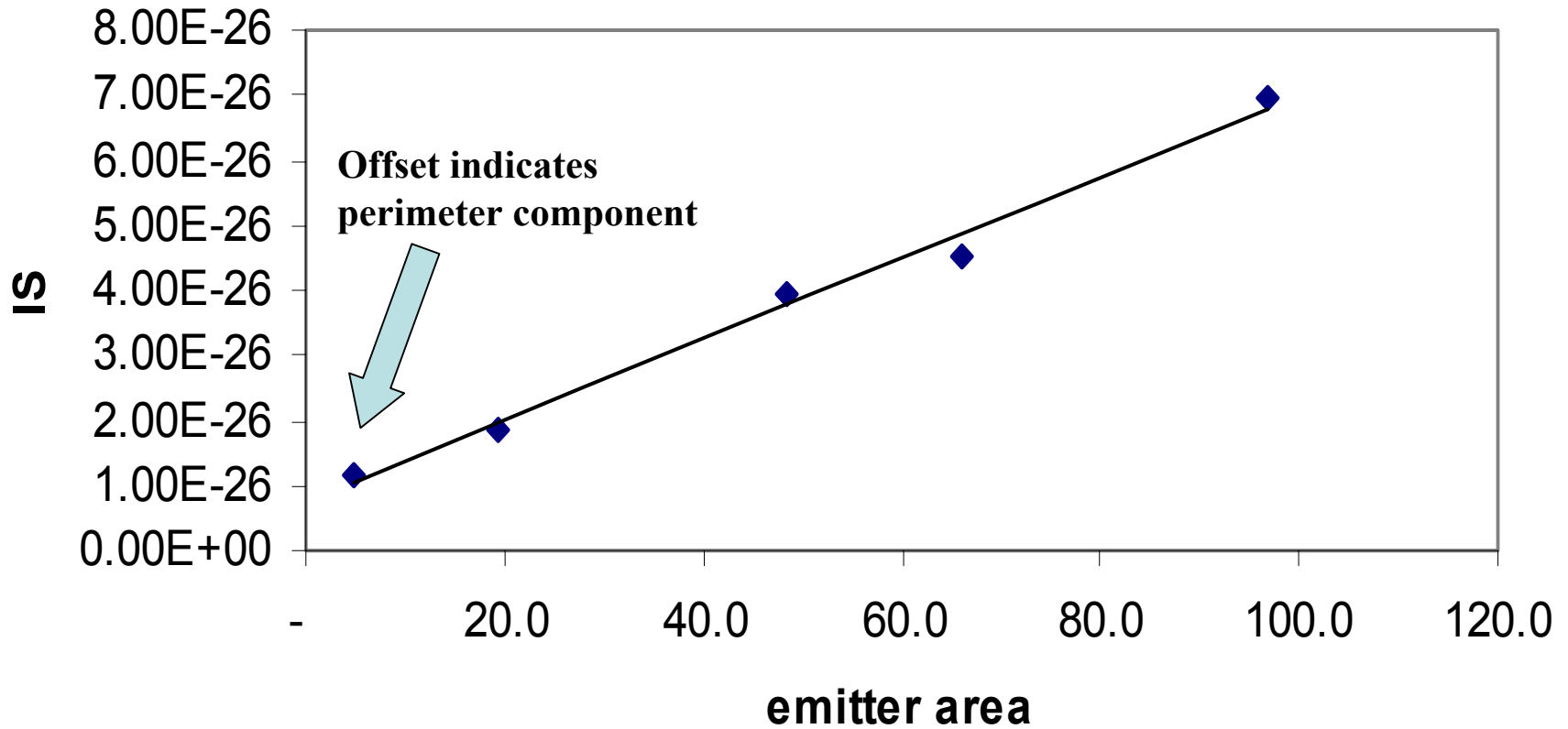
# Gummel characteristics verification (rectangular devices)

**IB vs. VBE measured and simulated for different emitter areas**



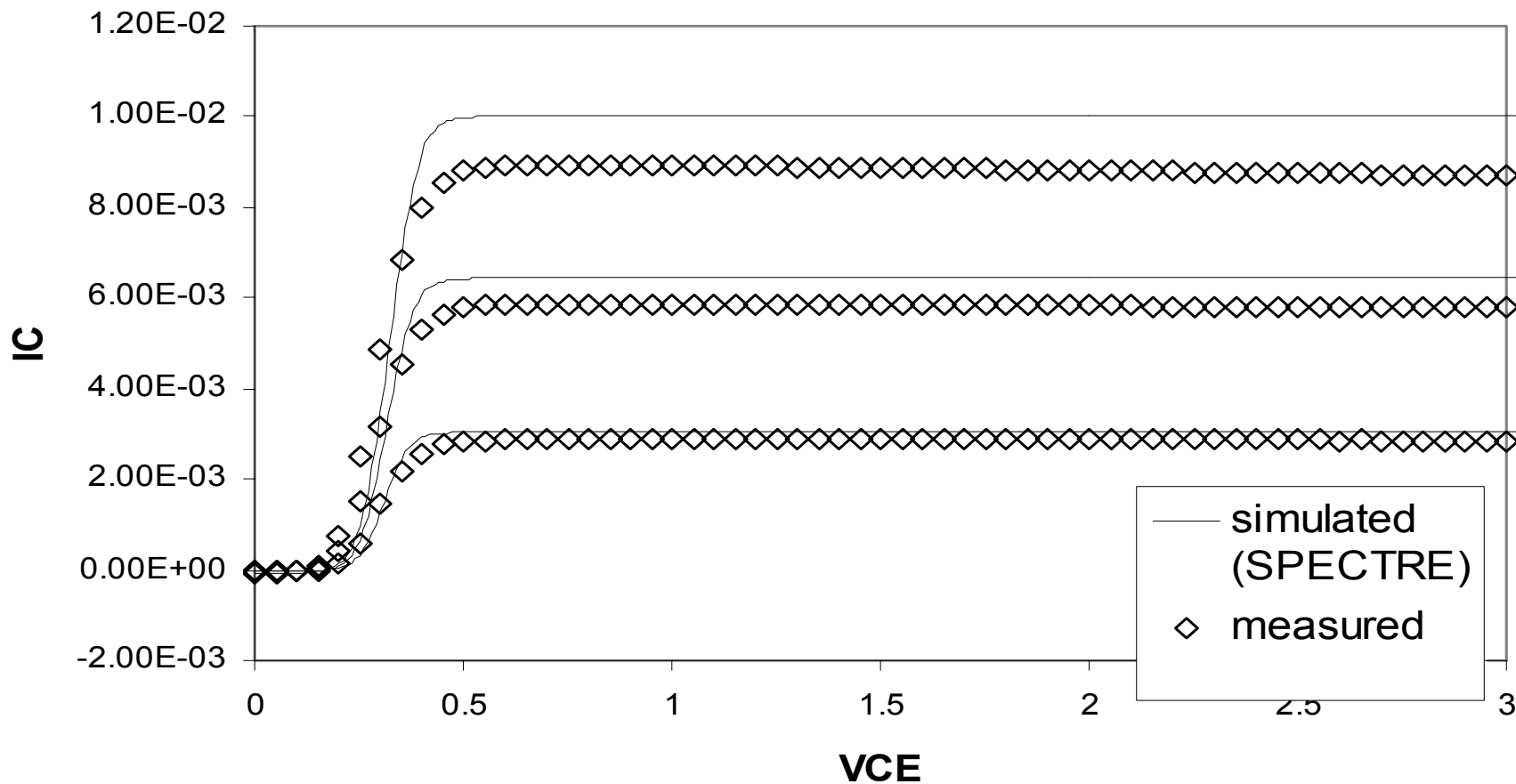
# Base emitter current scaling

## geometry scaling of base emitter current IBE



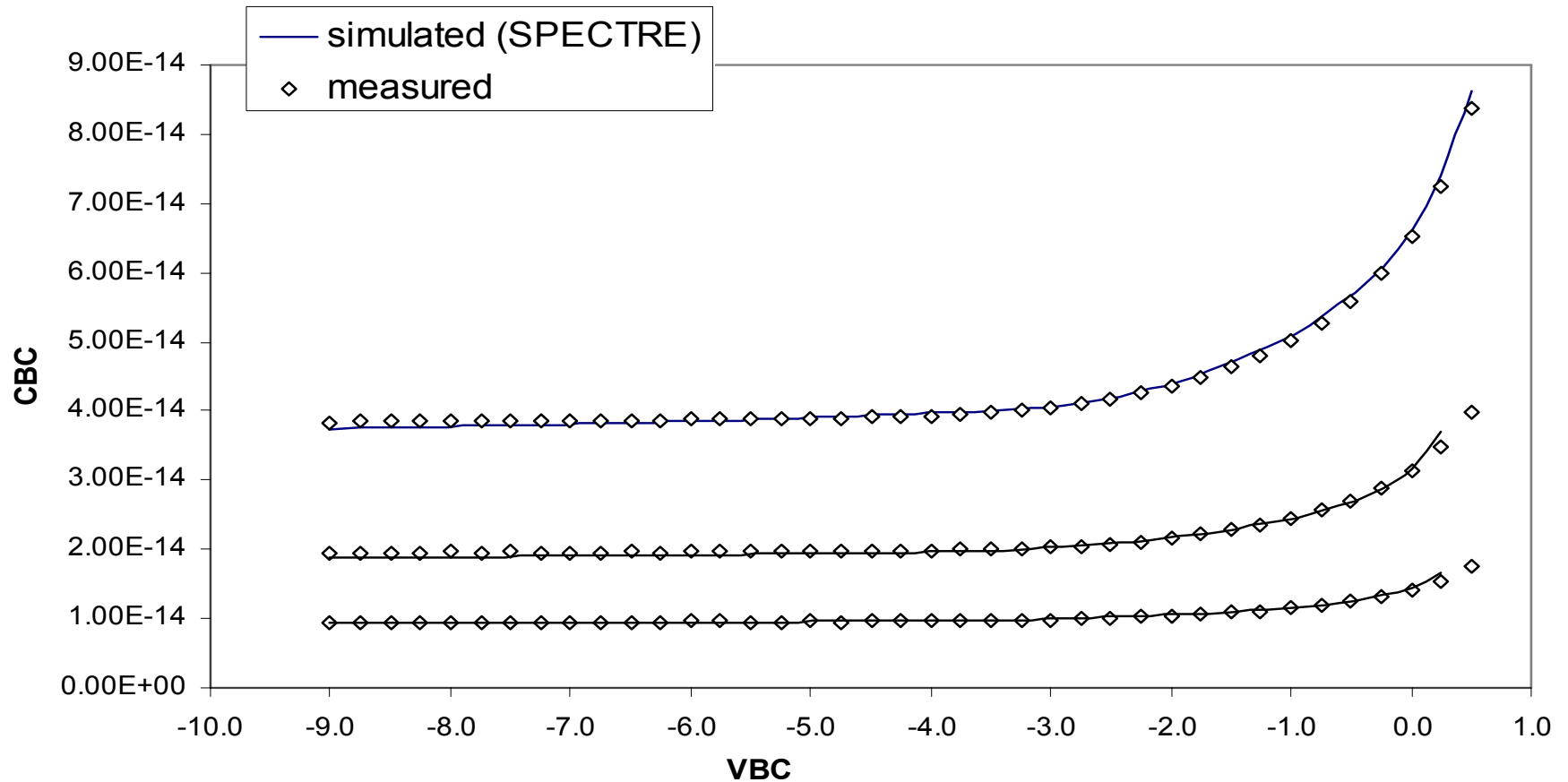
# Output curves verification

## output curves (forced IB)

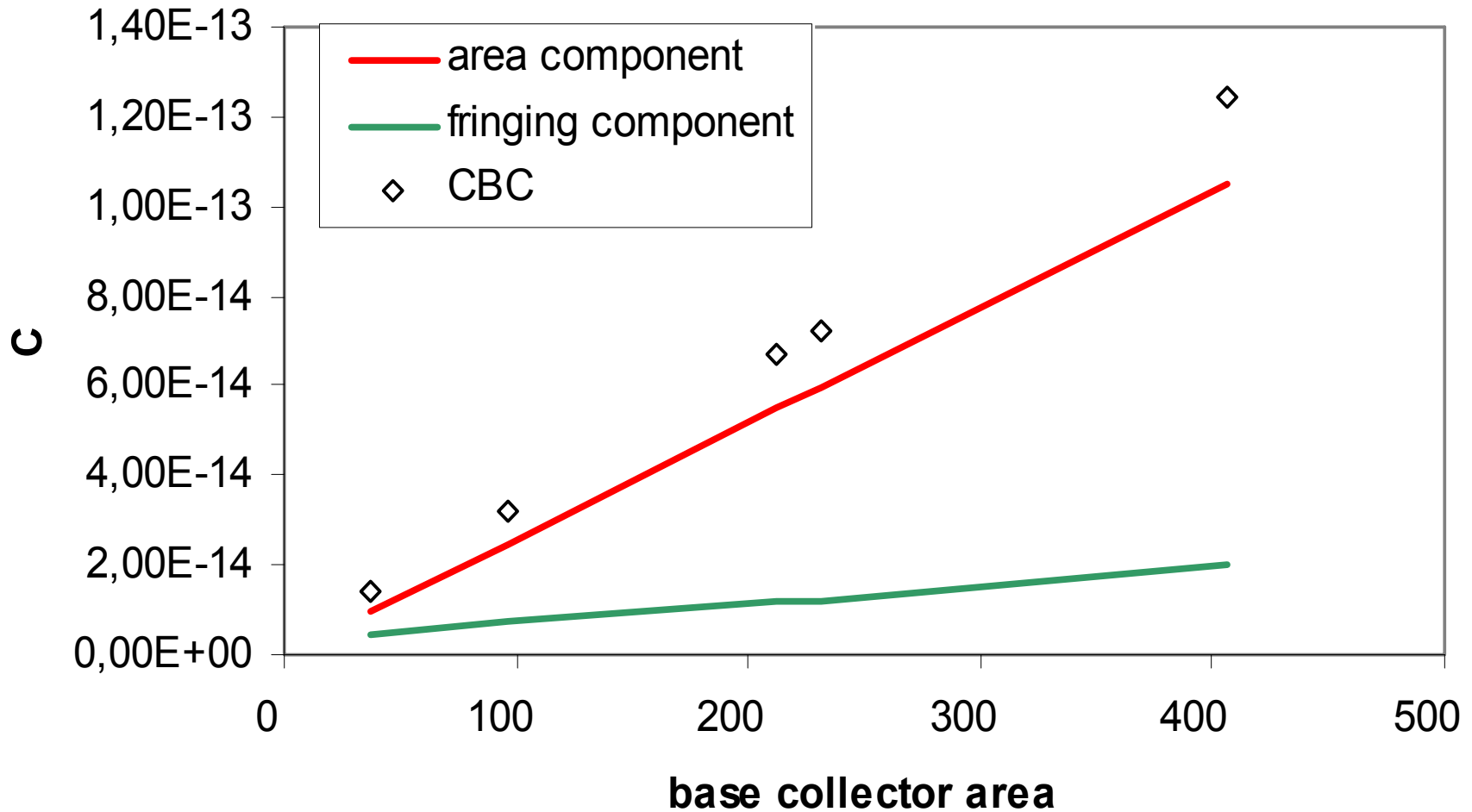


# Base collector depletion cap.

**CBC vs. VBC measured and simulated for different transistor sizes**

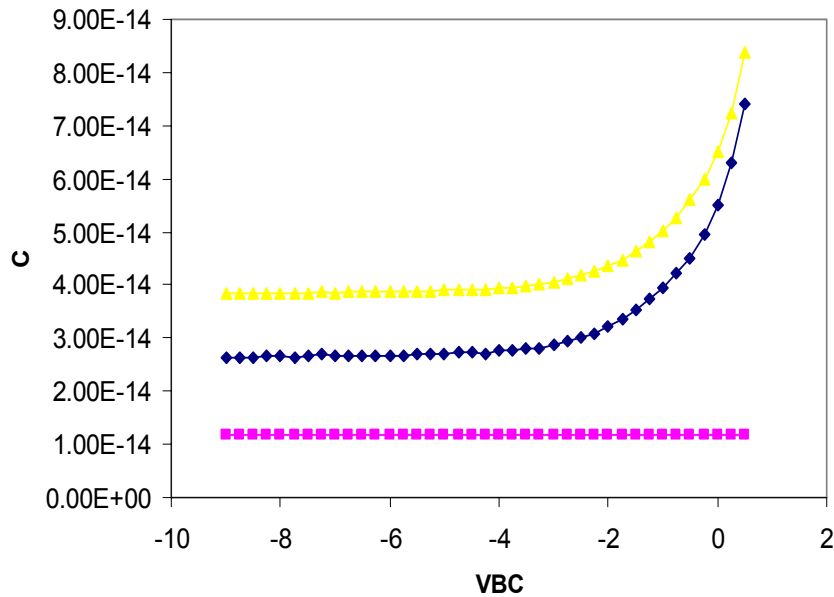


# CBC geometry separation and scaling

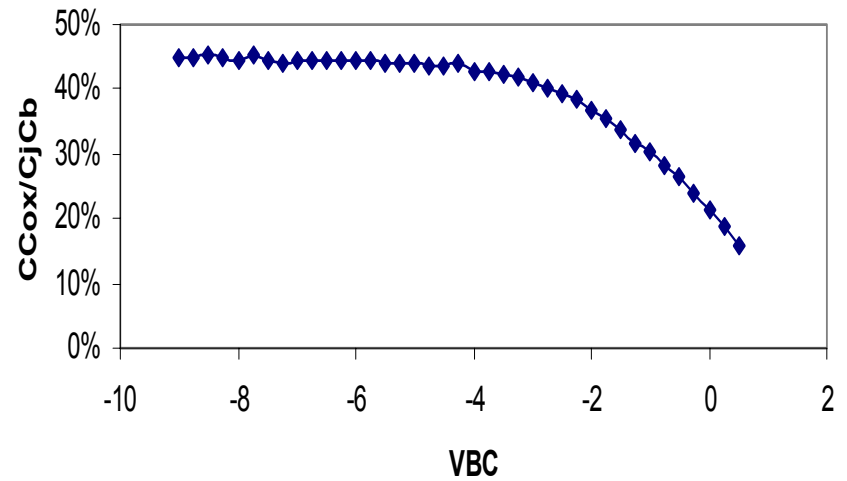


# BC fringing capacitance

CBC geometry split vs. VBC

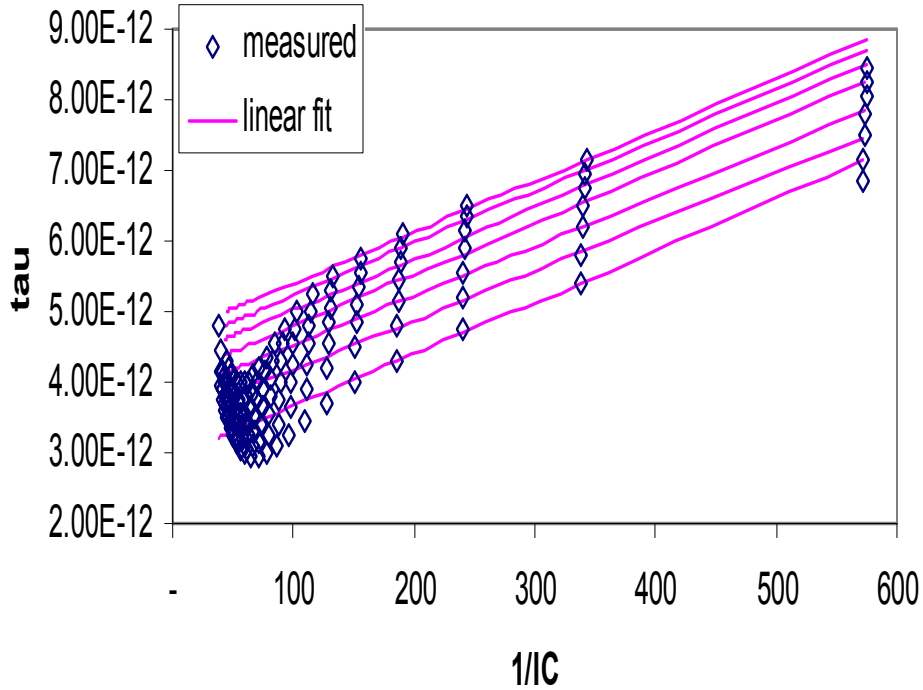


ratio of CBC fringing component to area component vs. VBC

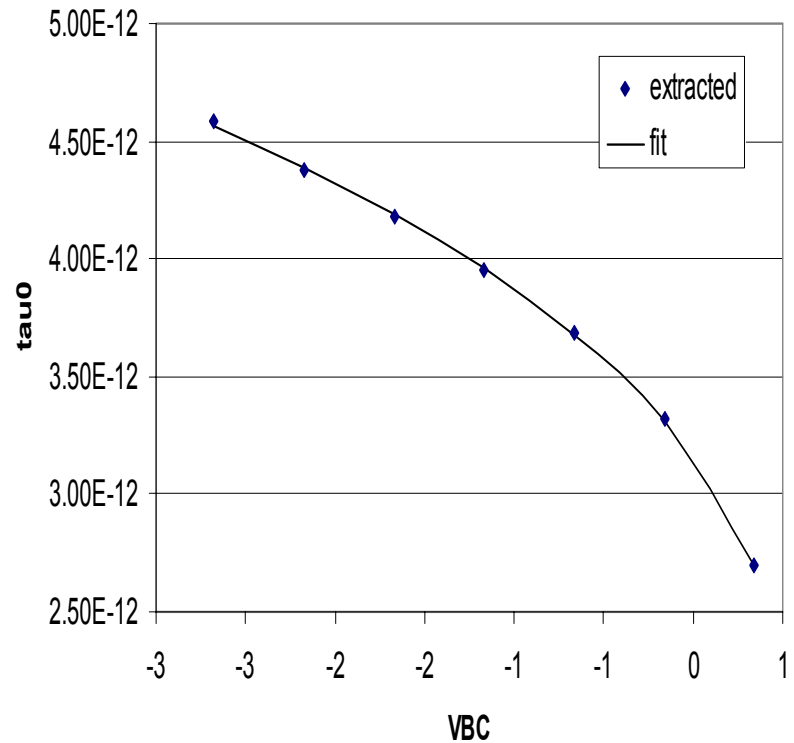


# Low current transit time

extraction of low current transit time



low current transit time  $\tau_0$  vs. VBC



# Summary

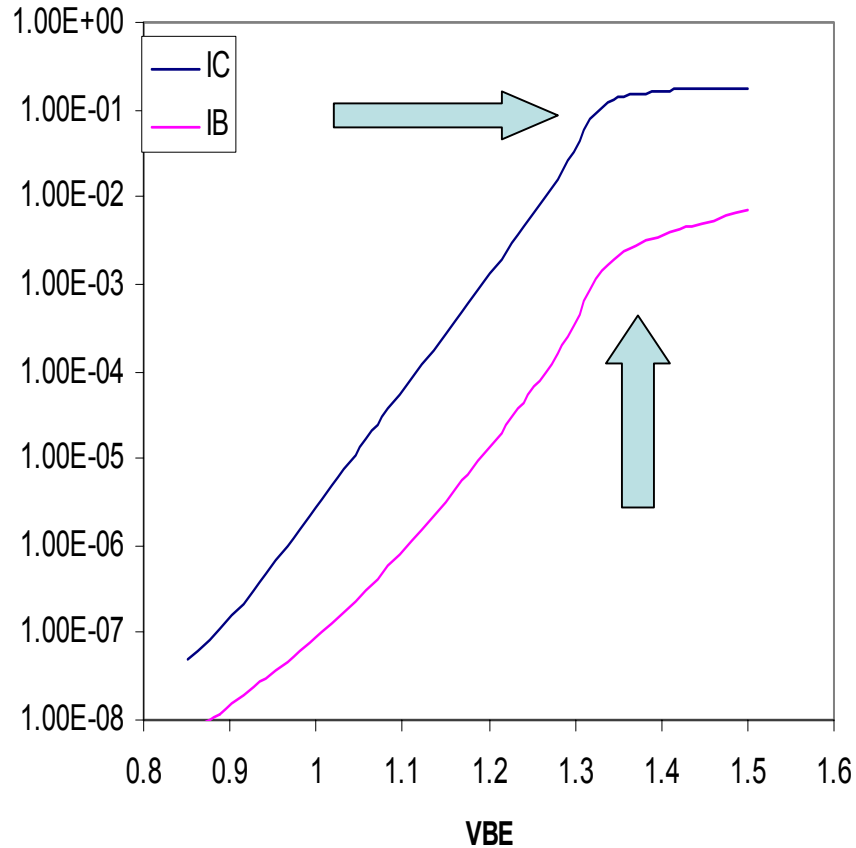
- HICUM model well suited for modeling DC characteristics
- Transit time model in HICUM has to be enhanced (velocity overshoot)
- Scaling equations in TRADICA well suited for mesa-HBTs
- Model parameter generation with TRADICA possible for low IC applications

# CONEXANT's HBT-3 process

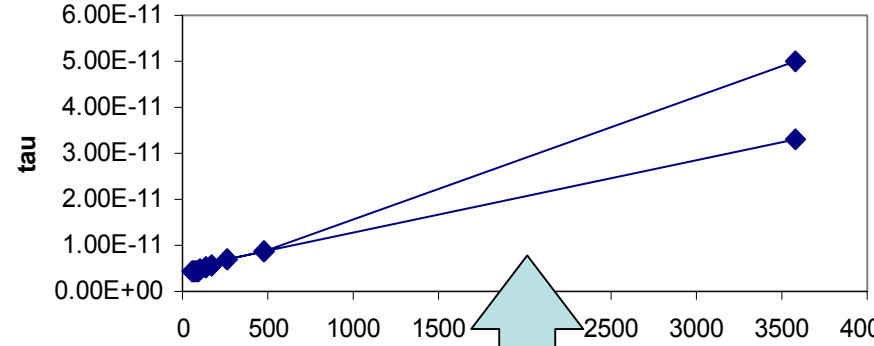
layer	material	dopants
substrate	GaAs	semi insulating
subcollector	n GaAs	Si
collector	n GaAs	Si
base	p GaAs	C
ledge (emitter)	n AlGaAs	Te
emitter 1	n GaAs	Te, Si
emitter 2	n InGaAs	Te, Si

# Importance of accurate measurements

Gummelplot



transit time vs.  $1/I_C$



transit time vs.  $1/I_C$

