

R_{TH} Scalable Model for NPN devices in a 0.35 μ m SiGe Technology without deep trench

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Introduction

- Introduction
- R_{TH} extraction
- Mono-emitter scalable approach
- R_{TH} for multi-emitter devices
- Electrical characteristics
- Conclusion

- Availability of a HICUM scalable model for the NPN devices of BiCMOS6G technology (0.35μm, LOCOS isolation, f_T around 45GHz). Temperature parameters (V_{GB}, A_{LB}) have been extracted as well.
- R_{TH} extraction performed for each transistor of a large set of devices (few L_E and W_E, interdigitated structures).
- Scaleable approach for mono-emitter devices using simple resistance analogy.
- Multi-emitter transistors behaviour is more complex.
- Comparison between measurements and simulations without/with self-heating on main electrical characteristics.

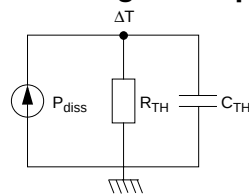
COMMENTS:

- The work on a R_{TH} scalable model starts with a 0.35μm BiCMOS technology featuring SiGe LV and HV NPN devices (Bv_{ceo} equal to respectively 3.3V and 5.0V). A HICUM scalable model is available for these devices including temperature parameters (zeta's, V_{GB}, A_{LB},... extracted from measurements).
- For a large set of devices (geometries used for the HICUM scalable model extraction and validation, few L_E and W_E and multi-emitter devices) DC and AC measurements were available (no transient measurement). Using these data a single-geometry R_{TH} extraction is performed for every devices.
- Using the R_{TH} extracted values versus the devices geometries, a scalable approach is built based on an electrical analogy for the R_{TH} calculation (R_{TH} is calculated as a simple resistance). The mono-emitter devices give straight-forward results whereas the multi-emitter transistors behaviour is more complex.
- Finally interesting comparisons between the scalable model with/without R_{TH} and measurements are drawn for the main electrical figures (Output characteristics, f_T,...).

R_{TH} Extraction (1)

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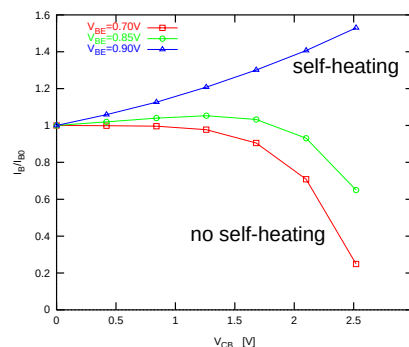
- Self-heating description in HICUM is done via a thermal sub-circuit:



$$\Delta T = R_{TH} \cdot P_{diss}$$

$$\text{with } P_{diss} = V_{BE} \cdot I_B + V_{CE} \cdot I_C$$

- Base and collector currents are very sensitive to temperature, so I_B is used as a temperature sensor (knowing V_{GB} , A_{LB}):



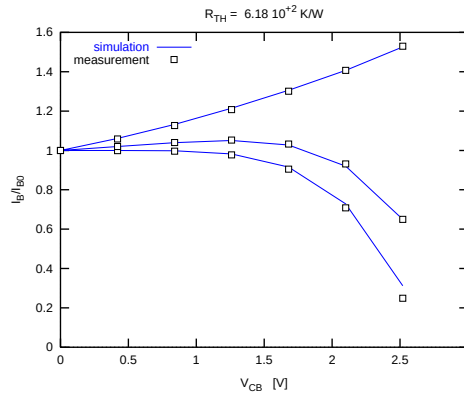
COMMENTS:

- The R_{TH} extraction is done in the frame of the HICUM model. The self-heating is described with a thermal sub circuit that uses an electrical analogy. The thermal power dissipated in the device is considered as a current generator in a simple RC circuit (R_{TH} and C_{TH}). The temperature elevation (ΔT =internal device temperature minus room temperature) is considered as the bias. The thermal power is calculated with I_C and I_B and the bias conditions.
- The electrical characteristics used for the R_{TH} extraction are the $I_B(V_{CB})$ curves at different constant V_{BE} values because I_B is very temperature sensitive. Below a certain V_{BE} value (around 0.7V) no self-heating impact could be detected. If V_{BE} increases (0.85V), the self-heating makes I_B increases with V_{CB} until the avalanche phenomenon takes over. For higher V_{BE} (0.90V) the self-heating is dominant, and avalanche phenomenon limit is pushed away.

R_{TH} Extraction (2)

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- The R_{TH} extraction is 'single geometry', i.e. performed for each device at 27°C. It is a global optimization on I_B(V_{CB}) at V_{BE}=cst curves:



- This extraction is performed on devices with L_E from 0.8μm to 40μm, W_E from 0.4μm to 1.6μm, N_E from 1 to 6.

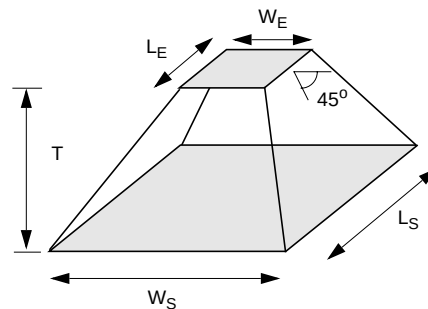
COMMENTS:

- R_{TH} value is extracted with an optimization on the I_B(V_{CB}) curves measured at room-temperature.
- On the plot, measurement data are points whereas the simulation is drawn with lines. The influence of the R_{TH} parameter is dominant for V_{CB} lower than 1V, where there is no avalanche. For higher V_{CB} where avalanche occurs, avalanche temperature parameters are sensitive as well (ALFAV, ALQAV are optimized). Avalanche phenomenon is temperature sensitive.
- The R_{TH} extraction is performed for devices with L_E from 0.8μm to 40μm, W_E from 0.4μm to 1.6μm, N_E from 1 to 6.

Mono-emitter scalable approach (1)

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- It is assumed that the heat flows from the emitter surface to the silicon substrate with a 45° angle with respect to the surface (no deep trench).
- Electric resistance analogy: the thermal resistance may be expressed with a pyramidal resistance formula (P. R. Gray and R. G. Meyer, "Analysis and Design of Analog integrated circuits", third edition, 1993):



$$R_{th} = \frac{\rho_{th} \cdot T}{W_E \cdot L_E} \cdot \frac{\ln(a/b)}{(a-b)} \quad (\text{Eq-1})$$

with $a = \frac{W_E}{W_S}$ and $b = \frac{L_E}{L_S}$,
 ρ_{th} the thermal resistivity,
 and T the wafer thickness ($= 350\mu\text{m}$).
 W_S and L_S could be easily calculated:

$$L_S = L_E + 2 \cdot T$$

$$W_S = W_E + 2 \cdot T$$

COMMENTS:

- The scalable approach is based on the calculation of the thermal resistance with a simple electrical resistance formula.
- The heat is assumed to flow from the emitter surface down to the silicon substrate with a 45° angle. In this technology there is no deep trench that can stop the lateral dissipation of the heat. Thus the heat is supposed to flow through a pyramid.
- Using the formula of an electrical pyramidal resistance, the thermal resistance could be calculated with the device dimensions.
- Eq-1 gives the thermal resistance versus the thermal resistivity, the wafer thickness and the emitter dimensions.

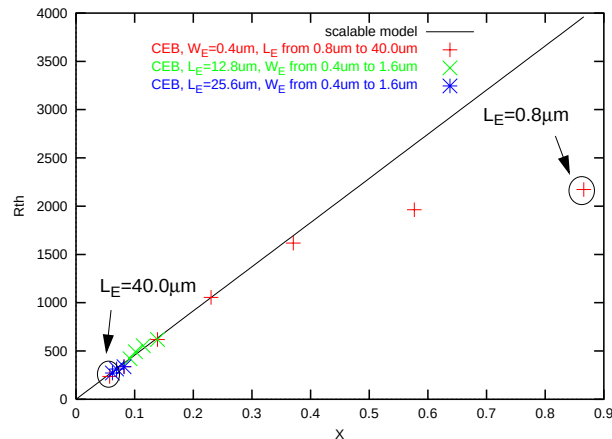
Mono-emitter scalable approach (2)

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□ Eq-1 could be written as:

$$R_{th} = \rho_{th} \cdot X \quad \text{with} \quad X = \frac{T}{W_E \cdot L_E} \cdot \frac{\ln(a/b)}{(a-b)} \quad (\text{Eq-2})$$

□ A linear regression is performed on Eq-2:



□ Pyramidal resistance scaleable model is validated!

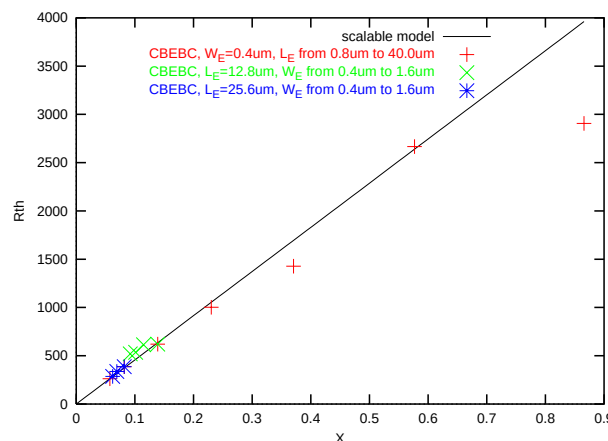
COMMENTS:

- Eq-1 is modified in Eq-2, where the thermal resistance is the product of the thermal resistivity and a geometrical factor.
- A linear regression is performed on Eq-2 using the R_{TH} values extracted on each CBE devices geometries.
- The points are well aligned for long and large devices. This validates the pyramidal resistance approach. The short devices have lower resistances than expected.

Mono-emitter scalable approach (3)

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- Extracted ρ_{TH} value = $4.575 \cdot 10^{-3} \text{ m.K/W}$ vs silicon: $\rho_{TH} = 6.666 \cdot 10^{-3} \text{ m.K/W}$ ($\kappa_{TH} = 1/\rho_{TH} = 150 \text{ W/m.K}$): SiGe layer? too simplistic model (non-uniform T°)?
- Lower R_{TH} for small devices: 3D dissipation effect?
- Validation on CBEBC devices:



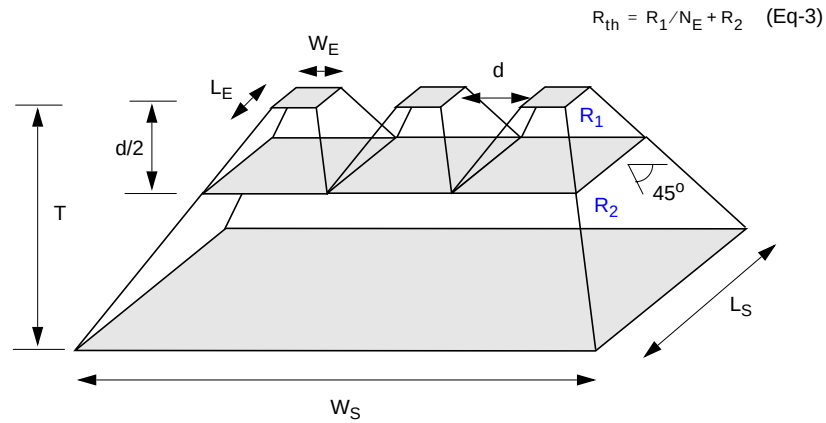
COMMENTS:

- The extracted ρ_{TH} value is 30% lower than the value found in literature for Si. This could have several explanations: the base of the transistor (region where the temperature is maximum) is a SiGe layer and not a Si layer, the model is too simple (R_{TH} should distinguish two contributions, one for the device-where the heat is created- one for the substrate-where the heat is dissipated-), the geometrical modeling of the heat flow (45° pyramid) is not the most accurate...
- The shortest devices have lower R_{TH} values than expected with the pyramidal model. This could have several explanations: as for other electrical characteristics (f_T , output characteristics) short devices could sometimes have a not-typical behaviour (due for instance to a not-typical vertical doping profile) compared to long ones, 3D dissipation effect: the ratio perimeter/surface is higher for short devices and should improve the lateral heat dissipation (straightforward for devices surrounded by deep trench, the ratio area within the deep trench (heat dissipation) over emitter surface (heat source) is favourable to short devices)...
- It should be noticed that in technologies with deep trench, short devices also exhibits proportionally smaller R_{TH} value.
- The extracted ρ_{TH} value is validated on CBEBC devices, and the model fits the extracted R_{TH} values quite well

R_{TH} for multi-emitter devices (1)

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- Mono-emitter approach is adapted, multi-pyramidal resistance:



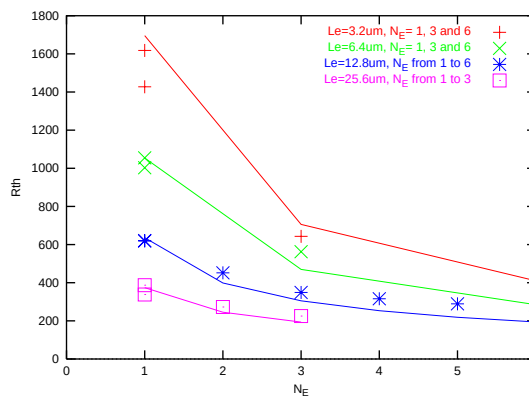
- Previous extracted ρ_{TH} value = 4.575.10-3m.K/W is used.

COMMENTS:

- Multi-emitter devices have multiple heat sources so the pyramidal approach is adapted.
- As described in Eq-3 the total R_{TH} is calculated as a sum of N_E small pyramids (R₁) in parallel, in series with a big one (R₂).
- R₁ and R₂ are calculated using the extracted ρ_{TH} value.

R_{TH} for multi-emitter devices (2)

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- Calculated values are optimistic for $N_E > 2$. The longer the device, the more R_{TH} is under-estimated.
- Interdigitated devices suffer from multiple heat source (leading to non-uniform emitter current).
- Long devices do not benefit from the 3D heat dissipation.

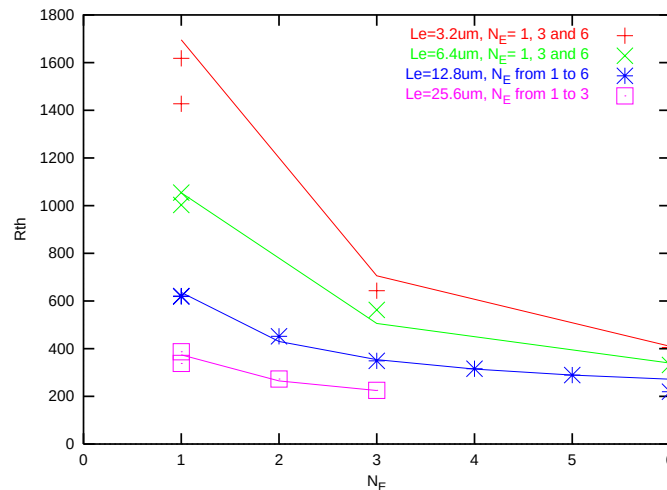
COMMENTS:

- The plot depicts R_{TH} values versus N_E (number of emitters) for several L_E (emitter lengths).
- On the plot, R_{TH} extracted values for multi-emitter devices are points whereas the model is drawn with lines.
- Globally the model is optimistic especially for great N_E. The longer the device is, the more R_{TH} is underestimated by the model.
- The first point could be explained: interdigitated devices have multiple heat source, so they heat more than a single-emitter device at the same bias conditions. In addition the temperature is not the same in each emitter finger (emitter fingers in the centre of the device heat more), and the current is not distributed identically in each finger.
- The second point could also be explained: short devices dissipate proportionally more than long ones.

R_{TH} for multi-emitter devices (3)

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- Empirical laws has been found: linear increase of R_{TH} with N_E (40% increase compared to multi-pyramidal model to for N_E=6), only activated for L_E>6μm:



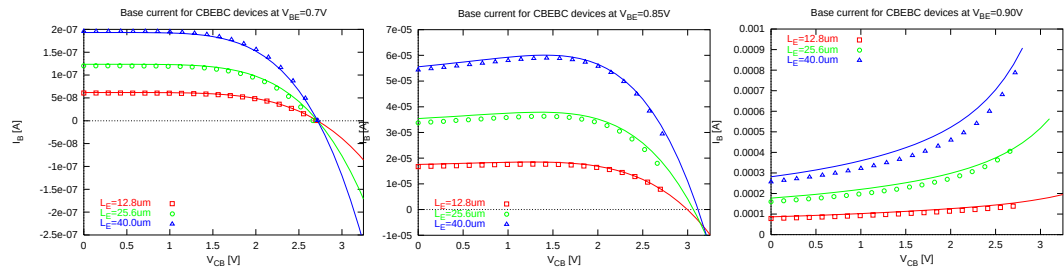
COMMENTS:

- As a compact modeling point of view, the discrepancies found for multi-emitter structures should be corrected.
- Empirical laws have been found to increase R_{TH} linearly with N_E compared to the pyramidal model prediction (40% increase for N_E=6) but only for devices with emitter long enough (L_E>6μm).
- With these additional laws the model fits the data very well.

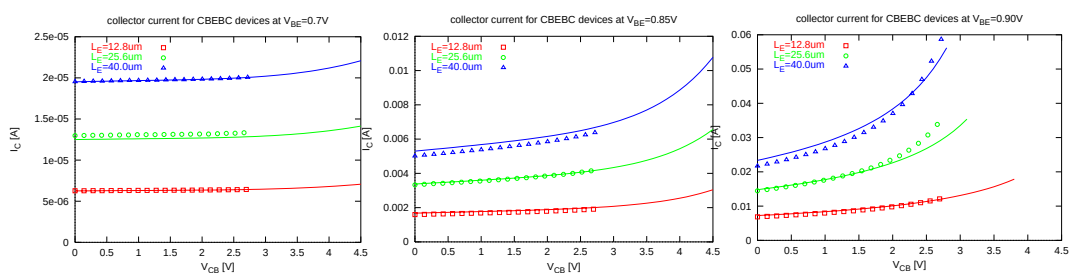
Electrical characteristics (1)

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□ I_B(V_{CB}) curves for 0.4μm×12.8μm, 25.6μm, 40.0μm CBECB devices:



□ I_C(V_{CB}) curves for 0.4μm×12.8μm, 25.6μm, 40.0μm CBECB devices:



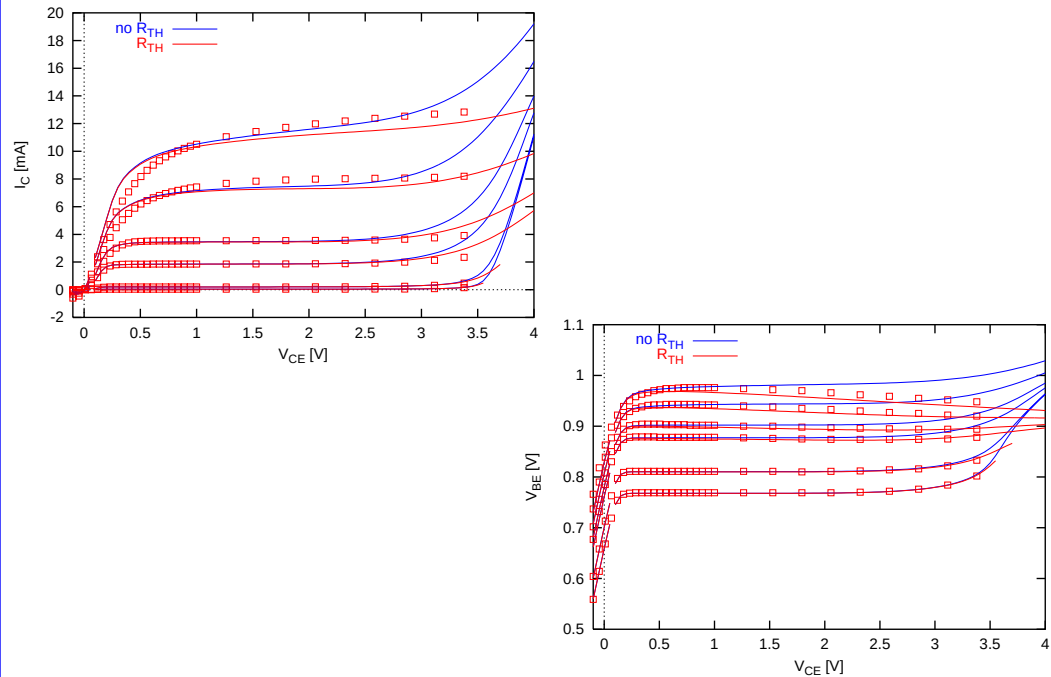
COMMENTS:

- The last part of the presentation depicts the main electrical characteristics impacted by the self-heating hence demonstrating the great interest of a R_{TH} scalable model even for a 'modest' performances technology.
- In the following plots measurement data are points whereas simulations with/without R_{TH} are drawn with lines.
- On these plots I_B(V_{CB}) and I_C(V_{CB}) curves are drawn for three V_{BE} values (0.7V=no self-heating, 0.85V=self-heating and avalanche takes over, 0.9V=self-heating and avalanche is pushed away) for L_E from 12.8μm to 40μm.
- The simulations (obviously including R_{TH} model) agree well with both I_C and I_B measured data.

Electrical characteristics (2)

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□ Output characteristics for a 0.4μm×6.4μm CBEBC device:



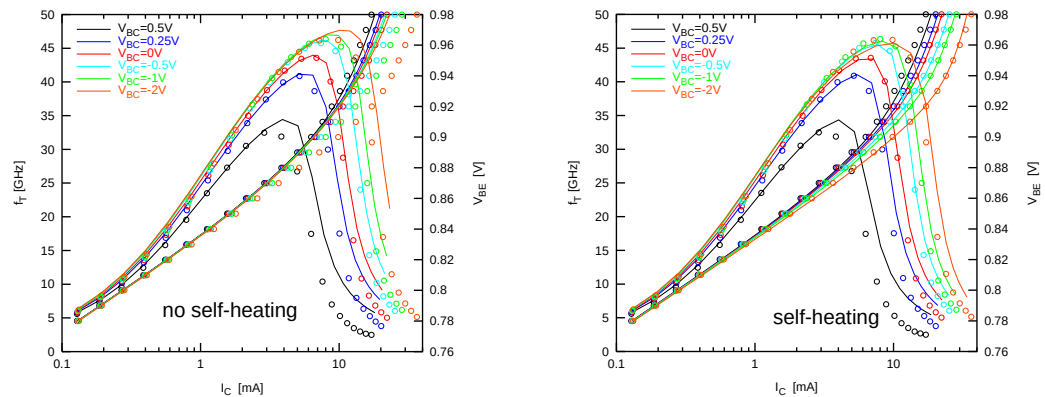
COMMENTS:

- On the first plot, the Output characteristics of a 0.4μm×6.4μm device are drawn for several I_B . The second plot depicts the measured V_{BE} versus V_{CE} for each I_B value.
- On the second plot the decrease of V_{BE} versus V_{CE} is typically due to self-heating. As long as the temperature increases with the thermal power (=with V_{CE}), I_B increases and the V_{BE} required to maintain a constant I_B , consequently decreases. Obviously the model without R_{TH} (in blue) fails to match this trend, whereas the R_{TH} model (in red) agrees well with the measured data.

Electrical characteristics (3)

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- $f_T(I_C)$ and $I_C(V_{BE})$ plots for a 0.4μm×12.8μm CBEBC at $V_{CB} = -0.5, -0.25, 0, 0.5, 1.0, 2.0V$:



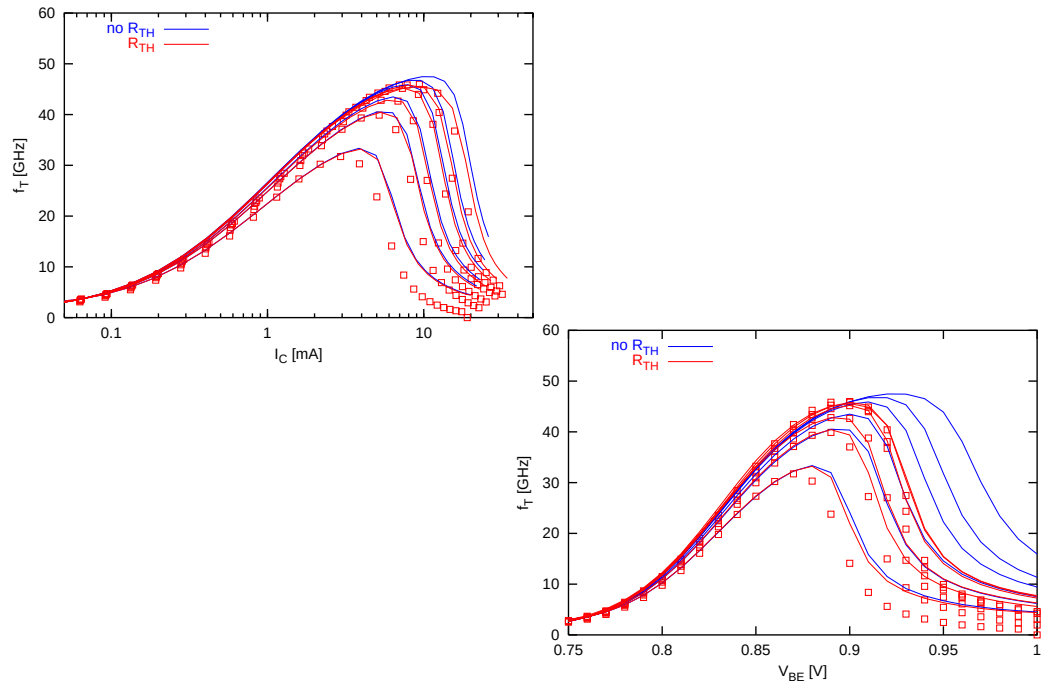
COMMENTS:

- On these two plots, both models are compared to measured $f_T(I_C)$ and $I_C(V_{BE})$ for several V_{CB} . The first plot depicts simulations coming from the model without R_{TH} whereas the second plot uses the model with R_{TH} .
- The high-injection transit time parameters of the HICUM scalable model have been extracted and optimized on the $f_T(I_C)$ characteristics. This explains the good agreement between the model without R_{TH} and the measurement points for $f_T(I_C)$. Concerning the $I_C(V_{BE})$ data points, the model without R_{TH} fails to match the data points especially for high V_{CB} where self-heating impact greatly the collector current.
- On the second plot, the model with R_{TH} modifies slightly the fit on the $f_T(I_C)$ characteristics but the main improvement comes from the accurate description of the $I_C(V_{BE})$ on the whole V_{CB} range.

Electrical characteristics (4)

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□ **f_T plots for a 0.4μm×12.8μm CEB at V_{CB}=-0.5, -0.25, 0, 0.5, 1.0, 2.0V:**



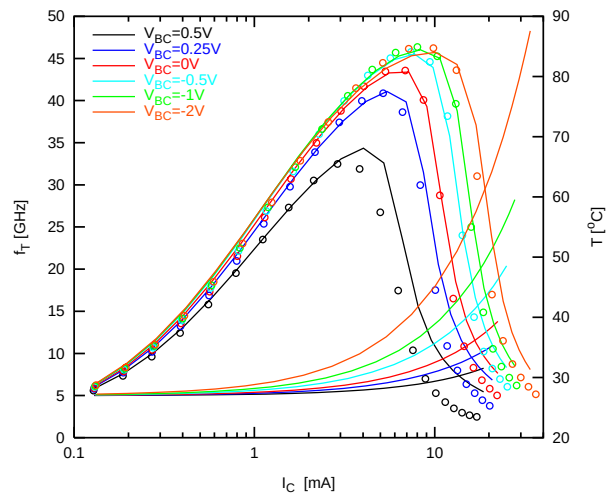
COMMENTS:

- On the first plot, both models (red=with R_{TH}, blue=without R_{TH}) are compared to measured $f_T(I_C)$. On the second plot, both models are compared to measured $f_T(V_{BE})$.
- Introducing the R_{TH} in the model slightly modifies the fit on the $f_T(I_C)$ curves, it lowers the maximum f_T for high V_{CB} (=2V). At such strong bias conditions the internal device temperature increases, so the f_T performance decreases.
- The main improvement of the R_{TH} is depicted on the second plot. As explained in the previous slide, the accurate description of the $I_C(V_{BE})$ allows an accurate description of the $f_T(V_{BE})$ on the whole V_{CB} range.

Electrical characteristics (5)

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- **f_T(I_C) plot for a 0.4μm×12.8μm CBEBC at V_{CB}=-0.5, -0.25, 0, 0.5, 1.0, 2.0V with simulated device temperature (R_{TH} included):**



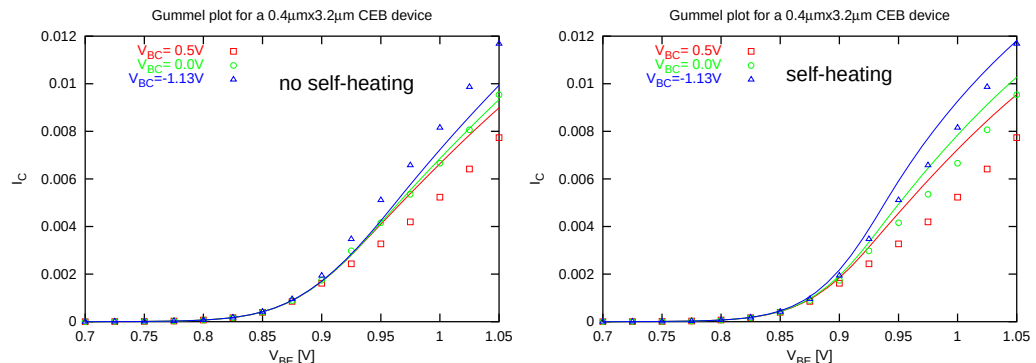
COMMENTS:

- The fifth HICUM node (=temperature) allows to collect the device internal temperature in the simulation.
- The plot depicts the f_T(I_C) curves of a 0.4μm×12.8μm devices as well as the device temperature given by the simulator. Obviously higher V_{CB} (=more thermal power dissipated in the device) gives higher device temperature.
- At peak f_T, the temperature increase could reach 20°C for the strongest V_{CB}. 50°C increase could be reached at higher current than the peak f_T currents.

Electrical characteristics (6)

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□ I_C (V_{BE}) for a 0.4μm×3.2μm CEB device:



□ R_{TH} allows an accurate description of I_C and I_B variation with V_{BC} at high V_{BE}, but R_E value (effective extracted value, including self-heating effect) is now wrong.

COMMENTS:

- On these two plots, both models are compared to measured I_C(V_{BE}) in linear scale. The first plot depicts simulations coming from the model without R_{TH} whereas the second plot uses the model with R_{TH}.
- These plots underline that some parameters should be re-extracted or re-optimized after the introduction of the R_{TH}. Actually the extraction of the HICUM scalable model has been done without taking into account the R_{TH} model, so some parameters (like the emitter resistance) are 'effective' i.e. they include the self-heating impact.

CONCLUSION

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- **Scaleable R_{TH} model feasibility demonstrated!**
- **Many room for improvement:**
 - R_{TH} extracted on top of the parameter extraction flow, need to take into account during the flow?
 - Self-heating non-uniform for interdigitated device, in depth analysis required.
 - Improve the scalable model for small devices.
 - Self-heating variation in temperature?
 - R_{TH} scalable model for state-of-art technologies with deep trench?

COMMENTS:

- The feasibility of a scalable (in L_E and W_E and for multi-emitter devices) R_{TH} model has been demonstrated.
- There are still many rooms for improvement, should the self-heating be extracted at the end of the extraction flow or sooner, the general thermal behaviour of interdigitated devices has been understood but in-depth analysis is needed, the behaviour of short devices should be studied in detail, the model behaviour (with R_{TH}) should be checked in temperature, and finally the R_{TH} modeling work has to be done on a 'state-of-the-art' technology with deep trench.