HICUM Status Overview

M. Schröter

Chair for Electron Devices and Integrated Circuits
(CEDIC)
University of Technology Dresden
Germany

Dept. of Electrical and Computer Engin.
Wireless Communications Center
University of California at San Diego
USA

mschroter@ieee.org
http://www.iee.et.tu-dresden.de/iee/eb/eb_homee.html

Outline

- Availability of version 2.1 (simulators, foundries)
- HICUM/Level2 Version 2.2
- Model release notes
- Development effort
- Model verification

Availability of HICUM/Level2 V2.1 in Circuit Simulators

(Please contact simulator vendor for details and the latest status of availability)

simulator	*first release*	*latest release*	*comments*
ELDO-RF	**10/99**	**7/03**	ELDO AMS2004.1; ext. thermal node; Harm. Balance
SPECTRE-RF	**10/99**	**?/03**	version > 446.100.70 with HICUM2.1
ADS	**7/00**	**5/03**	ADS2003C: design tested stable version
Smart-SPICE	**11/00**	**11/00**	can be combined with UTMOST
MicrowaveOffice	**2003**	**04/04**	numerically stable; contains also HICUM/Level0
APLAC	**10/01**	**6/03**	APLAC 7.62a
HSPICE	**2/01**	**2/02**	working on stable release in conjunction with MWO
TEKSPICE	**8/02**	**8/02**	various proprietary numerical improvements
Xpedion	**?/03**	**?/03**	(available according to customers)
SPICE3F5	**4/02**	**4/02**	one of the reference circuit simulators

Apache NSpice, HSIM: code sent as per request, implementation in progress

- Various (other) in-house simulators (ASX (IBM), ...)
- Verilog-A version of model code; also, stand-alone kit enabling coupling with other tools

Availability of HICUM/Level2 V2.1 Foundry Libraries

(Please contact foundry for details and the latest status of availability)

foundry	*process name*	*process type*	*released*	*comments*
Atmel	UHF6(S)	20GHz Si bipolar	/	TRADICA[1], lv&hv[2]
	SIGE1	40GHz SiGe bipolar	?/02	TRADICA , lv&hv
		50GHz 0.35µ SiGe BiCMOS	?/04	TRADICA , lv&hv
	SIGE2	90GHz SiGe bipolar	?/04	TRADICA
IBM	7HP	120GHz SiGe BiCMOS	?/?	lv&hv&mp
	8HP	210GHz SiGe BiCMOS	?/?	lv&hv&mp
JazzSemi	BC35	35GHz 0.35µ Si BiCMOS	7/98	TRADICA[1], lv&hv
	SBC35	60GHz 0.35µ SiGe BiCMOS	3/99	TRADICA, lv&hv&mp
	SBC18	150GHz 0.18µ SiGeBiCMOS	10/00	TRADICA, lv&hv&mp
ST	confidential	45GHz SiGe BiCMOS	yes	lv&hv
	confidential	60GHz SiGe BiCMOS	yes	lv&hv
	confidential	150GHz SiGe BiCMOS	yes	lv
TSMC	SG035	50GHz 0.35µ SiGe BiCMOS	?/04	TRADICA[1], lv&hv&mp
??				

[1] indicates geometry scalable TRADICA-generated libraries

[2] lv = low-voltage (high-speed) npn, hv = high-voltage npn, mp = medium-speed (special purpose) npn

HICUM version 2.2

- physics-based extensions
  - background
  - open for discussion

- numerics/implementation related
  - mostly recommendations

- documentation
  - release notes with detailed documentation of changes/additions
  - model description update
    (detailed derivation in model description is not desired by most users)

Note: information below is a first draft for discussion (missing various details)

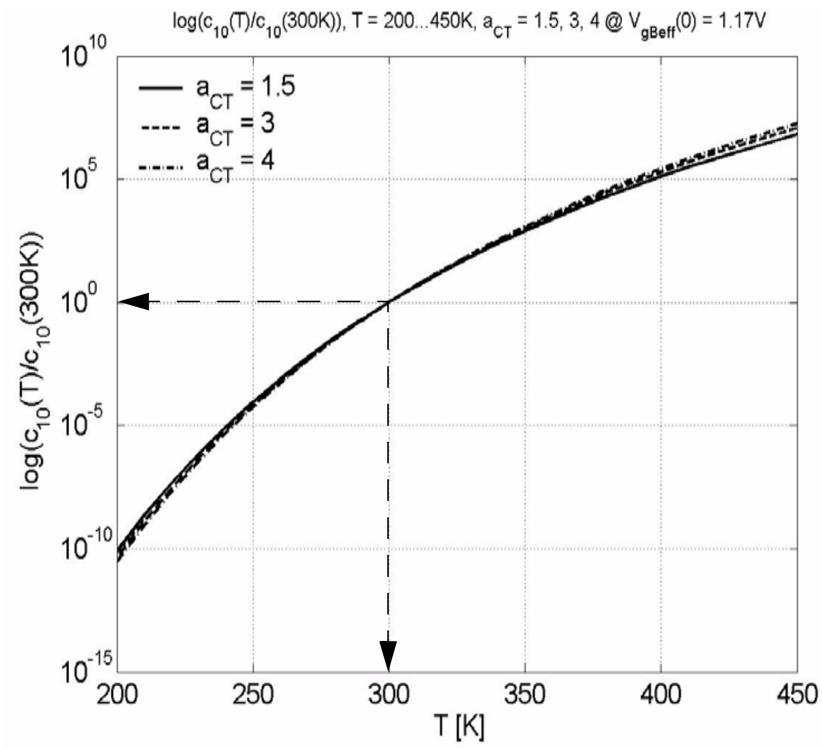
=> still subject to change until official release of version 2.2

Transfer current and GICCR

- generalized formulation for temperature dependent ICCR factor (requested by some users)

$$c_{10}(T) = c_{10}(T_0)\left(\frac{T}{T_0}\right)^{a_{CT}}\exp\left[\frac{V_{gBeff}(0)}{V_{T0}}\left(1-\frac{T_0}{T}\right)\right],$$

  requiring the new model parameter a_{CT}



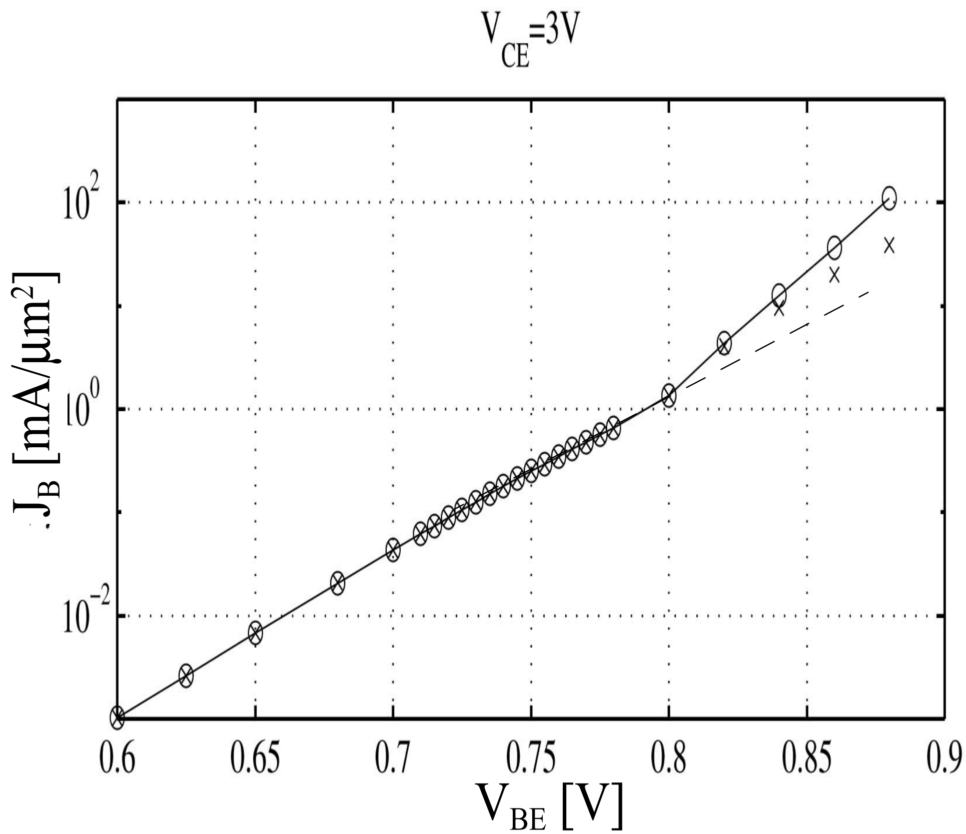
- plot shows normalized c_{10} vs temperature at $V_{gBeff}(0)$ = 1.17V for a_{CT} variation
  => little impact
  => easily compensated for in practice by $V_{gBeff}(0)$

- zero bias hole charge temperature dependence
  - two options are still being investigated (based on device simulation results)

- base region reach-through: limitation of $Q_{p,j} = Q_{p0} + h_{jEi}Q_{jEi} + h_{jCi}Q_{jCi}$ at high reverse biased junctions by hyperbolic smoothing function $Q_{p,low} = Q_{B,rt}\left(1+\frac{x+\sqrt{x^2+a}}{2}\right)$ with $x = \frac{Q_{p,j}}{Q_{B,rt}} - 1$

Base current components

Excess base current at high current densities from recombination at the BC barrier



- high forward bias
  - ⇒ field at BC junction decreases
  - ⇒ pile-up of holes “before” the Ge drop)
  - ⇒ formation of dipole layer
  - ⇒ i.e. conduction band barrier
  - ⇒ pile-up of electrons
  - ⇒ increased recombination
  - ⇒ increased base current
- observable in 1D case (no r_{series})
- add’l current: $\Delta I_{Bhb} = \dfrac{\Delta Q_{fB}}{\tau_{Bhb}}$
- 2D case: masked by series resistances
  ⇒ difficulty for extracting parameter τ_{Bhb}

Note: onset of high-current effects ⇒ keep using I_{CK}

Base current components (cont'd)

- Temperature dependence: more general equation

$$I_{BEiS}(T) = I_{BEiS}(T_0)\left(\frac{T}{T_0}\right)^{a_{BEi}} \exp\left[\frac{V_{gEeff}(0)}{V_{T0}}\left(1-\frac{T_0}{T}\right)\right]$$

with $a_{BEi} = \frac{m_{Cf}(a_{CT} + \alpha_Q T_0)}{m_{BEi}}$ and additional parameter $V_{gEeff}(0) = \frac{m_{Cf} V_{gBeff}(0)}{m_{BEi}} - \alpha_{Bf} T\, V_{T0}$

  - note: calculating V_{gEeff} from above equation corresponds to using current gain TC (as in V2.1)

- BC component => modified temperature dependence

$$I_{BCiS}(T) = I_{BCiS}(T_0)\left(\frac{T}{T_0}\right)^{a_{BCi}} \exp\left[\frac{V_{gCeff}(0)}{V_T}\left(\frac{T}{T_0}-1\right)\right]$$

with $a_{BCi} \approx 4 - \zeta_{Ci}$ and $V_{gCeff}(0) \approx V_{gBeff}(0)$ (no new parameters)

- similar modifications for I_{BEp}, I_{BCx}

Depletion capacitances and charges

- exponential smoothing can cause numerical overflow for large forward or reverse bias

=> replaced exponential by *hyperbolic* smoothing

(changes presented below apply to all depletion charges and capacitance formulations)

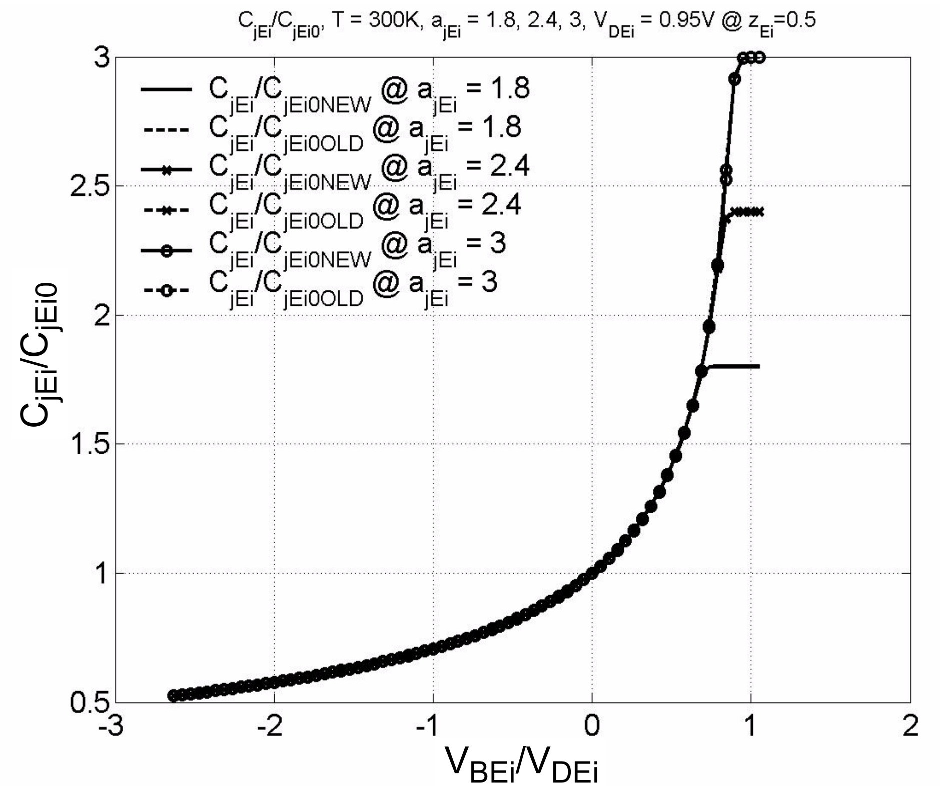
- internal base-emitter component (forward bias smoothing only)

  - auxiliary (smoothed) voltage

$$v_j = V_f - V_T \frac{x + \sqrt{x^2 + a_{fjE}}}{2} < V_f$$

with $x = \dfrac{V_f - v_{B'E'}}{V_T}$

  - constant $a_{fjE} = 4\, ln^2(2) = 1.921812$: adjusted to minimize difference to v2.1 formulation
(a$_{fjE}$ is not a model parameter)



Depletion capacitances and charges (cont'd)

- internal base-collector component
  - common argument $y = \frac{V_{DCi} - V_{B'C'}}{V_{PTCi}}$ with smoothing function $f_{jC,f} = \frac{y + \sqrt{y^2 + a}}{2}$ for forward bias
  - reverse bias: argument $x = 1 - f_{jC,f}$ and smoothing functions $f_{jC,pd} = 1 - \frac{x + \sqrt{x^2 + a_{pd}}}{2}$ (partial depl.) ,

$$f_{jC,PT} = 1 - \frac{x - \sqrt{x^2 + a_{pd}}}{2} \text{ (punch-through)}$$

=> replace voltages in charge expression, $Q_{jCi} = Q_{jCi,pd} + Q_{jCi,PT}$, by smoothing functions:

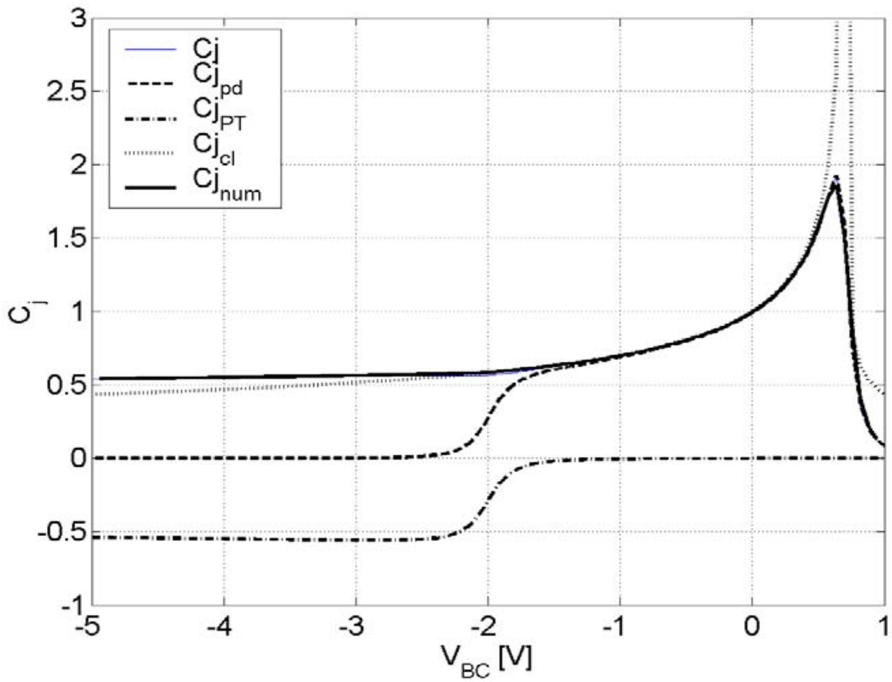
$$Q_{jCi,pd} = \frac{C_{jCiPT} V_{PTCi}}{1 - z_{Ci}} \left[\left(\frac{V_{DCi}}{V_{PTCi}} \right)^{1 - z_{Ci}} - f_{jC,pd}^{1 - z_{Ci}} \right] \quad , \quad Q_{jCi,PT} = \frac{C_{jCiPT} V_{PTCi}}{1 - z_{Cir}} \left[1 - f_{jC,PT}^{1 - z_{Cir}} \right]$$

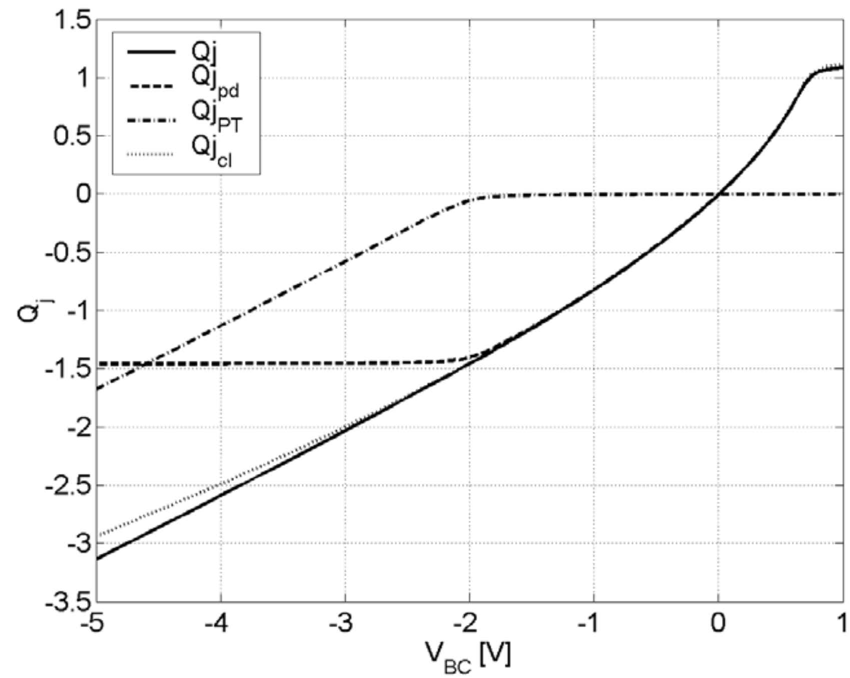
=> derivative yields depletion capacitance

$$C_{jCi} = \frac{C_{jCiPT}}{\sqrt{x^2 + a_{pd}}} \frac{f_{jC,f}}{\sqrt{y^2 + a_{Cf}}} \left(\frac{1 - f_{jC,pd}}{f_{jC,pd}^{z_{Ci}}} - \frac{1 - f_{jC,PT}}{f_{jC,PT}^{z_{Cir}}} \right)$$

BC depletion capacitance (cont'd)

normalized BC charge Q_j and capacitance C_j, and their components





pd = partial depletion PT = punch-through cl = classical (text book) expression num = numericxal derivative for verification

- punch-through and forward bias limiting included, compatible for version 2.1
- strongly simplified (and easier to understand) and numerically more suitable than version 2.1
- note: no impact on existing low-current transit time formulation (see later)

Depletion capacitances and charges (cont'd)

temperature dependence of built-in voltage

- smoothing towards high temperatures to avoid negative built-in voltage

  - auxiliary voltage at T_0 (with $V_{T0} = k_B T_0/q$):

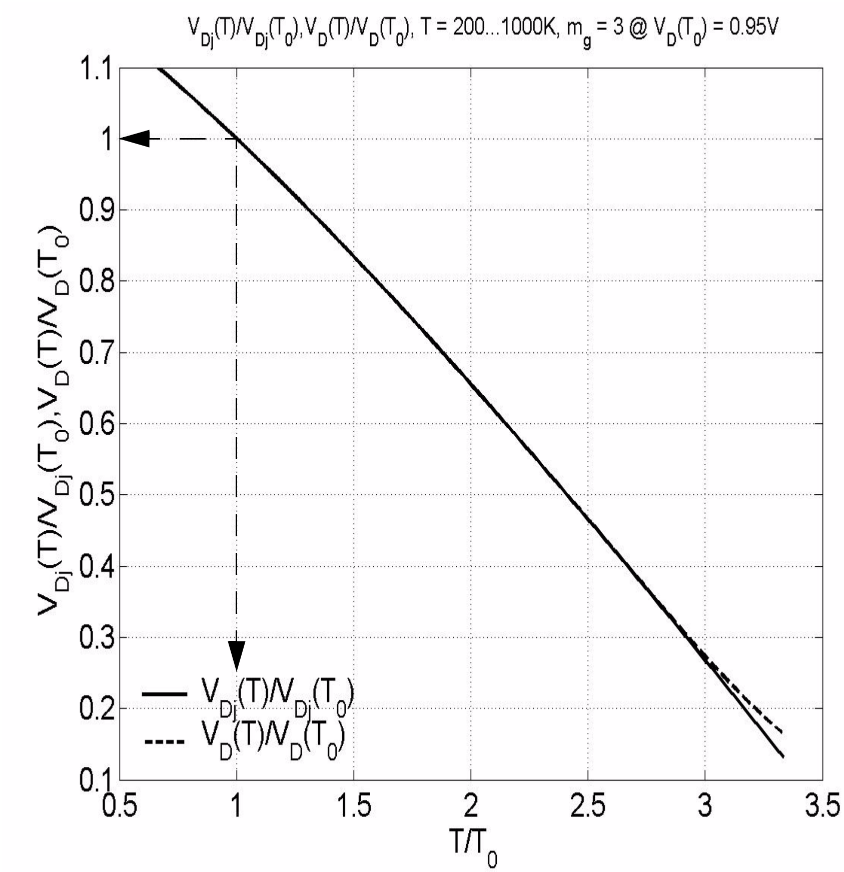
$$V_{Dj}(T_0) = 2V_{T0}\ln\left[\exp\left(\frac{V_D(T_0)}{2V_{T0}}\right) - \exp\left(-\frac{V_D(T_0)}{2V_{T0}}\right)\right]$$

  - auxiliary voltage at T:

$$V_{Dj}(T) = V_{Dj}(T_0)\left(\frac{T}{T_0}\right) + V_g\left(1 - \frac{T}{T_0}\right) - m_g V_T \ln\left(\frac{T}{T_0}\right)$$

  - final smoothed value at T:

$$V_D(T) = V_{Dj}(T) + 2V_T\ln\left(\frac{1}{2}\left[1 + \sqrt{1 + 4\exp\left(-\frac{V_{Dj}(T)}{V_T}\right)}\right]\right)$$



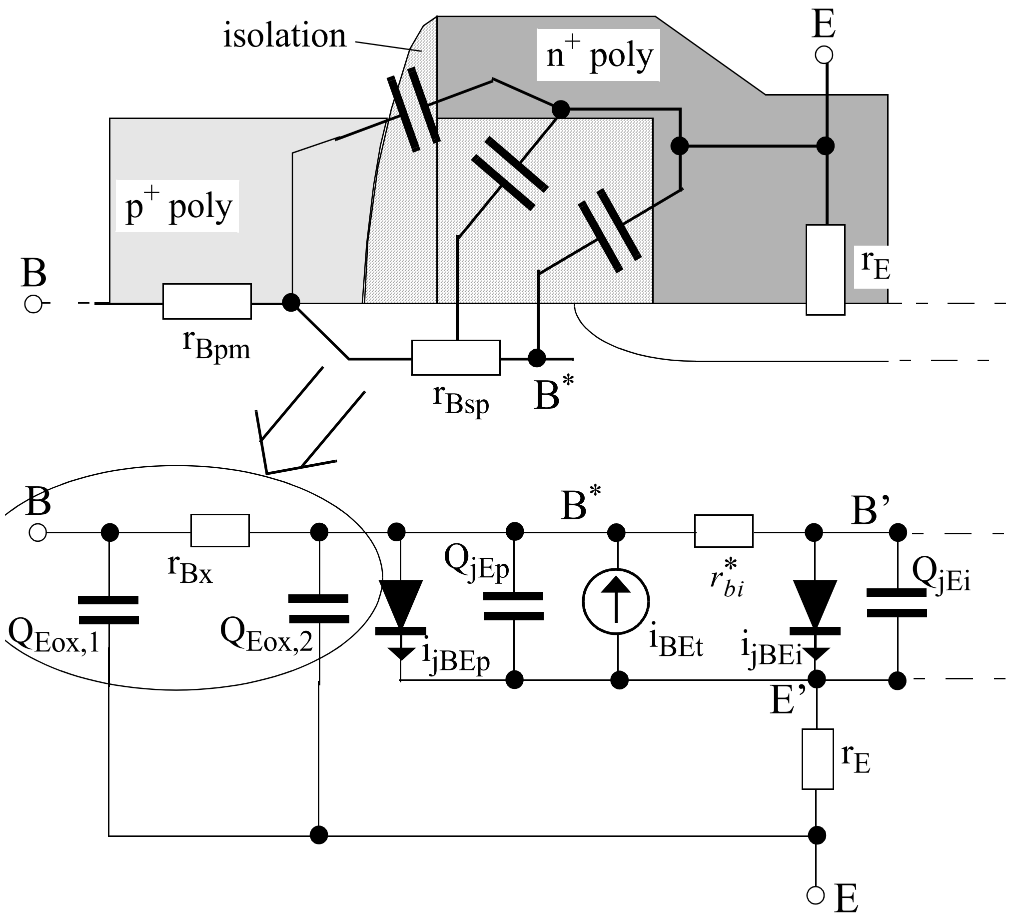
Transit time

- effective collector voltage
  - hyperbolic smoothing: $v_{ceff} = V_T\left[1 + \frac{u + \sqrt{u^2 + a_{vceff}}}{2}\right]$ with $u = \frac{v_c - V_T}{V_T}$ and a_{vceff} (= 1.921812)
- numerical derivative of I_{CK} has been replaced by analytical derivative
- temperature dependence of V_{lim}
  - replacing former term $1 - \alpha_{vs}\Delta T \approx \left(\frac{T}{T_0}\right)^{-a_{vs}}$ => smooth expression $V_{lim,T} = V_{lim}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{Ci} - a_{vs}}$
- Emitter transit time
  - smooth new physics-based expression: $\tau_{Ef0}(T) \cong \tau_{Ef0}(T_0)\left(\frac{T}{T_0}\right)^{a_{\tau Ef}} \exp\left[-\frac{\Delta V_{geff}(0)}{V_T}\left(\frac{T}{T_0} - 1\right)\right]$

  with $\Delta V_{geff}(0) = V_{gBeff}(0) - V_{gEeff}(0)$, $V_{gEeff}(0) = \frac{m_{Cf}V_{gBeff}(0)}{m_{BEi}} - \alpha_{Bf}T\ V_{T0}$ (see I_{BEiS})

  and $a_{\tau Ef} = a_{BEi} - a_{CT} - 0.5$, $a_{BEi} = 3.5$

Parasitic BE capacitance



- distributed capacitance mostly along link (spacer) region and associated series resistance r_{Bsp}
- need simple lumped representation best first order approach:

  π equivalent circuit

  => partitioning across r_{Bsp}
- new parameter for partitioning

$$f_{CEox} = \frac{C_{Eox,\,1}}{C_{Eox}}$$

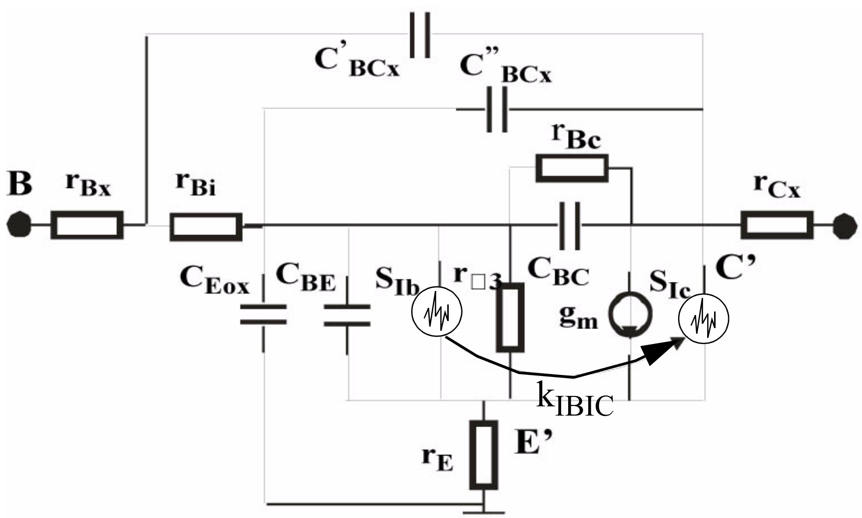
- can also be used to include metal cap:

$$f_{CEox} = \frac{C_{Eox,\,1} + C_{BE,\,metal}}{C_{Eox} + C_{BE,\,metal}}$$

Recommendations for improvements

... directly related to the simulator implementation & features (rather than model equations)

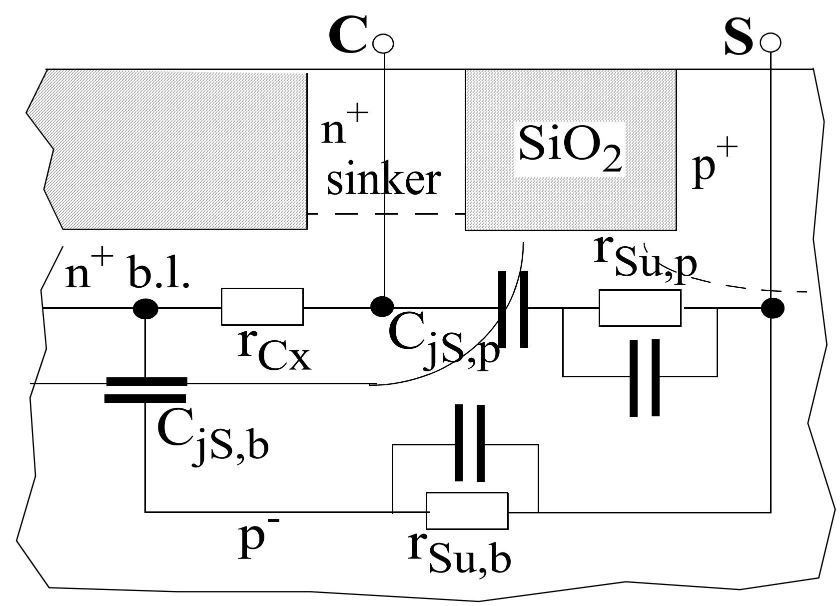
- model parameters (and associated calculations)
  - should be *available* (already in V2.1): MCF, HJEI, IS (alternative to C10), ZETACX
  - new parameters in V2.2: HFE, HFC, ALCT, VGE, ALCB, KIBIC
  - should be *deleted*: KRBI
  - *flags* for turning on/off: self-heating, vertical NQS effects
- separate thermal node
  - available already in some simulators (ADS, ELDO, ...) => should now be a standard feature
- noise correlation factor



- indicated by theoretical considerations, although detailed physics and related modeling are still being debated
- indicated by measurements (more for III-V HBTs, but also for SiGe HBTs)
- implementation issues for Harmonic Balance and Period Steady-State analysis are unknown
- how to include in Verilog reference code ?
- not included in stand-alone solver

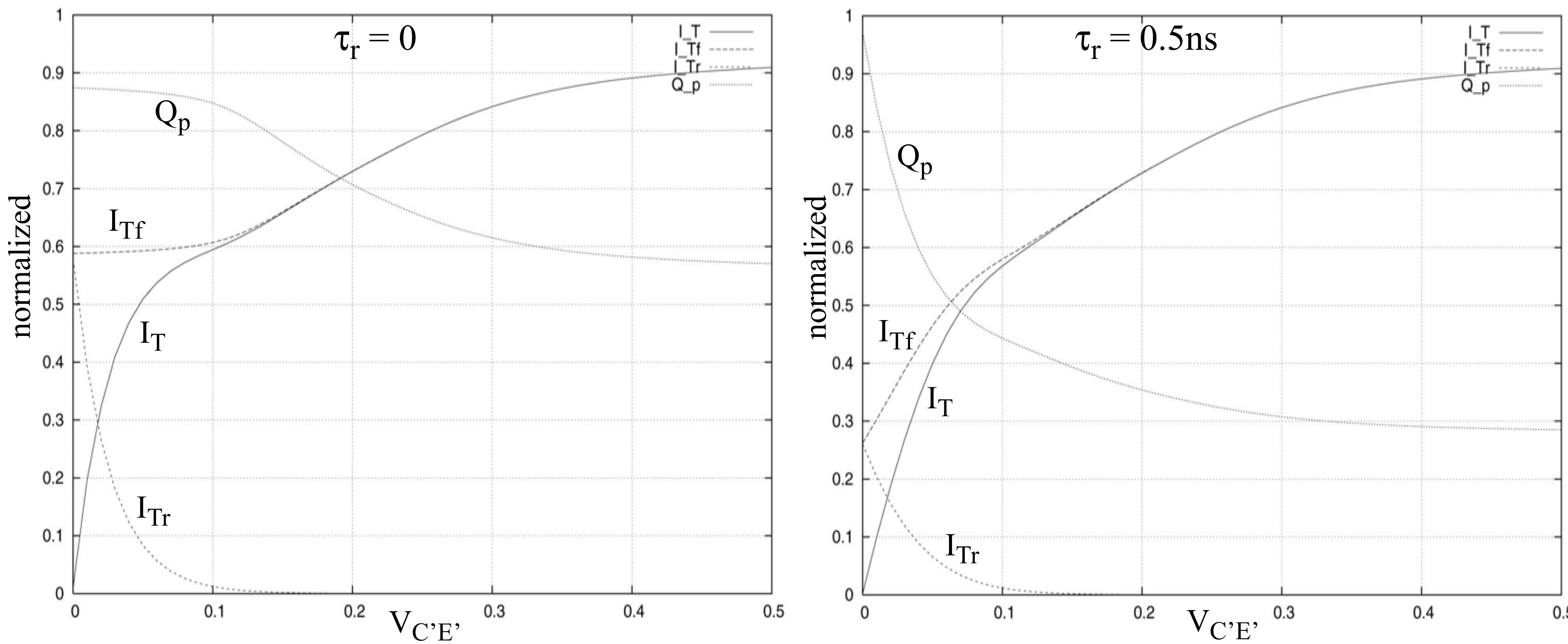
FAQs

- convergence issues in (production) circuits - possible causes
  - simulator implementation or type of analysis (e.g., PSS analysis has been generally difficult to run)
  - device operation at too high current densities => simulator indicates biasing issue in circuit (there were at least two known production design cases in the past 6 months)
  - device operation at too high power => simulator indicates device destruction
  - voltage (change) limitation schemes: extremely important but different from simulator to simulator (e.g.: generally needs to be included also in Verilog-A code to secure reliable convergence)
- substrate capacitance and substrate coupling network
  - electrically distributed (especially for large structures)
  - substrate depletion cap is coupled with substrate network
  - several variations (STI, DTI, substrate contact location...) depending on process
    => fixed topology implemented in compact model would limit application
    => add separately as needed via subcircuit
  - suggested improvement beyond existing single elements => shown in figure on the right



FAQs (cont'd)

- kink in IC-VCE characteristics ... a 1D case study
  - $\tau_f = \tau_{f0}(VB'C') + \Delta\tau_f$, output characteristics @ $V_{B'E'} = 0.9V$

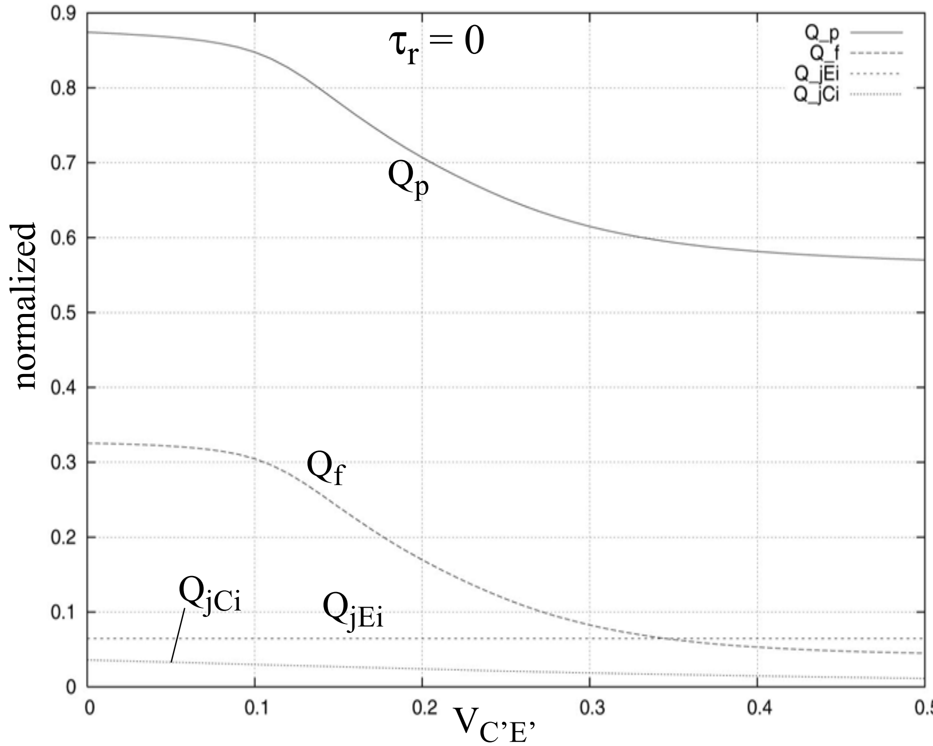


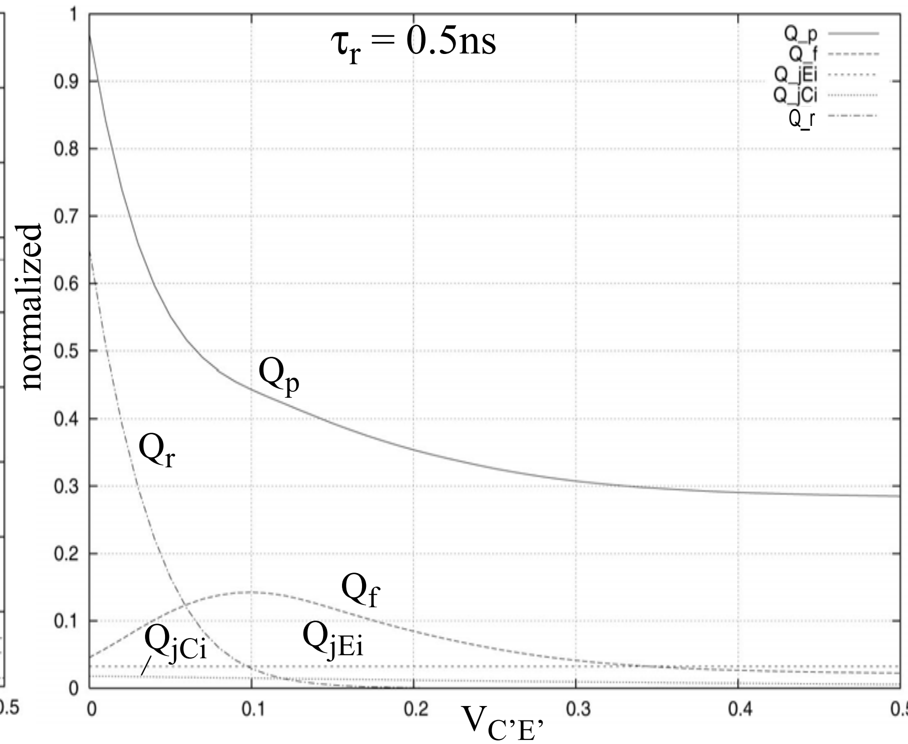
  - for $\tau_r = 0$ => Q_p and I_{Tf} flatten towards $V_{C'E'} \to 0$ => kink at hard saturation
  - effect is independent of BC capacitance and charge, e.g., in $\tau_{f0}(VB'C')$

FAQs (cont'd)

... explanation of possible kink in IC-VCE characteristics

- charges





=> kink is caused by ***minority*** charge calculation towards $V_{C'E'} \rightarrow 0$

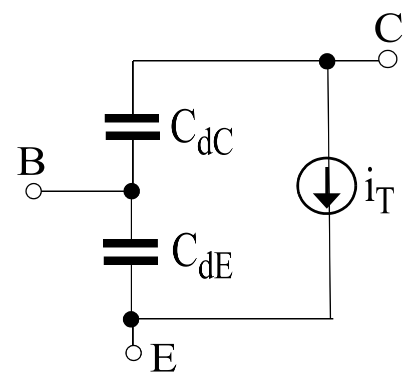
- however: complete neglection of Q_r at hard-saturation is non-physical

=> need to develop extended charge description for hard-saturation

FAQs (cont'd)

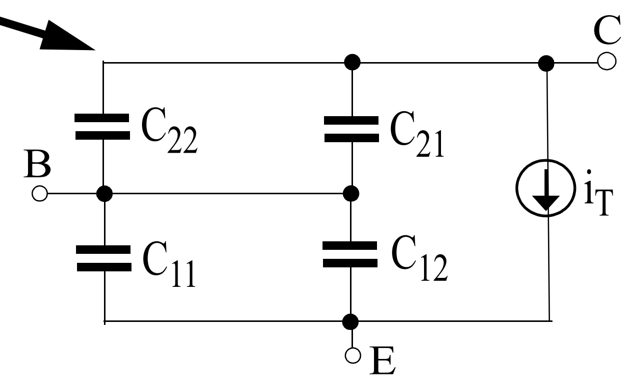
- "BC" minority charge (Q_{dC}) and capacitance (C_{dC})
  - total minority charge under quasi-static condition is (integration) path independent

$$dQ_m = dQ_f + dQ_r = \left.\frac{\partial Q_m}{\partial V_{B'E'}}\right|_{V_{B'C'}} dV_{B'E'} + \left.\frac{\partial Q_m}{\partial V_{B'C'}}\right|_{V_{B'E'}} dV_{B'C'} = C_{dE} dV_{B'E'} + C_{dC} dV_{B'C'}$$



  - a common misconception is to assume the r.h.s. equivalent circuit for C_{dE} and C_{dC}
  - correct approach: solve the time dependent continuity equation => transient ICCR (TICCR [Klose & Wieder 1987]); e.g.:

$$\Delta i_C(t) = qA_E \int_0^{x_C} F_C(x, t) \frac{\partial n}{\partial t} dx$$



$$F_C = \frac{\int_0^{x_C} h(\xi, t) p(\xi, t) d\xi}{\int_0^{x_C} h(x, t) p(x, t) dx} \quad , \quad h(\xi, t) = \exp\left(\frac{v_{B'E'} - \varphi_p}{V_T}\right) \frac{1}{\mu_n n_i^2} \frac{|j_{nx}| A_E}{i_T}$$

  - C_{11}...C_{11} are "self"- and transcapacitances defined by Δi_C, Δi_E (notice the complicated equations!!)

Model release notes

- Version 2.2 release: simulators
  - Verilog-A
  - stand-alone solver HICUMNA: depending on funding from CMC/others
  - DEVICE: only for CEDIC cooperation partners

- ... and test cases
  - only standard analysis possible: DC, AC, temperature, transient (limited extent)
  - noise is not included in stand-alone solver; implementation unknown yet in Verilog-A

Notes:

- implementation
  - demand for model support exceeds CEDIC resources (see separate slides)
  - effort and cost for commercial implementation can be as large as for development

Model development effort

Outline

- intrinsic transistor
- external transistor
- parasitic effects
- statistical modeling
- model parameter determination

mostly covered by TRADICA development

Model development - intrinsic transistor

Overview

- improved physics-based collector model for S/DHBTs
  (incl. high-current and barrier effects, avalanche, current dependent BC cap, hard saturation)
  - SiGe HBTs with advanced conventional doping profile
  - Low-Emitter Concentration (LEC) SiGe HBTs
- 3D GICCR theory and application to compact model element definition
- charge partitioning schemes in S/DHBTs
- high-frequency noise component decomposition
- high-frequency (single- and multi-tone) distortion
- III-V HBTs (AlGaAs, InGaAs, InP)
  - non-local transport => impact on transit time and transit frequency
  - geometry scaling

Modeling the bias dependent field at the BC junction

- main assumptions: $N_{Ci}(x)$ = const, $v_n = v_s$ $\Rightarrow$ integration of Poisson equation yields for

low voltages (partial depletion)

$$E_{jc} = E_{wc} + \sqrt{\frac{2qN_{Ci}}{\varepsilon}}\sqrt{\left(1-\frac{I_{Tf}}{I_{lim}}\right)(v_{ceff} - E_{wc}w_{Ci})}$$

with $$E_{wc} = \rho_{Ci}\frac{I_{Tf}}{A_E} = \frac{I_{Tf}}{qA_E\mu_{nCi}(E_{wc})N_{Ci}}$$

high voltages (full depletion)

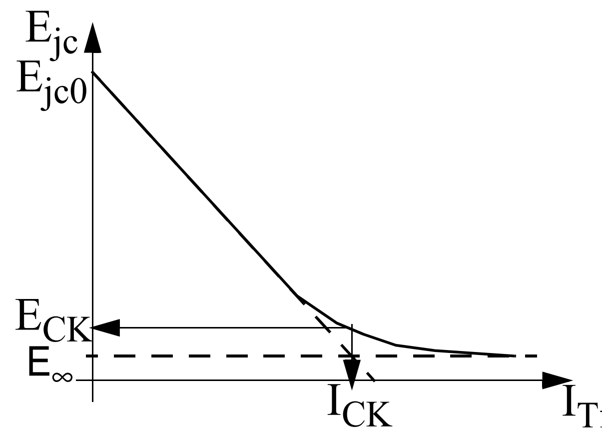
$$E_{jc} = \frac{v_{ceff} + V_{PT0}(1 - I_{Tf}/I_{lim})}{w_{Ci}}$$

with $$V_{PT0} = \frac{qN_{Ci}}{2\varepsilon}w_{Ci}^2$$

- issues with above equations:
  - limited validity range: $v_{ceff} > E_{wc}w_{Ci}$ (@ low voltages); $I_{Tf} = I_C < I_{lim} = qN_{Ci}v_sA_E$ (@ high voltages)
  - difficult to extend numerically stable beyond I_{lim} (and I_{CK}) into high-current range

- proposed approach here:
  - linear I_{Tf} dependence at low current
  - level off toward high currents

  smooth in between
  - smoothing function depends on key "parameters" E_{jc0}, I_{CK}, E_∞



Modeling the bias dependent field at the BC junction

comparison between device simulation and analytical equation

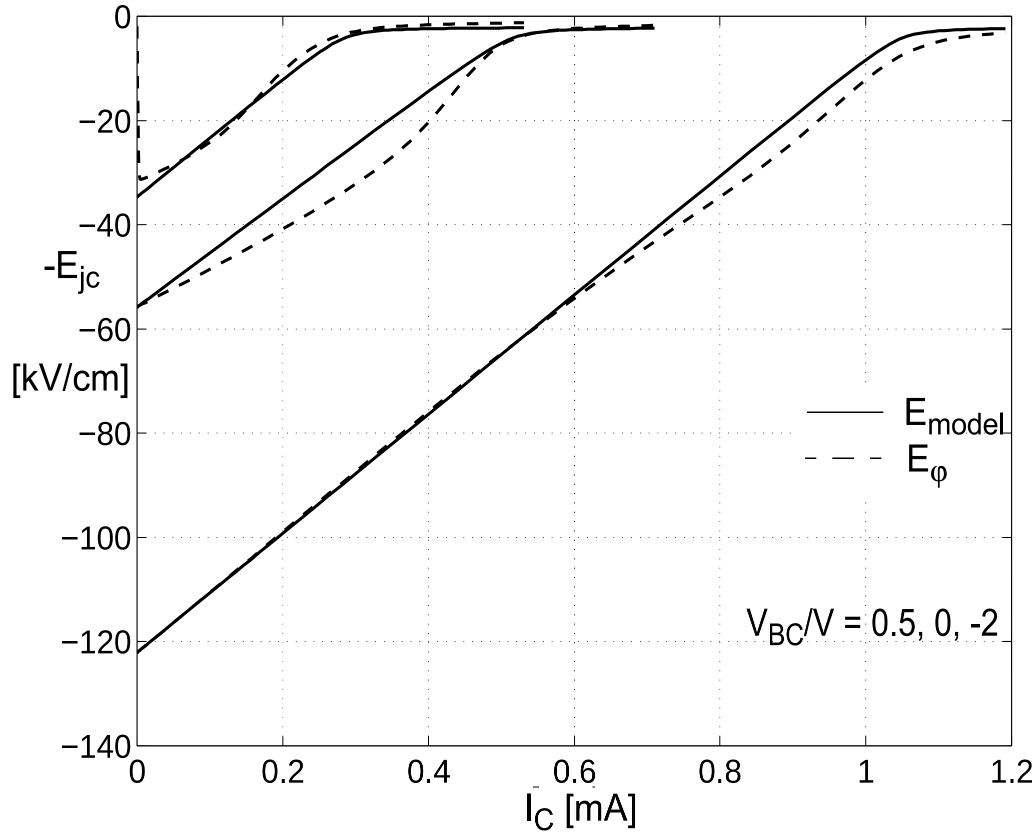
- model equation: $E_{jc} = E_{\infty} + f_e E_{lim}$

  with

$$f_e(V_{BC}, I_{Tf}) = \frac{e_j + \sqrt{e_j^2 + g_{jc}\frac{E_{CK}}{E_{lim}}}}{2},$$

$$e_j = \frac{(E_{jC0} - E_{\infty}) - (E_{jC0} - E_{CK})\frac{I_{Tf}}{I_{CK}}}{E_{lim}}$$

- parameter: g_{jc} (all other parameters are already available in HICUM)
- deviation at low V_{BC}: missing square root dependence



$\Rightarrow$ impact on model variables: see next slides

Base-collector charge and depletion capacitance

- incremental charge in BC region for quasi-static operation (path independent integral):

$$dQ_{BC}(V_{BC}, I_{Tf}) = C_{jCi}\, dV_{BC} + \tau_{BC}\, dI_{Tf}$$

- BC depletion capacitance is a function of voltage and current

$$C_{jCi}(V_{BC}, I_{Tf}) = \left.\frac{\partial Q_{BC}}{\partial V_{BC}}\right|_{I_{Tf}}$$

- relation to electric field via Gauss' law:

$$Q_{BC}(V_{BC}, I_{Tf}) = \varepsilon E_{jc}(V_{BC}, I_{Tf})$$

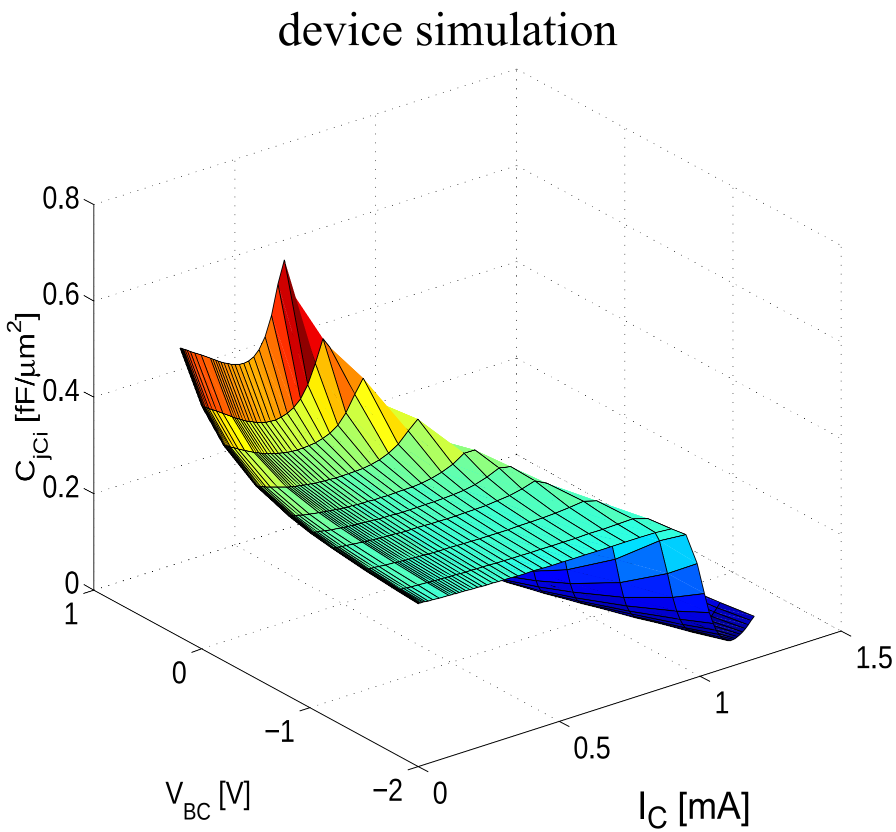
- model accuracy is maintained by describing E_{jc0} through measurable $C_{jCi}(V_{BC},0)$
- current dependence: include voltage drop across non-depleted collector (ohmic region)

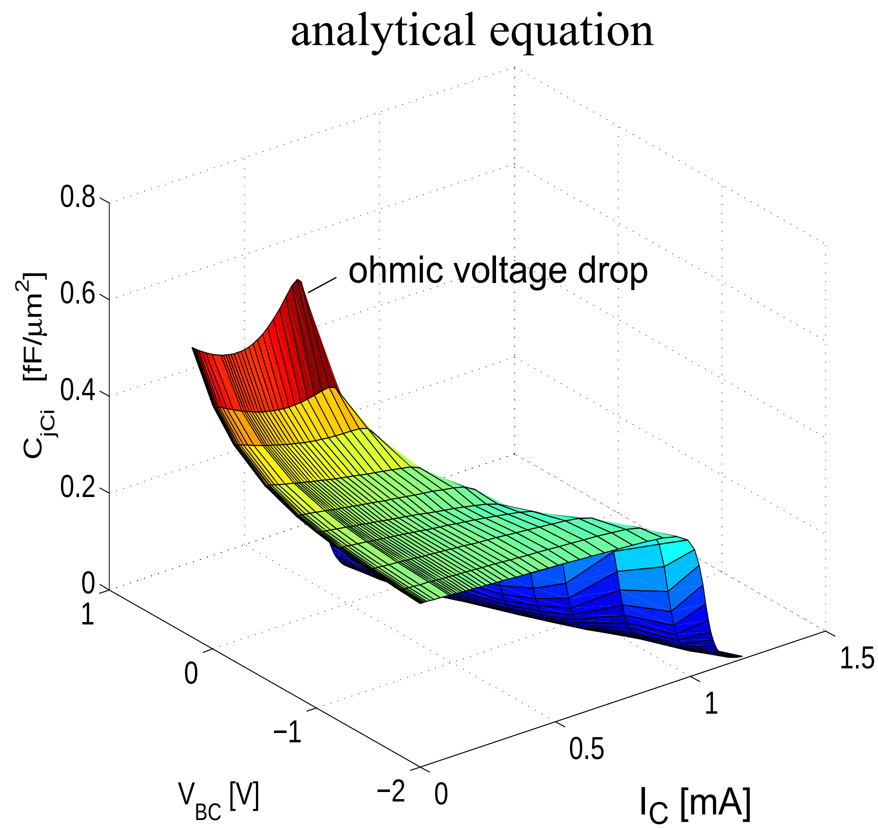
$\Rightarrow$ roughly approximated by $\Delta V_{pd} = V_{lim}\frac{I_{Tf}}{I_{lim}}\left(1 + \frac{I_{Tf}}{I_{lim}}\right)$

$\Rightarrow$ replace V_{BC} by $V_{BC} + \Delta V_{pd}$

$\Rightarrow$ retains explicit formulation

Current and voltage dependent results: comparison



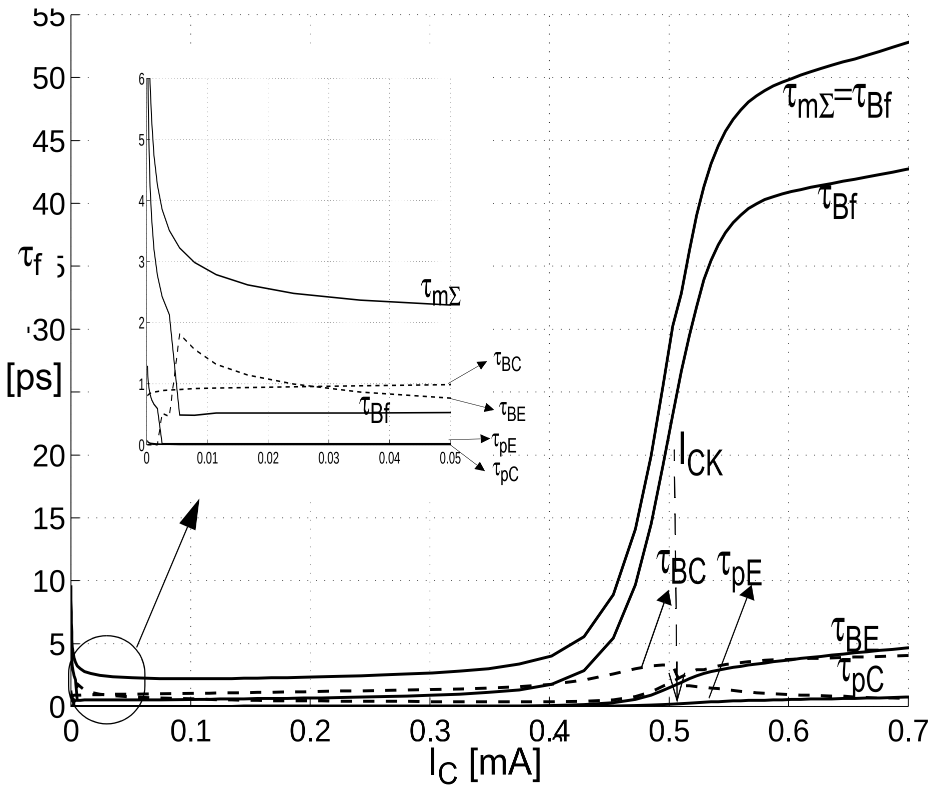


- very accurate voltage dependence (by "design") at zero current
- differences in current dependence caused by inaccuracy of E_{jc} formulation

overall: explicit formulation with reasonable accuracy and simplicity

Transit time

represents minority charge storage in the whole transistor: $\tau_f = \tau_{pE} + \tau_{BE} + \tau_{Bf} + \tau_{BC} + \tau_{pC}$



- relative importance of components in SiGe HBT depends on current density
- low current region:
  - (1) τ_{BC} , (2) τ_{Bf} , (3) τ_{BE}
- high current region:
  - mainly τ_{Bf} dominated (BC barrier !)
- Note: relative importance differs for
  - high-speed device (smaller τ_{BC})
  - Si BJTs (τ_{pC} large at high I_{Tf})
  - GaAs HBTs (τ_{BC} dominated at low I_{Tf})

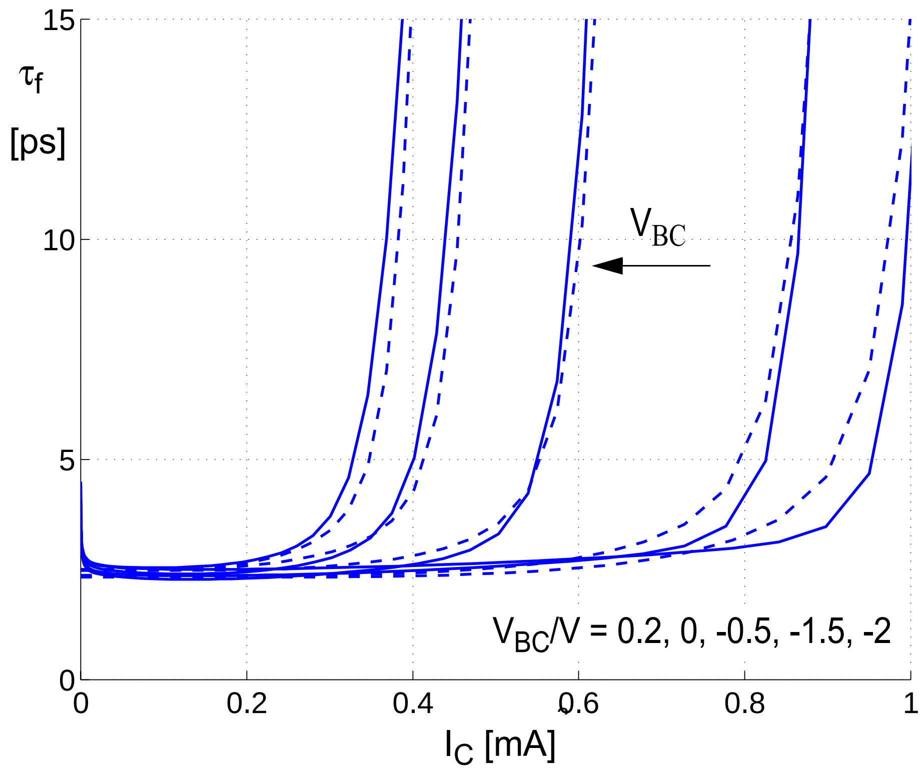
- impact of E_{jc}(bias) mainly on τ_{Bf} , τ_{BC}
  - τ_{BC} defined by incremental BC charge expression: $\tau_{BC}(V_{BC}, I_{Tf}) = \left.\frac{\partial Q_{BC}}{\partial I_{Tf}}\right|_{V_{BC}}$
  - τ_{Bf} model: extension of existing HICUM equation

Modeling the transit time

extended HICUM base component: $$\Delta\tau_{Bfv} = \tau_{Bfvl} f_u\left[1-\left(1-\left(\frac{v_n}{v_{sn}}\right)^{\gamma_u}\right)\frac{I_{Tf}}{u}\frac{du}{dI_{Tf}}\right]\exp(-b_{hc}u)$$

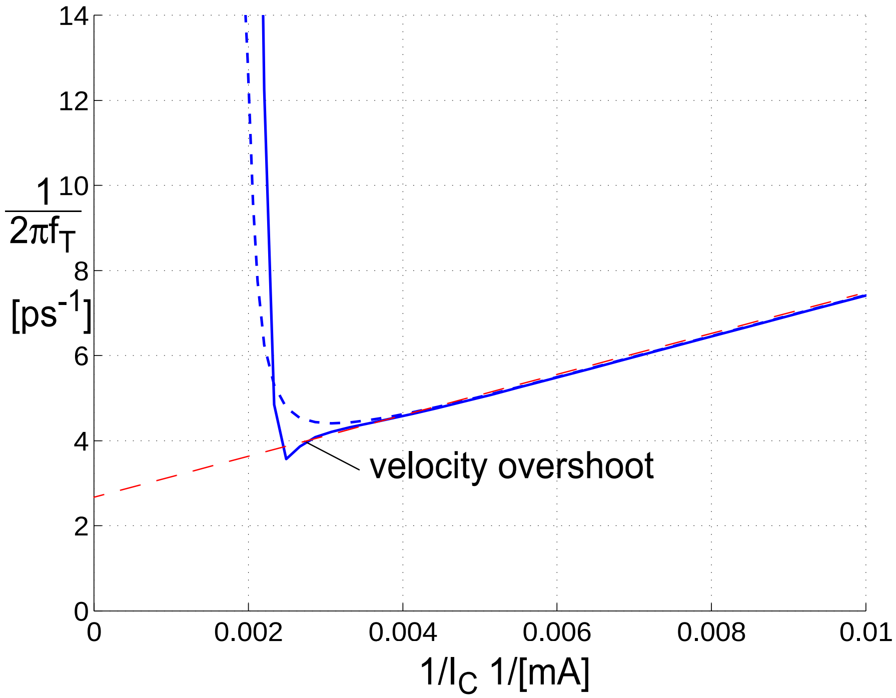
with $f_u(u)$ given in the proceedings b_{hc} as new model parameter, and g_u = 1(holes), 2(electrons)

- both transit time formulations depend on the normalized field $u = E_{jc}(V_{BC}, I_{Tf})/E_{lim}$



- comparison between device simulation and analytical equation:
  - good agreement over
    - wide voltage range
    - wide current density range
  - compatible with already existing HICUM formulation
  - physics-based
- comment on parameter determination
  - can use most extraction procedures already existing for HICUM
  - b_{hc}: see [2] in Proceedings or from fit

Modeling velocity overshoot



- observation:
  certain III-V HBTs show "spike" in transit frequency around peak
- cause:
  scattering of high-energy electrons from the lower to the upper valley
- issues:
  - determination of transit time using standard method (cf. Fig.)
  - modeling of "low-current" transit time

- approach: use E_{jc} as first-order approximation in standard velocity equation

$$v_n = v_{sn} \frac{(v_{max}/v_{sn})u + u^4}{1 + u^4} \quad \text{with} \quad u = E_{jc}(V_{BC}, I_{Tf})/E_{lim}$$

(feedback of faster carriers on field neglected)

External transistor

- series resistance models: mostly geometry dependence
  - r_{Cx} (since not measurable directly on transistor)
  - base resistance components
- (intra-device) substrate coupling
  - compact geometry scalable equations for r_{Su}, C_{Su} or
  - fast numerical procedure
- electrothermal effects
  - compact geometry scalable equations for R_{th}, C_{th} or
  - fast numerical procedure
- geometry scaling effects
  - perimeter depletion capacitance
  - perimeter injection and charge storage
  - current spreading

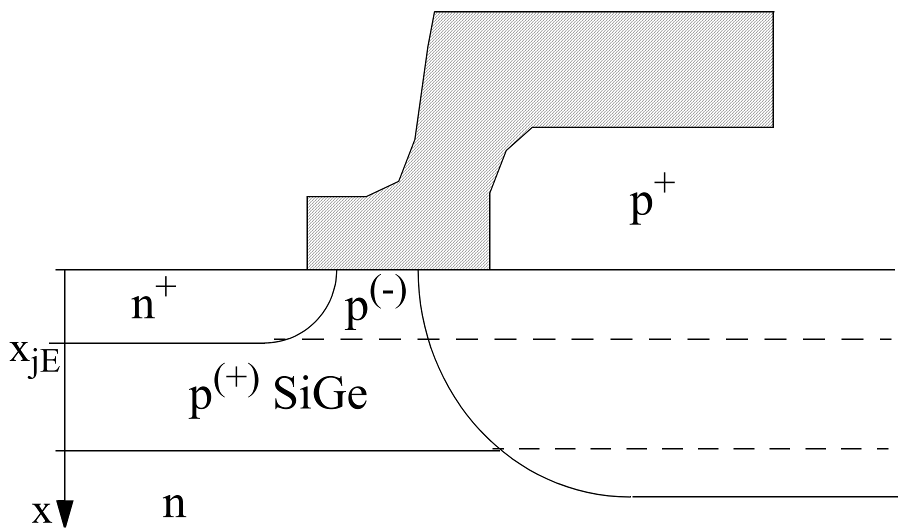
=> mostly geometry scaling related modeling (=> see TRADICA development)

Example: BE capacitance in advanced SiGe processes

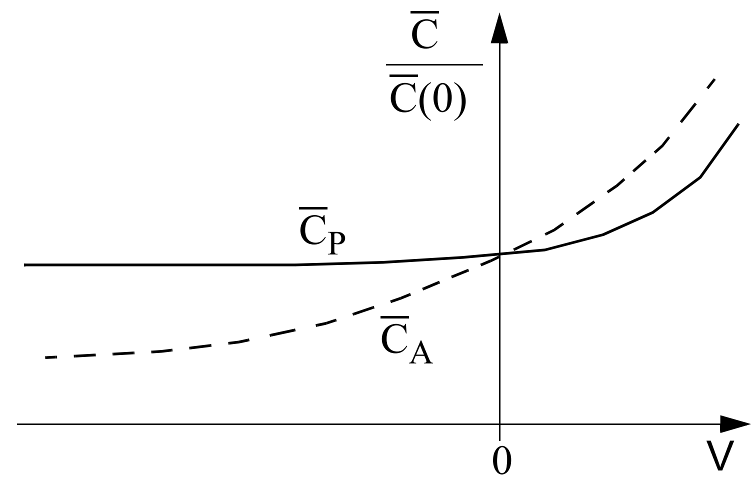
- trends:
  - $x_{jE} \downarrow$ => $N_{Bi} \uparrow$ => $C_A \uparrow$, $C_P \downarrow$
  - SiGe epi => $N_{Bp} \downarrow$ => $\overline{C}_P \downarrow$

  } $\overline{C}_P/\overline{C}_A \downarrow$

BE spacer structure at emitter perimeter



capacitance-voltage behavior



- Si cap layer grown during SiGe deposition is only lightly doped

  => punch-through of SCR at the perimeter (e.g. $N = 10^{17}\mathrm{cm}^{-3}$ => $w_{SCR} = 0.1\mu\mathrm{m}$)

  => bias independent (specific) perimeter capacitance

  => indistinguishable from oxide capacitance C_{Eox} during parameter extraction

  also: need to investigate perimeter injection, minority charge storage and geometry scaling

Related publications

- most recent publications:

[1] P. Sakalas, M. Schroter, W. Kraus, and L. Kornau, “Modeling of SiGe power HBT intermodulation distortion using HICUM”, Proc. ESSDERC, Lisboa, pp. 311-314, 2003.
[2] M. Malorny, M. Schroter, D. Celi, and D. Berger, “An improved method for determining the transit time of Si/SiGe bipolar transistors”, Proc. BCTM, pp. - , 2003.
[3] M. Schroter and H. Tran, „Modeling of base-collector junction related effects in heterojunction bipolar transistors“, (inv. paper), Compact Modeling Workshop of the International NanoTech Meeting, Boston (MA), pp. 102-107, March 2004.
[4] M. Schroter, H. Tran and W. Kraus, “Germanium profile design options for LEC-SiGe HBTs”, Solid-State Electronics, Vol., pp. 1133-1146, 2004.
[5] P. Sakalas, M. Schroter, R. Scholz, H. Jiang, M. Racanelli, “Analysis of microwave noise sources in 150GHz SiGe HBTs”, RFIC Symp., Tech. Dig., pp. -, June 2004.
[6] P. Sakalas, M. Schroter, P. Zampardi, M. Racanelli, “Microwave noise in III-V and SiGe-based HBTs: comparison, trends, numbers“, (inv. paper), Proc. 18th Int. Conf. on Noise and Fluctuations, Canary Islands (Spain), pp. -, May 2004.
[7] M. Malorny, M. Schroter, “Analytical method for calculating elements of an arbitrary equivalent circuit”, Proc. MIX-DES, Poland, pp. -, June 2004.
[8] M. Schroter, “Modeling of distortion in bipolar transistors - A review”, (inv. paper), Proc. 5th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, Atlanta (GA), pp. , Sept. 2004.

- other activities: see CEDIC web-site (http://www.iee.et.tu-dresden.de/iee/eb/eb_homee.html)

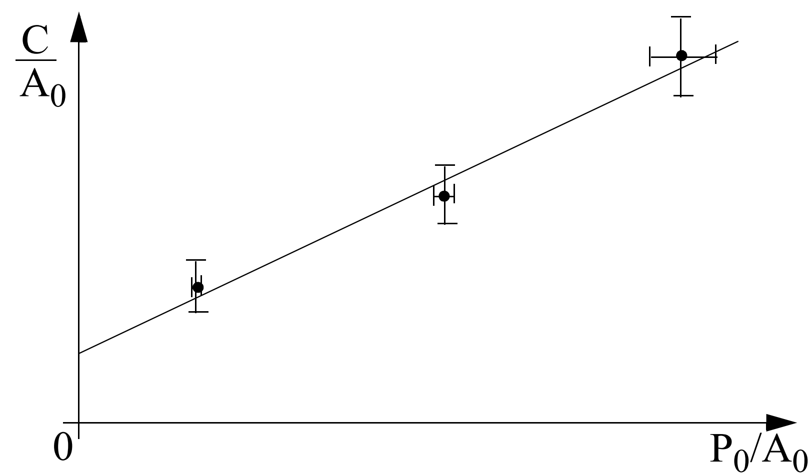
Parameter extraction

Review of error sources that can lead to model inaccuracy

- equipment:
  - chuck, wafer and device temperature
  - calibration substrate, cables, power and flatness, ...
- measurement:
  - bias point (e.g. need I_C, not V_{BE} => I_C), S-parameters (magnitude, phase)
  - signal-amplitude (must be small enough to avoid distortion, but large enough for accurate detection)
  - de-embedding:
    - complexity (multi-step) depends on frequency
    - less structures available than DUTs => equivalent circuit or scalable de-embedding models
- device geometry
  - lateral dimensions (e.g. emitter size) => can be a function of topography (lithography)
  - vertical dimensions (can be a function of lateral dimensions)
  - process tolerances => variation from die to die ...
- model
  - validity limits (equations, equivalent circuit)
  - fit/optimization of characteristics (limited accuracy, selection of unsuitable characteristics,...)

Geometry scalable extraction - revisited

- consider $\frac{C}{A_0} = \bar{C} + C'\frac{P_0}{A_0}$ with $\bar{C}, C'$ as area and perimeter specific parameters to be extracted from measured C, window area $A_0 = b_0 l_0$ and window perimeter $P_0 = 2(b_0 + l_0)$
- measurement error sources:
  - electrical and intra-die (variation of C): ΔC
  - geometry (assuming width and length vary uncorrelated, but with the same absolute value): Δb
- propagation of errors (cf. P. Bevington, "Data reduction and error analysis for the physical sciences") => error range for
  - the y-axis $\frac{\Delta\bar{C}}{\bar{C}} = \sqrt{\frac{\Delta C}{C} + \Delta b_0^2\left(\frac{1}{b_0^2} + \frac{1}{l_0^2}\right)}$
  - the x-axis $\Delta\left(\frac{P_0}{A_0}\right) = 2\Delta b_0\sqrt{\frac{1}{b_0^4} + \frac{1}{l_0^4}}$

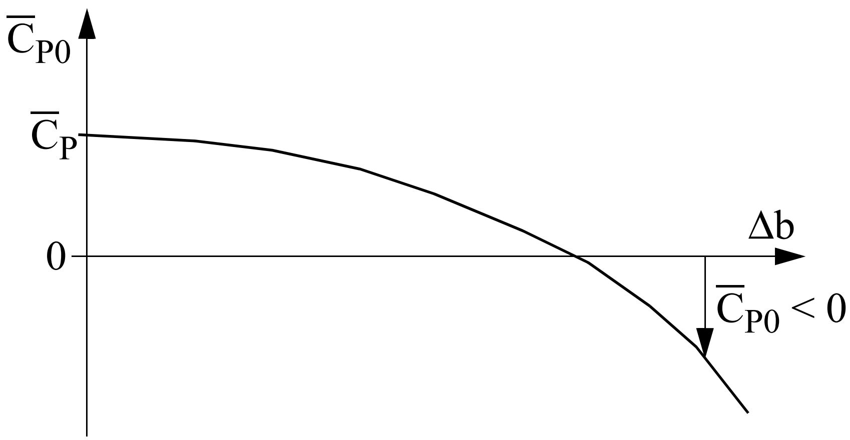


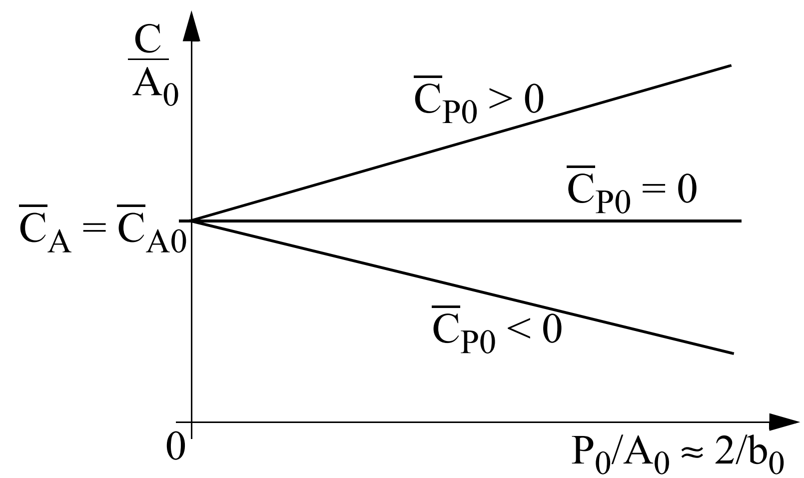
- experimental example see W. Kraus, ICCAP-Workshop 2002, Berlin, Germany

Impact of width uncertainty on capacitance determination

- assumptions
  - test structures with layout dimensions $b_0 << l_0$ => elimination of l_0 variation
  - actual emitter width $b = b_0 + \Delta b$, with Δb as uncertainty or width variation
- use standard equation => area specific component $\overline{C}_A$ = value extrapolated to $b \to \infty$
  - subtract standard equation for two different b (e.g. large and small b)
    => perimeter specific component $\overline{C}_{P0}$ from layout (b_0, l_0) as function of actual (measured) $\overline{C}_P$:

$$\overline{C_{P0}} = \frac{\overline{C_P} + \frac{C}{l_0 b_0}\frac{\Delta b}{2b_0}}{1 + \Delta b / b_0} \quad \Rightarrow \quad \text{for } \Delta b < 0: \ \overline{C_{P0}} = \frac{\overline{C_P} - \frac{C}{l_0 b_0}\frac{|\Delta b|}{2b_0}}{1 - |\Delta b| / b_0}$$





More thoughts on geometry scalable extraction

- fundamentally, size variations (compared to layout dimensions) are unavoidable consequences:
  - single geometry extraction assigns model parameter set to incorrect size
  - problem can only be treated statistically (which is the nature of the variations)
    => the more devices are being used for extraction the better the "average" model accuracy

=> alternatives

use more of the "same" geometry for single geometry extraction

=> ideally: average values of parameters

actually: fit errors are also included and unavoidable due to inherent problem to obtain physical information from single geometry extraction

uses multiple geometry devices

=> geometry scalable extraction

=> average out geometry uncertainty, (more) physical parameters ...

=> fundamentally more accurate than single device geometry extraction

... self-heating

- unavoidable in modern processes during measurements (at higher current densities)

- need to be either included or avoided during extraction
  - include by using corrections (mostly model-based with measured TCs)
  - avoid by using pulsed measurements
  - avoid by using proper test structures and extraction methodology; example: determine series resistances from test structures rather than from I-V characteristics at high J_C

- trends for self-heating:
  - power dissipation is proportional to A_{E0} (and thus n_E)
  - R_{th} is less than proportional to emitter dimensions

  => use $n_E = 1$ for extraction, limit l_{E0}

Model verification activities

- high-frequency noise
- distortion (harmonic and intermodulation)
- 0.18um BiCMOS and 200GHz processes
- benchmark circuits: LNA, mixer, ...   and test chip layout

=> see publications (also from industry and other institutions)

Summary

- increasing model demand and availability (simulators, libraries)
- version 2.2 is on its way ... => feedback ??
- resource issues for productization support still exist,
  while increased emphasis is needed for physics-based modeling
- (required) model development and research
  - collector field formulation => already yields promising results
  - GICCR extension to 2D/3D case will provide clear definition of internal model definition
  - geometry scaling of advanced SiGe processes needs to be investigated
  - hard-saturation and BC voltage-related minority charge modeling (for power transistors)
  - distributed electro-thermal models for power transistors and applications
  - statistical simulation with correlated PCMs for conventional and LEC process
- model verification: various processes