TRADICA Overview: Status and Development

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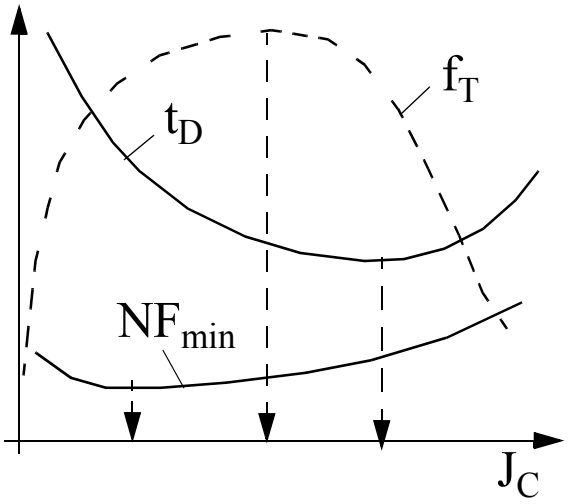
Outline

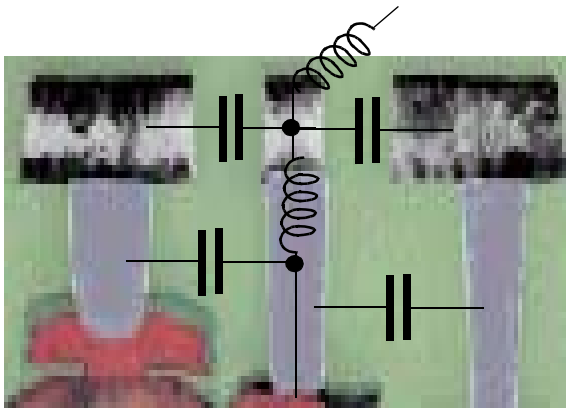
- Tool overview
- Version 5.2 features
- Design system integration

Tool overview

Motivation: the importance of geometry scaling for circuit design and optimization

- LNA design:
  - need to be able to size emitter area for achieving low noise and high gain *simultaneously*
- frequency divider, MUX, DEMUX ...:
  - proper transistor sizing for diff pairs, emitter followers, etc to achieve maximum speed with low jitter, etc. *simultaneously*
- biasing circuits
- statistical design and matching
  - process variations (lateral and vertical) are unavoidable => map size variations to electrical characteristics
- parasitic effects
  - spacers, metalization ...
  - substrate coupling effect
  - thermal effects and coupling

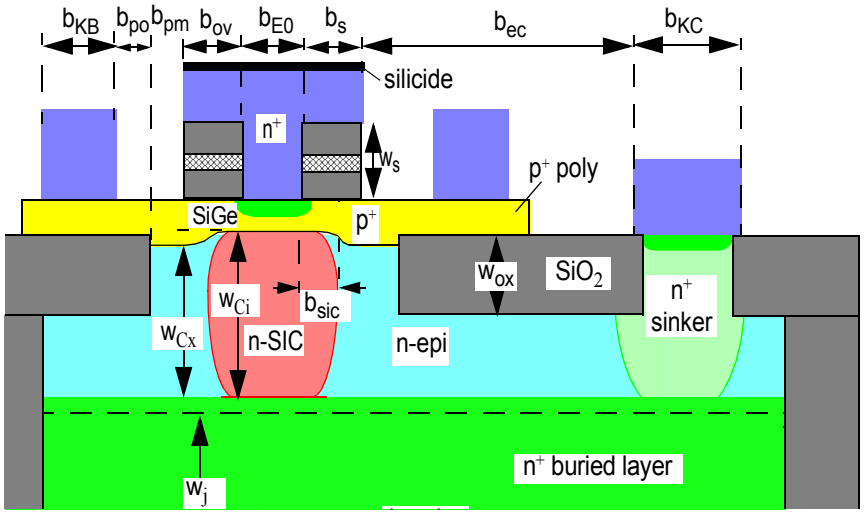


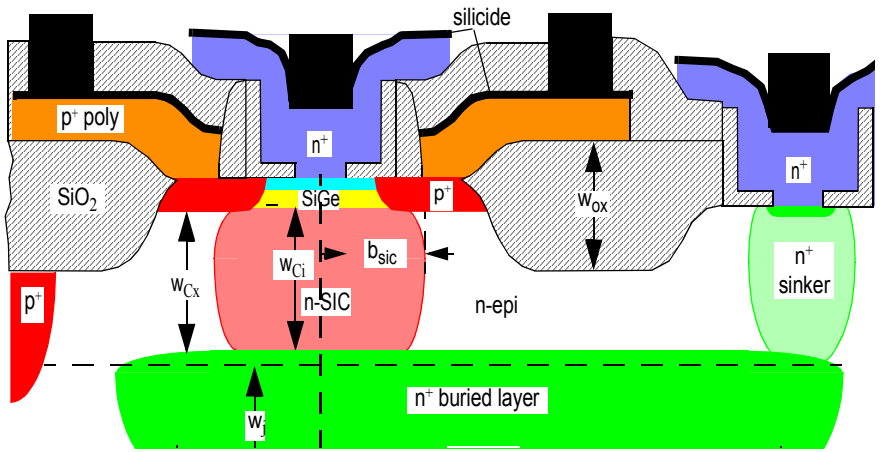


⇒ **fast parameter generation and sizing criteria**

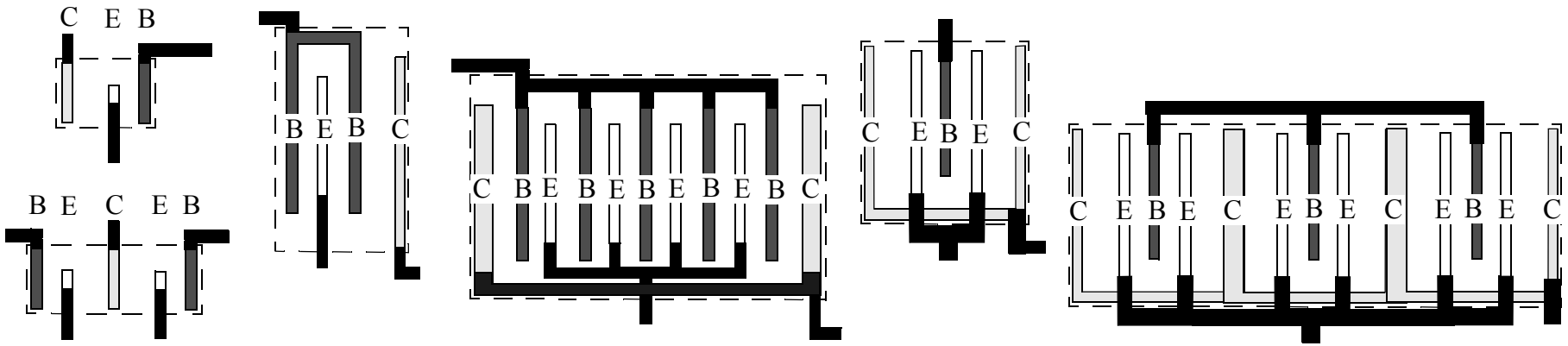
Geometry scaling

dealing with different device designs . . .





. . . and configurations



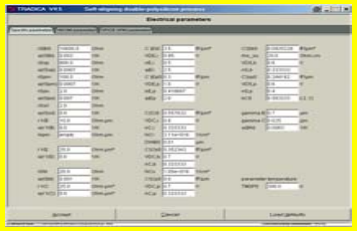
. . . makes implementing ***versatile*** geometry scaling equations in circuit simulators ***unfeasible***

What does TRADICA exactly do ?

Process control monitor (PCM) data

Process specific parameters

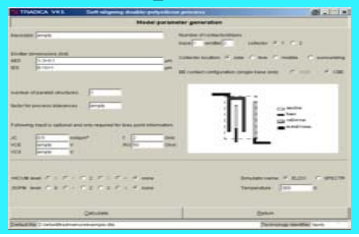
sheet resistances,
capacitances per area,
sat. currents per area,
...



Design rules

Transistor configurations

E width and length, number of E, B, C stripes, location ...



TRADICA

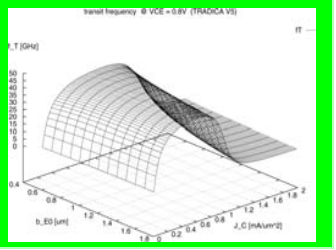
critical bias points
⇒ transistor sizing

model parameters

- device libraries
- for specified bias points

model characteristics

(fT, fmax, NFmin ... as function of geometry and bias)



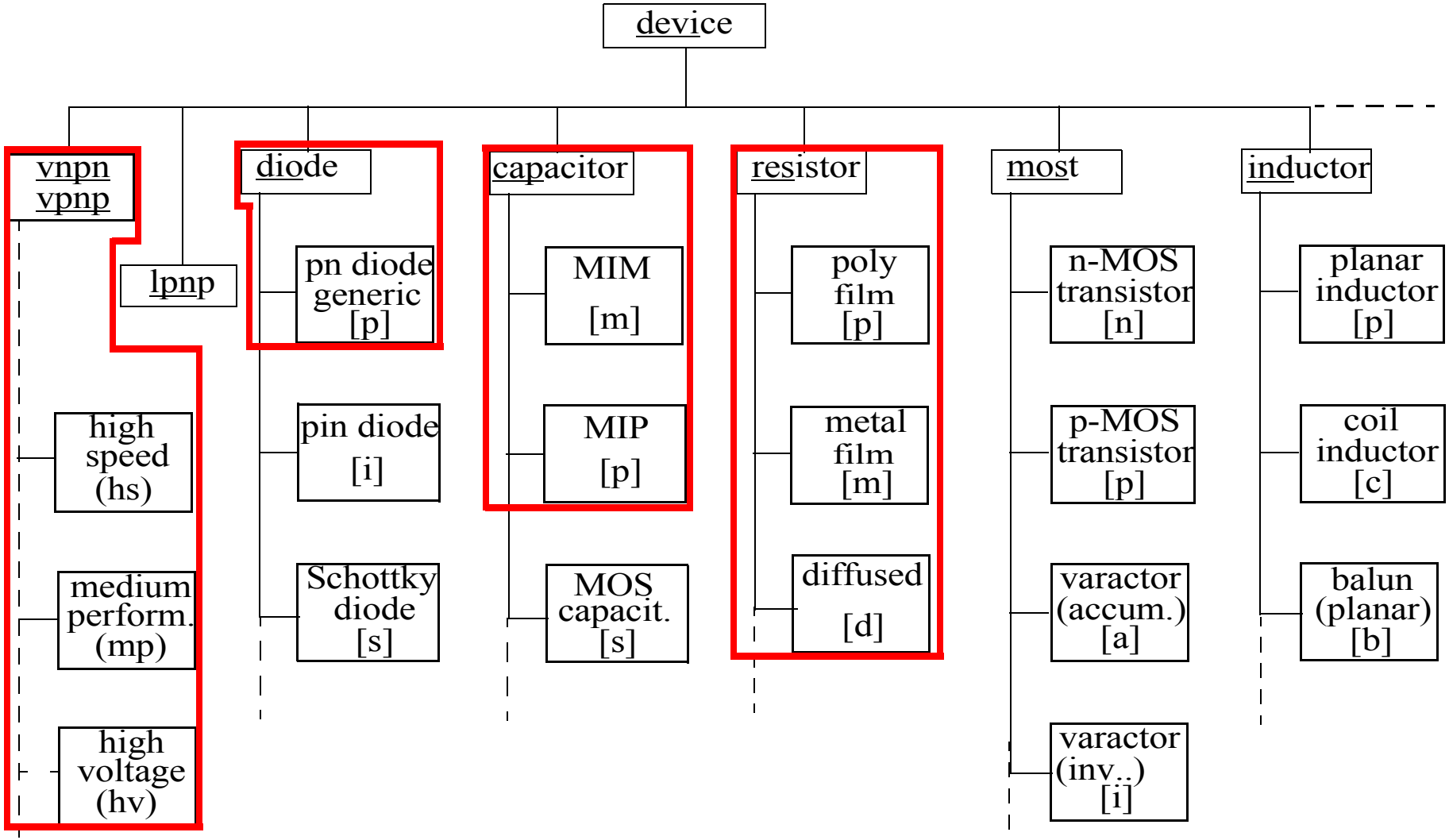
TRADICA version 5.2

new feature overview

- device portfolio
- statistical modeling (incl. correlated PCMs) → see separate presentation
  - internal procedure
  - external simulators
- automated parameter extraction
  - HICUM/Level0
  - SGPM (all Levels)
  - VBIC (planned)
  - from device simulation (DEVICE)
- distributed modeling → see separate presentation
  - electrical
  - electro-thermal
- non-standard geometry scaling

Device portfolio

... typical for h.f. circuit design and process technologies employed



(red boxes indicate models already existing in TRADICA)

"Non-scalable" process

Measured geometry scaling laws do not follow standard relations

$\Rightarrow$ **consequences:**

- limited number of devices => limited circuit optimization and suboptimal performance
- no statistical modeling and simulation => risk of additional design cycle(s)
- inconsistent and inaccurate models => increased effort for model maintenance and support
- passing on process issues to modeling => time delay for library delivery

$\Rightarrow$ cost increase (multiplied on the design side)

Problems can partially be overcome by spending more effort .... at the expense of

- time delays for model parameter delivery
- cost for modeling and for lost window of opportunity for foundry and design house

Note:

Designers will almost always select scalable process

(assuming similar performance, device portfolio)

Possible causes for non-scalable process

- incorrect information on actual dimensions
- emitter window etch (often difficult etch stop) => variation of x_{jE} and r_{SBi}
- transient enhanced diffusion (TED) => increasing w_B toward perimeter
  (mostly suppressed today using SiC)
- broken silicide and bi-modal base resistance distribution => unpredictable with any model
  (this is a yield issue which cannot be captured by statistical modeling !!)
- SIC implant too deep => spacer region pinch-off and increase of emitter perimeter current
- contact resistance: vias vs slot contact => integer vs. continuous scaling

measures for dealing with non-scalable process

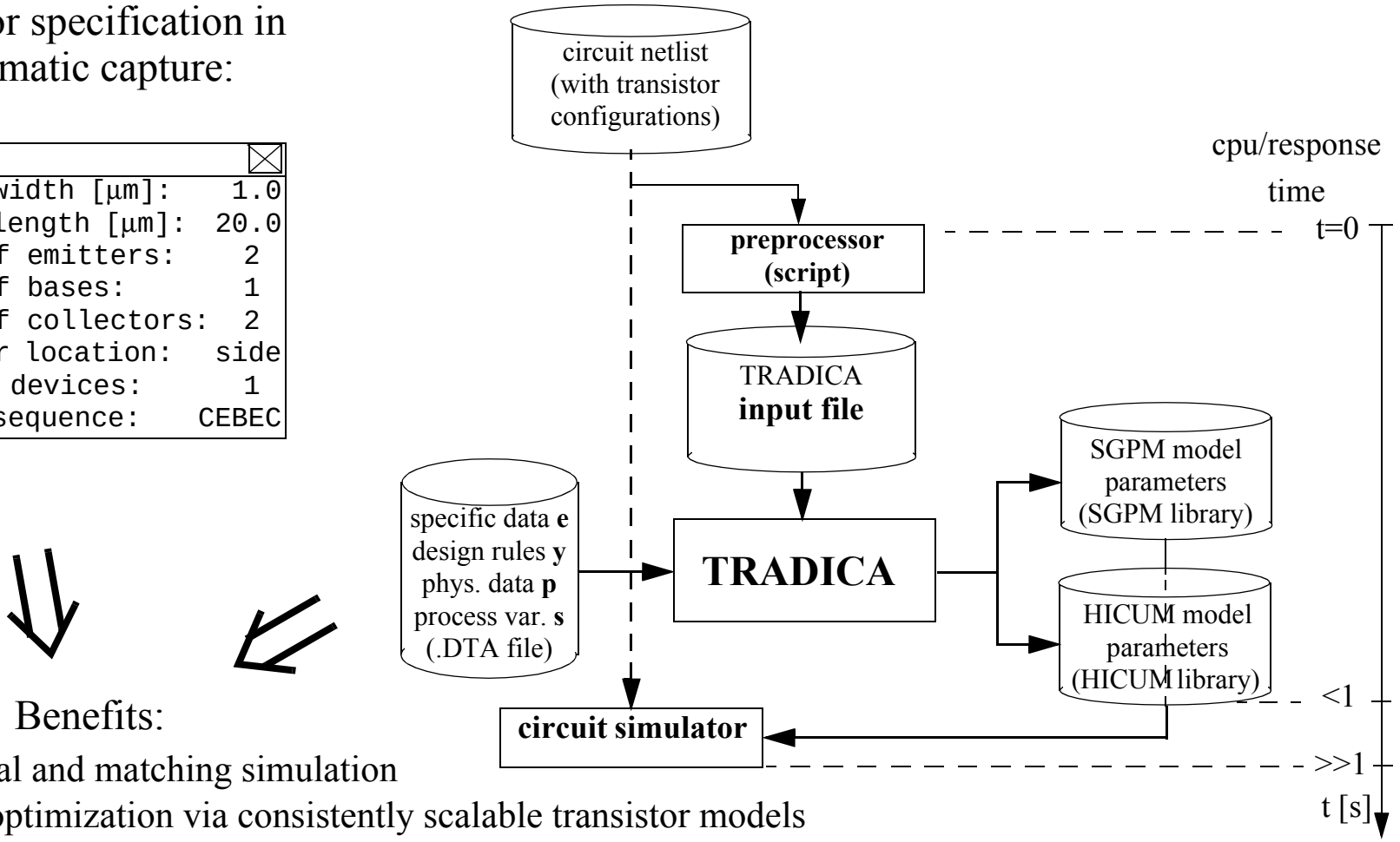
- fix process recipe in the first place (avoids transfer of problems to modeling and design)
- detect physical causes (need proper test structures) => develop new scaling equations
- non-physical post-processing (lack of time, no suitable test structures) => consequences...

$\Rightarrow$ **first step to increase TRADICA's flexibility**: postprocessing of specific parameters

Integration of TRADICA into a design system

transistor specification in schematic capture:

Q5	
emitter width [µm]:	1.0
emitter length [µm]:	20.0
number of emitters:	2
number of bases:	1
number of collectors:	2
collector location:	side
parallel devices:	1
contact sequence:	CEBEC



Benefits:

- statistical and matching simulation
- circuit optimization via consistently scalable transistor models
- parameter transfer via single "technology" file (xxxx.DTA)

⇒ significant enhancement of functionality for design at reduced maintenance effort for foundry

Summary

- TRADICA is a tool for
  - consistent model parameter generation (across sizes for the same model and across models!!)
  - device sizing
  - automated parameter extraction from device simulation
  - educational purposes

- Statistical and matching simulation is performed in a consistent way
  - internal model evaluation => used for corner library generation
  - control of external simulators => used for simulating circuit yield or process variation sensitivity
  - integration design system => seamless link between foundries, modeling and design houses

- Extension towards models for complete device portfolio of h.f. process technologies
  - correlated statistical simulation
  - supports organized modeling effort