TRADICA Overview: Status, Development, Demonstration

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Outline

- Tool overview
- TRADICA version A5.2
- Statistical modeling

Tool overview

Motivation: importance of geometry scaling for circuit design and optimization

- TRADICA is a tool for
  - consistent model parameter generation (across sizes for same model and across models!!)
  - device sizing
  - automated parameter extraction from device simulation
  - educational purposes

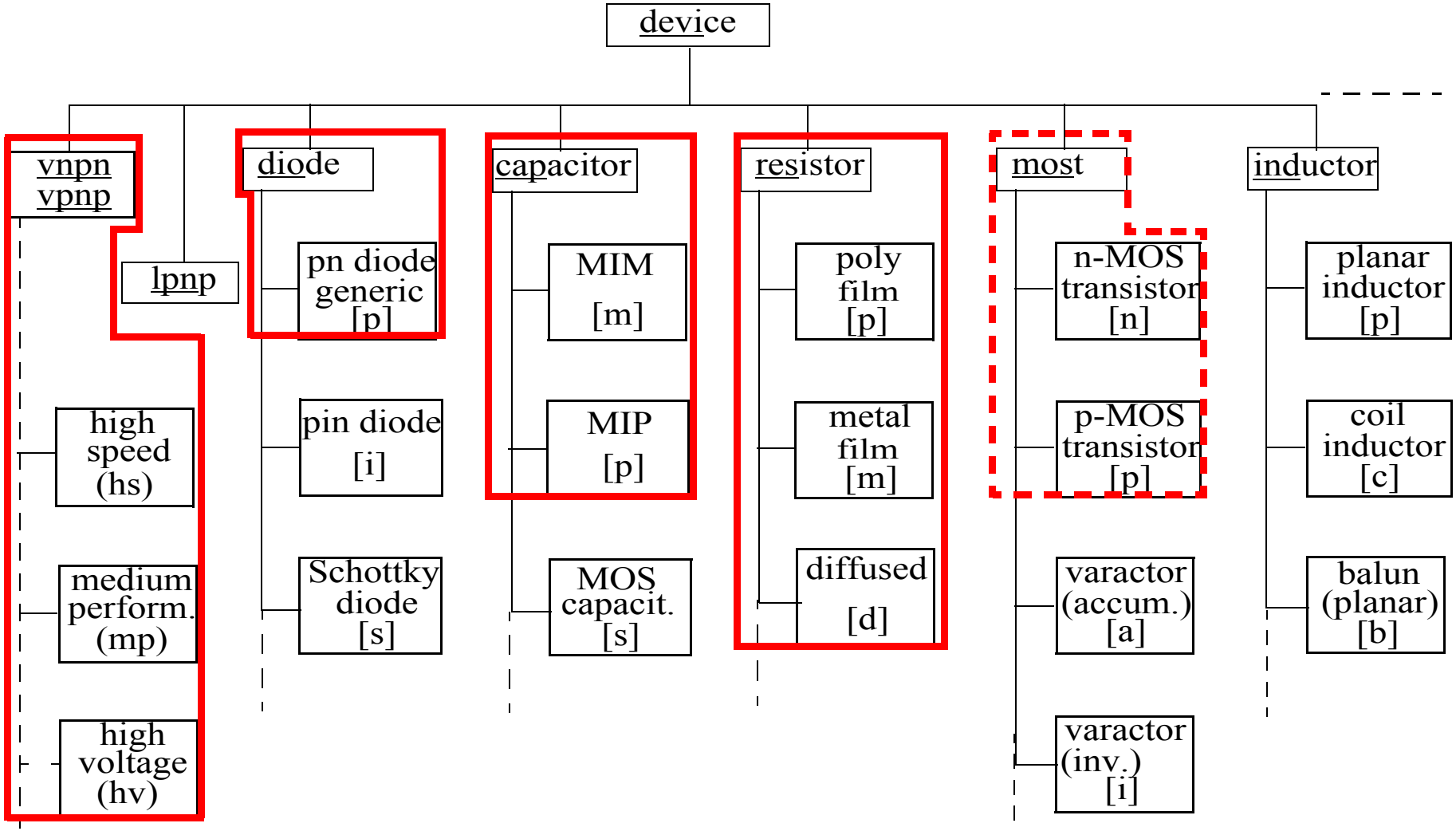
- Statistical and matching simulation is performed in a consistent way
  - internal model evaluation => used for corner library generation
  - control of external simulators => used for simulating circuit yield, process variation sensitivity
  - integration design system => seamless link between foundries, modeling and design houses

- Extension towards models for complete device portfolio of h.f. process technologies
  - correlated statistical simulation
  - supports organized modeling effort

$\Rightarrow$ **fast parameter generation and sizing criteria**

Device portfolio

... typical for h.f. circuit design and process technologies employed



(solid red boxes indicate models already existing in TRADICA, dashed boxes indicate models under development)

What does TRADICA do ?

Process control monitor (PCM) data

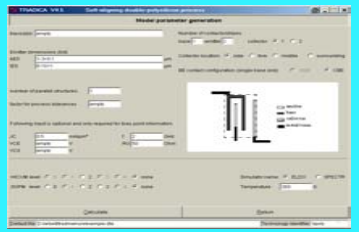
Process specific parameters

sheet resistances,
capacitances per area,
sat. currents per area,
...

Design rules

Transistor configurations

E width and length, number of E, B, C stripes, location ...



TRADICA

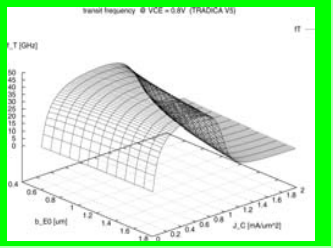
critical bias points
⇒ transistor sizing

model parameters

- device libraries
- for specified bias points

model characteristics

(fT, fmax, NFmin ... as function of geometry and bias)



TRADICA version A5.2

summary of new features

- completely re-designed graphical user interface (GUI) => targetted towards
  - handling of multiple devices
  - link to DEVICE, external simulators

- modular parameter extraction
  - C-V, I-V, transit time, data conversions - first version for device simulation
  - modules can be used to build flexible batch-based procedure
    => extremely fast re-extraction after process change or new measurements

- user-defined geometry scaling
  - on top of standard equations
  - any specific model parameter as function of any geometry parameter

- statistical modeling (incl. correlated PCMs via TPs) $\rightarrow$ see next slide
  - procedure with TRADICA controlling circuit simulation
  - GUI under construction

Statistical modeling

existing solutions

- Monte-Carlo variation of model parameters
  - ignores any (partially strong) correlations between model parameters of single transistor
  - completely ignores correlations between closely spaced transistors (i.e.intra-die correlation)
  - computational effort becomes quickly prohibitive
  - determin. of statistical model parameter distribution is extremely time consuming & erroneous
  - not predictive

=> needs a long time to generate wrong results !!!

- Worst-Case (WC) methods
  - eliminates computational efficiency issue of MC methods at the circuit design level .... but still requires time consuming preparation:
  - often used with principle component analysis, completely ignoring device physics => not predictive
  - originated from digital CMOS with delay time as only FoM => single circuit class
  - what does WC mean for an LNA, mixer, PA, oscillator ... ?

=> not (directly) applicable to analog and h.f. circuits

- process and device simulation: extremely time consuming

Process Control Monitor (PCM) based methods

with physics-based compact models ...

- (quickly) measurable electrical basic data as input (sheet resistance, capacitance per area...)
- physics-based compact models naturally capture also geometry scaling effects => enable matching simulation
- built-in accurate correlation between model parameters
- no need for WC models => applicable to all classes of circuits (but still can be used to create WC models for specific FoMs)

.. and in combination with DoE and RSM:

- Design of Experiment (DoE) approach with Response Surface Method (RSM) drastically reduce computational effort (as compared to MC method)

but: ***need modification of simulation flow control in design system***

can be done by adding an additional layer
(cf. Aspire(Mentor), Spayn(Silvaco) ... or TRADICA)

Existing status

- terminology: statistical ***modeling*** vs. statistical ***design***
- development of additional equations for SiGe LEC HBTs => predictive capability
- definition of technology parameters (TPs) and separation from PCMs
- definition of clear procedure for
  - shifting typical to nominal parameters
  - statistical simulation including correlations between different device types
- mapping of PCM variation (standard deviations) to TP variation using BPV
- verification: ongoing for
  - 1D device simulation (LEC, conventional profile)
  - measurements (Atmel-SIGE2); looking also for data for conventional HBT profile

Statistical modeling: Process Control Monitors (PCM)

... for high-frequency applications

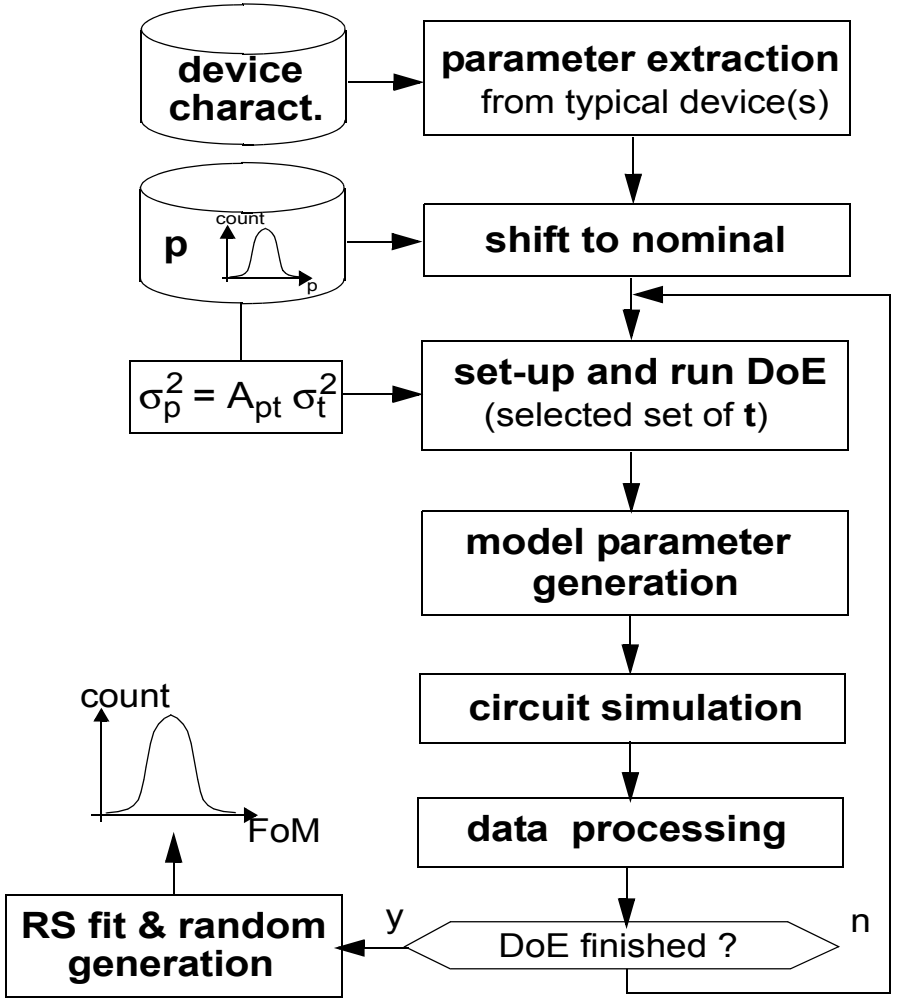
- (general) requirements
  - satisfy both process control *and* modeling
  - fast and easily measurable (sheet resistances, bias points)
  - information on high-frequency transistor behavior: at least the depletion capacitances ! (figures of merit, such as f_T, are desirable but usually are too time consuming to obtain in a production environment)
- test structures and PCM variables

structure	measurement condition	PCM
(rectangular) transistor tetrode	zero-bias	r_{SBi0}
large area high-speed transistor	BE zero-bias, BC zero-bias, currents at low forward bias	$\overline{C}_{jEi0}$, $\overline{C}_{jCi0}$, $J_{C,hs}$, $J_{B,hs}$ ($\&B_f$)
large area high-voltage transistor (without SIC)	BC zero-bias, BC punch-through, currents at low forward bias	$\overline{C}_{jCb0}$, $\overline{C}_{jCb,PT}$, $J_{C,hv}$, $J_{B,hv}$ ($\&B_f$)
various simple contact chains ...	DC I-V (single bias point)	sheet and contact resistances

Statistical modeling: procedure

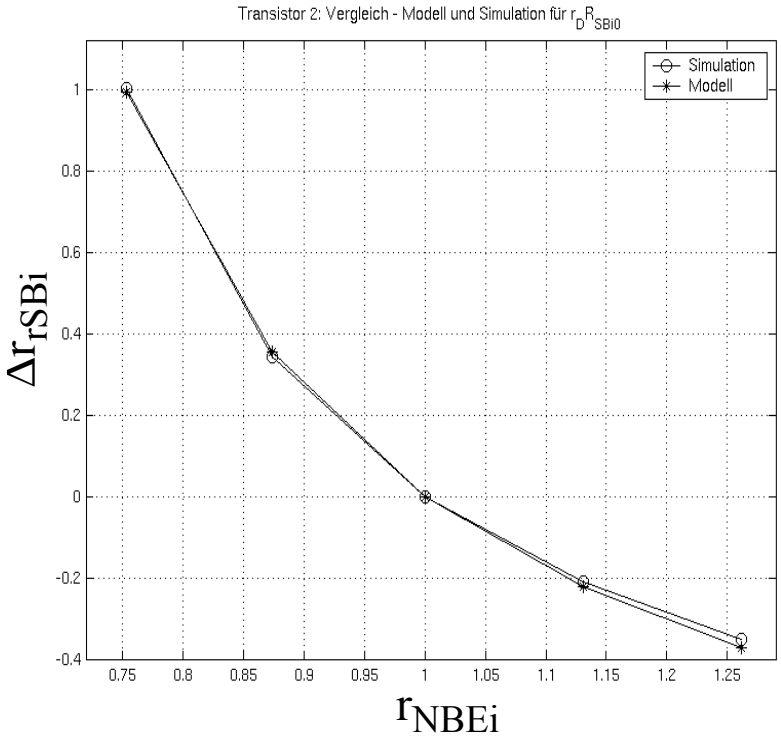
PCM and compact model based statistical modeling and simulation flow (schematic)

- many PCMs are correlated
  - ⇒ cannot be used for statistical modeling
  - ⇒ express by technology parameters
- TP examples:
  - doping concentrations
  - vertical widths (e.g., collector, base, emitter)
  - lateral dimensions (e.g., emitter width)
- **p**: PCM vector as (relative) standard dev.
  - measured on production wafers
- **t**: technology parameter vector
  - given by process conditions or
  - determined from p via (backward) propagation of variances
- simulation effort reduction:
  - Design of Experiment (DoE) method
  - Response Surface Method (RSM)

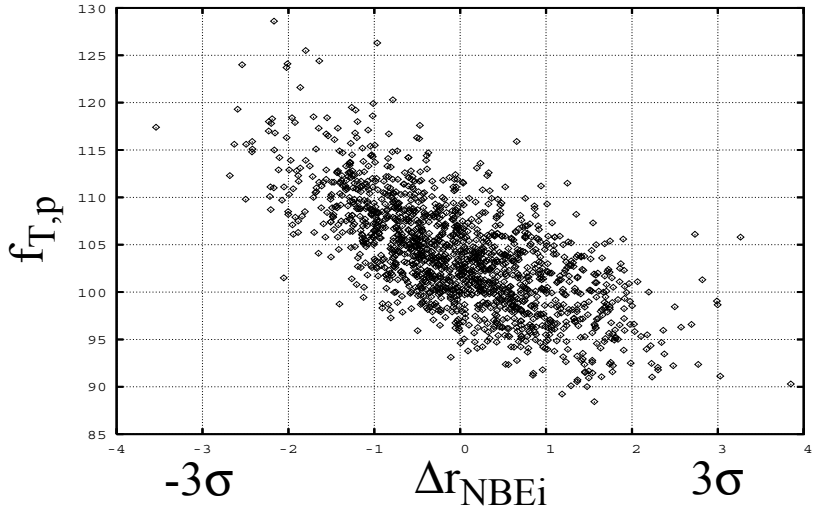


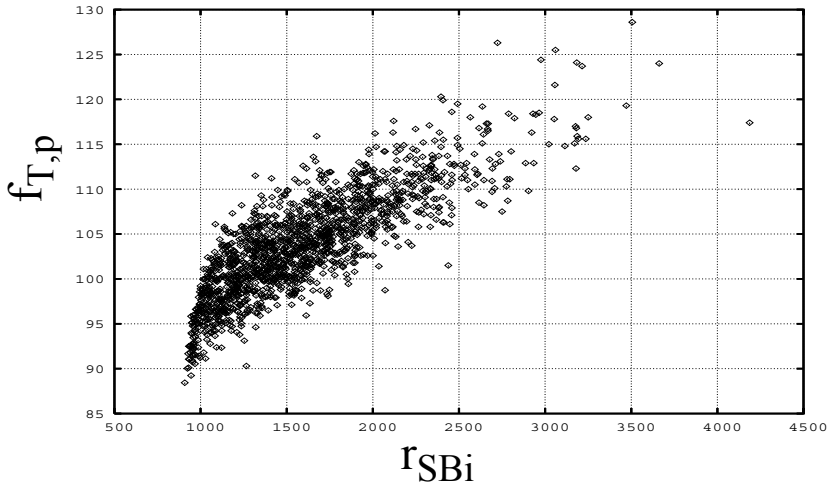
First results: statistical modeling

internal base sheet resistance and peak transit frequency vs base doping (TP)



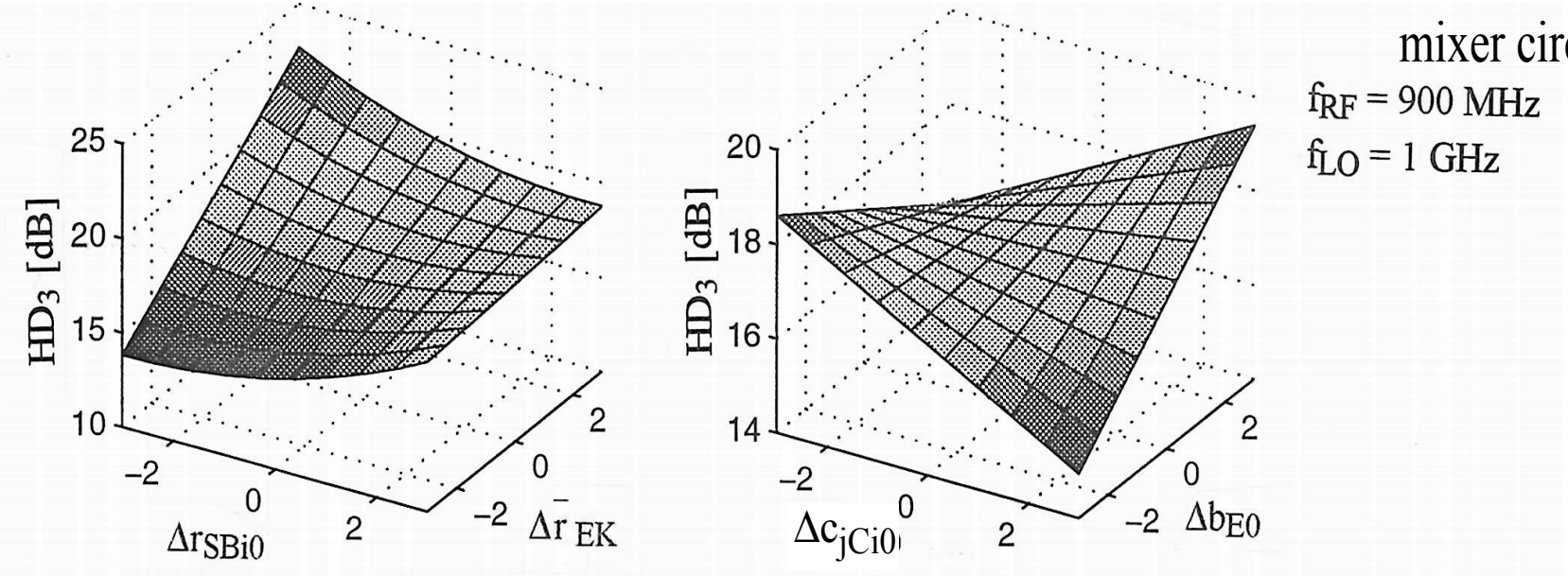
=> accurate model equations





"Desired" results: statistical circuit design

- response surfaces of selected figure(s) of merit (FoM) such as
  - for a compact model: f_T, power gain, noise figure ...
  - for a circuit: power gain, conversion gain, distortion (e.g. IP_3), noise figure, delay time...



- ... as well as probability distribution and yield curve

  => can be used to explore the sensitivity of a circuit w.r.t. process variations

- so far: TRADICA/MATLAB environment

  required: design system integration

Integration in design environment

options

- coding of scaling equations in simulator scripts
  - limited language capability
  - different syntax in different simulators
    => least common denominator permits ***only very simple*** equations and, hence, ***structures***
  - parameter values included in code => one script for each device flavor (high-speed, ...)
  - new copy of script for each process version
  - new copy of geometry scaling code also for each model
    => number of scripts increases rapidly over time => ***very high maintenance*** (incl. test effort)
  - does not solve issue of computational effort (due to MC simulation)
- coding in Verilog-A
  - better language capability and better defined across simulators (but still not identical)
  - can read numerical values from file
  - but: all other issues mentioned before remain

    additional issue for foundries: IP (equations, data) is open to external users
- separate special program (like TRADICA)

    => eliminates all of the above, even adds more advantages

Advantages of using TRADICA in design framework

as compared to geometry pre-processor in circuit simulator or in subcircuit

- updates for new device configurations and structures outside of simulator
  - far easier and faster testing
  - only have to maintain single source of scaling, predictive, statistical code
  - no limitation of script language constructs (=> higher flexibility and functionality)
  - runs with any circuit simulator => allows modular integration concept
  - has been used for model generation and been continuously developed for >20 years
    => huge ***experience*** and ***versatility*** and ***available now*** !!
- allows easy integration of sophisticated equations (incl. running ***external*** simulators)
  - semi-numerical solution of heat equation for geometry scaling
  - predictive and statistical model equations (incl. correlation between devices)
  - fast numerical solution for parasitic structures (e.g. h.f. substrate coupl.) for geometry scaling

  $\Rightarrow$ easy generation of a compact model *hierarchy* (incl. model compaction), satisfying different design needs
- automated generation of other models from reference model
- allows sophisticated device sizing methodologies aiding ***circuit synthesis***
- coupling with device simulation aids process development, concurrent engineering