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Device Modeling Group Goals

- provide physics-based compact models for a ***complete*** device portfolio
  - bipolar transistors: HICUM hierarchy
  - MOSTs: EKV, PSP (?)
  - passive devices: pn-diode (new model), resistors (TRADICA), capacitors (TRADICA), inductors and transformers (t.b.d.)
  - other effects: intra-device electrothermal coupling (Green's function approach in TRADICA), intra-device substrate coupling (t.b.d.)

- tools for structure dependent model generation, predictive and statistical modeling
  - mixed-mode circuit/device device simulator
  - TRADICA (incl. application modules)

  } ⇒ CAD system (P3S)

  ⇘ seamless design system integration

⇒ Enables:

- ***early*** and ***fast*** process evaluation and selection based on product needs
- parallel process and circuit design by predictive modeling ⇒ concurrent engineering
- circuit optimization, statistical modeling, migration between process technologies

HICUM/Level2 - present status

- version 2.2 was officially released in March 2005
  - Verilog-A only code (discussion see later), tested with SPECTRE only
  - code has been reviewed by G. Coram and C. McAndrew; feedback has been incorporated
  - C-code has been generated using ADMS and XML (s. L. Lemaitre's presentation)
  - compiled model (executable) linked to ADS (Tiburon), SPECTRE (ADMS with CMI)
  - DEVICE is available to cooperation partners only (support issue if publicly distributed)
    - code corresponds to SPICE-like model implementation (incl. most important derivatives)

- documentation (continuously updated)
  - separate document contains changes/additions ONLY
  - documented test cases (parameters and results) in ASCII format

- see www for detailed material (www.iee.et.tu-dresden.de/iee/eb/comp_mod.html)

- support contact: Anjan Chakravorty (chakravo@iee.et.tu-dresden.de)
  - focus on version 2.2: code formulation (in Verilog-A), test data, documentation, transfer new developments into product suitable code, version control, release procedure ...
  - version 2.1: implementation issues at some vendors still consumes significant resources
  - HICUM/L0: not included (yet)

HICUM/Level2 v2.2 (cont'd)

summary of new features

- improved temperature dependence
  - more accurate temperature dependent bandgap voltage model
  - static characteristics (V_g for each junction, flexible exponent factor in saturation current)
  - built-in voltages: physics-based extension towards extreme temperature limits
  - transit time: physics-based model for emitter transit time
  - critical current: extended description of saturation velocity
- additional base current caused by BC barrier effect
- various elements
  - internal base resistance: elimination of potentially negative value for high reverse V_{BC}
  - BE tunneling current: connect to either bottom or perimeter B node
  - parasitic BE capacitance: split between perimeter and external B node
- parabolic smoothing functions
  - base reach-through, BE depletion cap, transit time and critical current ...
  - exception: BC and CS depletion caps
- flags recommended for self-heating, vertical and lateral NQS effects

HICUM/Level2 (cont'd)

Version 2.2 summary of new model parameters (and flags)

name	description	default	test	unit	M
ZETACT	exponent coefficient in transfer current temperature dependence	4.5	3.5	-	-
VGE	effective emitter bandgap voltage V_{gEeff}	VGB	1.07	V	-
ZETABET	exponent coefficient in BE junction current temperature dependence	5	4	-	-
VGC	effective collector bandgap voltage V_{gCeff}	VGB	1.14	V	-
VGS	effective substrate bandgap voltage V_{gSeff}	VGB	1.17	V	-
TBHREC	base current recombination time constant at the BC barrier for high forward injection (default is v2.1 compatible)	0 (≡ ∞)	250	ps	-
TUNODE	flag for specifying the base terminal connection of the tunnelling current source: 0 = perimeter node (v2.1 compatible), 1 = internal node	0	1	-	-
CBEPAR	total parasitic BE capacitance (spacer and metal component)	0.0	0.6E-15	F	M
FBEPAR	partitioning factor of parasitic BE capacitance (default is v2.1 compatible)	1.0	0.5	-	-
ZETACX	exponent factor in substrate transistor transit time temperature dependence	1.0	2.2	-	-
FLSH	flag for turning on (1) or off (0) self-heating effects	0	1	-	-
FLNQS	flag for turning on (1) or off (0) vertical NQS effects	0	1	-	-
F1VG	coefficient K_1 in T dependent bandgap equation	$-1.02377E^{-4}$	=	V/K	-
F2VG	coefficient K_2 in T dependent bandgap equation	$4.3215E^{-4}$	=	V/K	-
version	version number	2.1	2.2	-	-

HICUM/Level2 (cont'd)

Version 2.2 summary of model parameter changes ...

no	old name	new name	(new) meaning
	aljei	ajei	ratio of max to zero-bias internal BE depletion capacitance
	aljep	ajep	ratio of max to zero-bias perimeter BE depletion capacitance
	CCOX	CBCPAR	total parasitic BC capacitance (trench and metal component)
	FBC	FBCPAR	partitioning factor of total BC capacitance

... and deletions

no	old name	new name	meaning
	CEOX	deleted	replaced by total parasitic BE capacitance CBEpar and partitioning factor
	KRBI	deleted	-
	ALB	deleted	-

HICUM/Level2 v2.2(cont'd)

release procedure / quality control

- **step 1**: after development of new equations (mostly physical effects)
  => detailed proposal to cooperation partners for discussion/feedback (incl. HICUM WS)
- **step 2**: incorporate feedback into formulations and internal (development) simulator
  => provide prototype version to cooperation partners & sponsors for test and review
- **step 3**: present new version (physics & numerics) to CMC for feedback
- **step 4**: finalize physics-based formulation and development code
  => transfer and implementation in production release prototype (Verilog)
- **step 5**: testing of Verilog code vs. development simulator
  (implementation done by different persons; possibly incl. EDA cooperation partner)
- **step 6**: official release"through" CMC (code, document with changes)
  (gather feedback from general community, possibly update code and doc.)
- **step 7**: finalize model documentation and web-site, code fixes

HICUM/Level2 v2.2(cont'd)

- model support
  - parameter extraction and determination
    - fundamental determination procedures are outlined (but can depend on process technology)
    - parameter extraction work belongs to model deployment and commercial application
      => model developer cannot provide (free of charge) parameter extraction
  - implementation: see slides on Verilog-A release

- reminder ...
  - Neither DEVICE FTN code nor SPICE3F are released as both are proprietary simulators
  - For HICUM in SPICE3F or the SPICE3F package, please contact Prof. J.-C. Perraud
  - Other than CEDIC co-operation partners, only Verilog-A model is supposed to be released and supported

Other information ...

- ... related to Cadence slides from 12/04 (re. HICUM implementation)
  - model benchmark from Toshiba (presented at MIXDES 2004) ; simulator: ADS

	DEV	Transient 1/8 DIVIDER	HB IP3 MIXER	HB TONE gainstage
HiCUM	0.80	77.2	220.7	3.3
Mextram 503	0.80	70.9	193.7	Didn't converge
Mextram 504	0.76	90.6	189.0	Didn't converge
VBIC	0.87	89.2	231.6	5.08
Gummel Poon	2.48	11.9	112.5	2.39

Table. 4. Summary of simulation benchmark test in seconds.

HICUM/Level0 - present status

Version 1.1

- surprisingly high demand => requested by all major simulator vendors
  - has diverted support resources from Level2v2.2

- changes vs. v1.0
  - v1.1 incorporates some of the HICUM/Level2 v2.2 improvements, such as: hyperbolic smoothing, improved temperature description (s. v2.2) ***plus*** pnp, noise
  - Verilog code: clean up, improvement of organization, use of language constructs, limiting ..

- implementation
  - ***separate*** model code $\Rightarrow$ full advantage of speed improvement
  - status: see separate slide "Simulator Availability"

- release
  - Verilog code only
  - DEVICE implementation planned (resource issue)

HICUM/Level0 (cont'd)

Version 1.1

- model verification / application to various process generations
  - 150GHz SiGe BiCMOS process from Jazz (see BCTM 2002)
  - 70GHz SiGe BiCMOS process from Infineon
  - 70GHz SiGe HBT process from ST
  - 230GHz SiGe HBT process from ST
  - 90GHz SiGe LEC HBT process from Atmel

- parameter extraction and generation
  - Fregonese et al., MIXDES 2004
  - journal paper to be submitted
  - XMOD: ICCAP-based solution
  - TRADICA: model generation from HICUM/L2

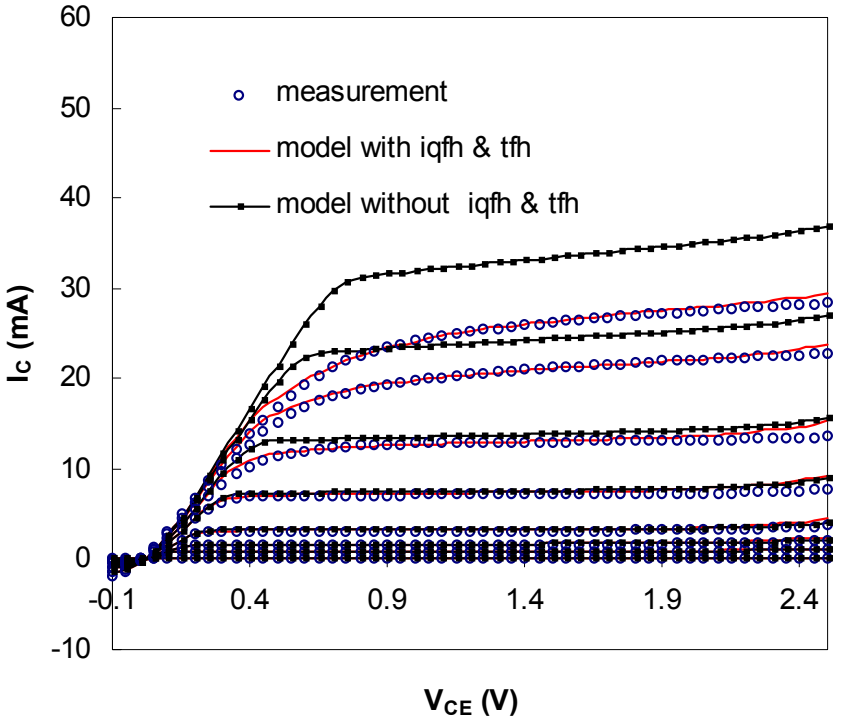
note on support: model has been requested by many companies, but

- development is only partially financially supported by ST and Jazz
- productization is not being funded at all !!

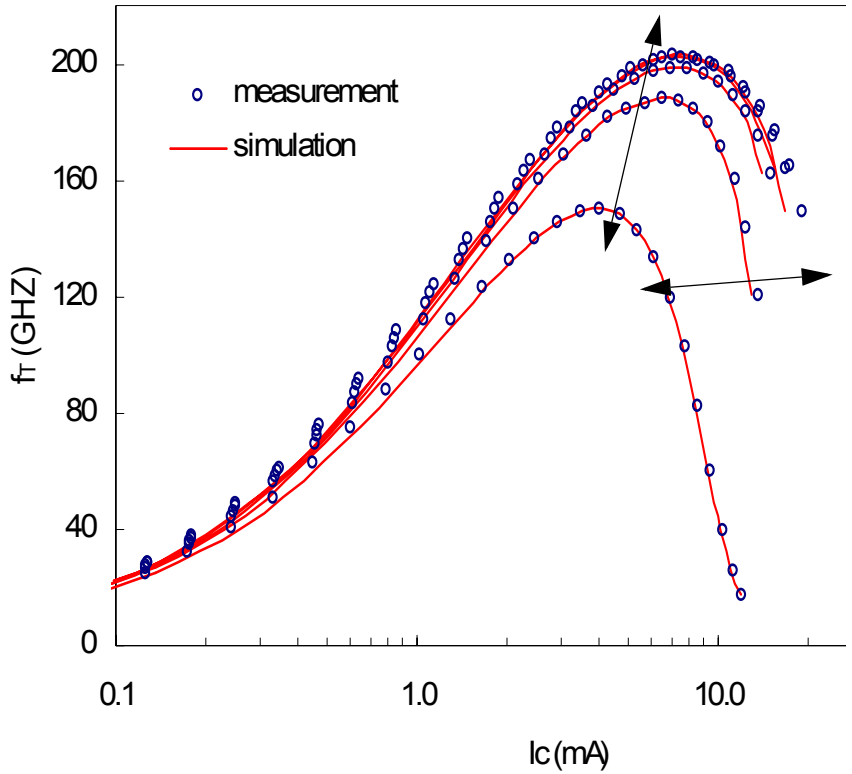
HICUM/Level0 (cont'd)

Version 1.1

output characteristics with and without high-current correction



transit frequency ($0.3*3.7\mu m^2$)



HICUM/Level0: summary of features

(... and improvements with respect to the SGPM)

- derived from HICUM/L2 formulation (= accurate reference)
- simple equivalent circuit with the same topology as the SGPM
- improved transfer current equation (bias dep. forward Early-effect, clearly defined non-ideality coefficient, simple explicit high-current/quasi-saturation correction)
- improved transit time and minority charge model (quicker and more reliable parameter extraction, significantly higher accuracy (based on simplified HICUM/L2 formulation)
- internal base resistance (more accurate and physics-based description of both conductivity modulation *and* emitter current crowding)
- (weak) avalanche breakdown in the base-collector junction
- includes parasitic (bias independent) BE and BC capacitances
- full temperature dependence, single-pole s.h. network (& external thermal node)
- parameter determination
  - single device parameter extraction possible
  - *automated* generation of geom. scalable parameters from HICUM/L2 at no **extra** effort/cost

Availability of HICUM in Circuit Simulators

(version numbers and some comments refer to latest tests (dated 6/04) at STM on LNA, mixer and frequency divider)
(Please contact simulator vendor or see vendor web-site for details and the latest status of availability)

simulator	*1st release*	*latest version*	*L2-V*	*L0-V*	*comments*
ADS	**7/00**	**ADS2003C**	2.1	1.0	very stable and fast
ELDO-RF	**10/99**	**AMS2004.1/2**	2.1	rec 1.1	very stable and reasonably fast
AnalogOffice	**2003**	**rel. 04/04**	2.1	1.0	numerically stable
SPECTRE-RF	**10/99**	**5.0.33.031104**	2.1	rec 1.1	have now promised to fix bugs in L2
Smart-SPICE	**11/00**	**rel. 11/00**	2.?		can be combined with UTMOST
APLAC	**10/01**	**7.92c**	2.1	rec 1.1	still limited stability for L2
HSPICE	**2/01**	**2004.2-beta2**	2.1	rec 1.1	full compatibilty with AWR-AO for L2
TEKSPICE	**8/02**	**rel. 8/02**	2.?		proprietary numerical improvements for L2
GoldenGate	**?/03**	**3.3.14**	2.?		
HSIMplus	**4/02**	**5.0_2004.20.7**	2.?	rec 1.1	latest release L2 in May04;
SPICE3F5	**4/02**	**11/04**	rec 2.2	rec 1.1	reference simulator: HB, Verilog & Compiler

- Various other (partially in-house) simulators (ASX (IBM), Eagleware, Micro-Cap, NEXXIM (Ansoft) ...)
- Verilog-A version of model code; also, L2 stand-alone simulator enabling coupling with other tools

Model release format

(summarized from various discussions)

- Question: Why release compact models in Verilog-A (V-A) code only ?

Answer: (i) V-A is a commonly defined simulator independent standard that allows potential model users to immediately evaluate a model in their mainstream circuit simulators for their process technologies;
(ii) V-A model compilers are now available that translate V-A code into C code that can the be linked to the simulator.
(iii) test data can be generated flexibly at each simulator vendor

- Q: Isn't Verilog-A code too slow for circuit simulation ?

A: (i) Yes, but the V-A code is only for model evaluation purposes, and not for circuit simulation and (production) parameter extraction;
(ii) Compiling the Verilog code and linking the resulting executable to the simulator will yield fast model execution.

Model release format (cont'd)

- Q: Q: As EDA vendor, I want to minimize the implementation effort and need SPICE compatible code C code!

  A: All simulators have different model interfaces and data structures. Hence, a model developer can only satisfy a SINGLE simulator vendor with the model code format. However, a V-A compiler can generate code directly for each simulator (if the EDA vendor funds the development of the related compiler option.

- Q: Compiler generated V-A code is not readable, while as EDA vendor, I need read able code to be able to optimize it for performance!

  A: (i) Define readable code! There is no guarantee for readable hand-written code.
  (ii) Compilers can be enhanced to produce "readable" code and partially already offer some features in this direction (see ADMS's color coding of variables).
  (iii) Compilers can also be enhanced to produce optimized code, which is a ***one-time*** effort compared to performing this work for every model release again.

Note: model derivatives depend on state variables which can vary depending on simulator implementation

Model release format (cont'd)

- Q: For model implementation (simulator, parameter extraction tool), I need code with ***derivatives***! Why can't the model developer provide the derivatives ?

A: (i) Calculating the derivatives is ***not required*** for (physics-based) model development and only an additional burden that slows down development.

(ii) If a model developer would use a Math tool to calculate the derivatives, he would have to ***maintain an additional code version*** and to still transfer that tool's results into C code. A model compiler does the same but does not require the additional code (which is also not necessary for model development).

(iii) Model compilers generate ***complete*** derivatives. This technique is superior to hand-calculated and -coded derivatives from the developer which have proved to be unreliable in the past.

Note: EDA industry is grossly underfunding model productization !

Model release format (cont'd)

- Q: For model implementation, are still test data required ?

  A: Ultimatively, only a netlist and test model parameters should be required but not the often vast amounts of test data, since each model "implementor" can now use the Verilog-A model code to generate test data for any test set up.

- Q: Once a compiled model has been created and linked to a simulator, can that executable (of the compiled model) be distributed to model users (employing of course the same simulator) ?

  A: This seems to have to be answered on a case by case basis;
  - Cadence requires to sign an NDA for the CMI => no distribution allowed
  - ADS with Tiburon compiler: distribution seems possible
  - ELDO ? others ?
  - Is this also dependent on the compiler used (ADMS, Tiburon) ?

Model release format (cont'd)

- Q: VA compiler generated executable code is slower than executables created from hand-optimized code ?

  A: (i) The difference depends on the model and seems to be 10...20%.
  (ii) While this may be the case for the first version of existing VA compilers it is expected (by compiler developers) to be significantly reduced in upcoming versions.

Summary:

model release in Verilog-A solves long-standing problems
=> extremely attractive approach for providing on-demand custom models

Model release format (cont'd)

some issues

- In the past, EDA vendors have failed to agree on same simulator-model standard !
  - Verilog-A fulfills exactly this purpose for model developers
- Some existing limitations with the Verilog-A code release approach
  - support of a standard node voltage limiting feature ("pnjlim") to improve convergence for elements with exponential characteristrics (already addressed by LRM 2.2)
  - high power in electrothermal simulation: special temperature increase limiting ?
  - node collapsing feature for zero series resistances (can be easily included in compilers)
- Non-Quasi-Static effects
  - vertical NQS effect: function absdelay() is not recommended => what to use?
  - lateral NQS effect: need to have value of C=CJEI+... in parallel to RBI with charge C*VRBI
- Correlated Noise in bipolar transistors
  - correlation factor is frequency dependent => presently testing possible solution ?
- Model compiler(s)
  - still some difficulties to get model compilers running on different OSs
  - HICUM/L0 in SPECTRE: need to match specific versions of UNIX, SPECTRE/CMI(?), ADMS

Model development and deployment support issues

... apply to all model developers

- CMC
  - has started in 2004 to support HICUM/Level2 productization (with limited amount though)
- EDA companies (see slide with model availability) have
  - been demanding *significant* effort/resources for supporting implementation
  - not financially supported above efforts (except Agilent in 2000)
  - partially offered/provided software donations (helpful, but does not provide cost of living)
- foundries
  - have financially supported model development (but productization through CMC only)
- design houses
  - expect quality "models" to be included in design kit and associated cost
  - have demanded some effort/resources for supporting model related questions

=> significant interest and demand but little willingness for financially supporting development and, especially, required productization effort

Model development at universities - reiterated

- task/work *must*
  - have sufficient research (theory and experiment) contents to qualify for theses
  - not be service-type of work competing with existing companies to avoid law suits (cost dumping)

- implementation of results
  - can only be for demonstration purposes
  - *must not require* significant manpower (examples: GUI, coding in *several* simulators, ...)
  - cannot use cost- or manpower-intensive EDA tools

- release/deployment *must not require*
  - significant maintenance (including, e.g., legacy issues, extensive versioning effort)
  - to be forced into legal obligations and responsibility for functionality other than for developed case
  - to be forced to disclose IP into public domain in violation of existing laws for inventions

Model development work

... towards version 2.3

- improved GICCR:
  - bias dependent weighting functions for 1D BC barrier modeling
  - geometry dependence based on multi-dimensional Master-GICCR (s. WCM 2005)

- effects in III-V HBTs: merging UCSD model features with HICUM
  - GICCR: include (BE) barrier diffusion in GICCR
  - transit time: include velocity overshoot (using collector field model published at WCM 2004)
  - current dependent BC depletion capacitance (using collector field model publ. at WCM 2004)

- Other:
  - h.f. noise correlation (possibly already in v2.2 as addendum)
  - study best option for implementing NQS effects (numerical issues, correct physics)
  - simpler model for voltage dependent BC, CS capacitances (PT *and* forward bias limiting)
  - improved BC breakdown model (using collector field model published at WCM 2004)
  - geometry effects (new ones, non-standard scaling)

- further input from model users is solicited

Most recent related publications (s. also web-site)

- Papers (s. also http://www.iee.et.tu-dresden.de/iee/eb/eb_homee.html)

[1] P. Sakalas, M. Schroter, R. Scholz, H. Jiang, M. Racanelli, “Analysis of microwave noise sources in 150GHz SiGe HBTs”, Tech. Dig. RFIC Symp., Fort-Worth (TX), pp. 291-294, 2004.

[2] P. Sakalas, M. Schroter, P. Zampardi, M. Racanelli, “Microwave noise in III-V and SiGe-based HBTs: comparison, trends, numbers“, (inv. paper), Proc. SPIE 18th Int. Conf. on Noise and Fluctuations, Canary Islands (Spain), pp. 151-163, 2004.

[3] M. Malorny, M. Schroter, D. Berger, D. Celi, “Analytical method for calculating elements of an arbitrary equivalent circuit”, Proc. MIXDES, Poland, pp. 79-84, 2004.

[4] M. Schroter, P. Sakalas, H. Tran, “Modeling of distortion in bipolar transistors - A review”, (inv. paper), Proc. 5th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, Atlanta (GA), pp. 131-134, 2004.

[5] M. Schroter, “High-frequency circuit design oriented compact bipolar transistor modeling with HICUM”, (inv. paper), IEICE Transactions on Electronics Special Issue, 2005, in print.

[6] M. Schroter, H. Tran, “Two-/three-dimensional GICCR for Si/SiGe bipolar transistors” Workshop on Compact Modeling, International NanoTech Meeting, Anaheim (CA), May 2005.

[7] P. Sakalas, J. Herricht, M. Schroter, P. Zampardi, "Verification of π-Equivalent Circuit based Microwave Noise Model on AIIIBV HBTs with Emphasis on HICUM", IMS, Long Beach, June 2005.

- Tutorials, book chapters

[8] P. Sakalas, J. Herricht, M. Schröter, “Noise measurements and modeling of high-speed Si devices“, invited tutorial at the IEEE Workshop on Compact Modeling for RF/Microwave Applications, Montreal (Canada), Sept. 2004.

[9] M. Schroter, “Modeling of SiGe bipolar transistors”, invited tutorial at the Modeling Workshop of the Fabless Semiconductor Association (FSA), Santa Clara (CA), Oct. 2004.

[10] M. Schroter, Chapters “Advanced compact bipolar transistor models - HICUM” and “Integral Charge-Control Relations” in “The SiGe Handbook”, ed. by J. Cressler, CRC Press 2005, in print.

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