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ÉCOLE NATIONALE SUPÉRIEURE D'INGÉNIEURS DE CAEN
& CENTRE DE RECHERCHE

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New Models into SPICE

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using the new Verilog A Model compiler for SPICE 3F5
(+ manual optimisations)

1- New features of the new Verilog A Model compiler

2- New Models : (+ manual optimisations)

2.1 limiting strategies :
=> type 1
=> type 2

2.2 Models (from 2006 Verilog A code) :
=> HICUM level 0 : hicumL0V1p11 ::> HIC206
=> HICUM level 2.1 : hicumL2V2p11 ::> HIC216
=> HICUM level 2.2 : hicumL2V2p21 ::> HIC226
=> MEXTRAM level 504 .6 ::> TS5046
=> VBIC level 1.2 .6 ::> VBIC126

3- Circuits and Parameters sets to test each models

4- Simulations Results

5- Remaining Works ...

6- Other Developments

7- CONCLUSIONS

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1- New features of the new Verilog A Model compiler :

1-1 "V(n1,n2) <+ exp" ....

BUT in fact NOT USED ! ! :

****

=> In fact not used in initial MEXTRAM && VBIC
Verilog A code

=> to have fair time simulations comparisons,
also not used in all SPICE new HICUM
Verilog A code
(some slight modification done)

ie : ex : HIC226
5 Ext nodes : C,B,E,S,TSH , 5 Int nodes : CI,BP,BI,EI,SI
more when using feature : "V(n1,n2) <+ exp"
6 Int Branch nodes :
br_b_bpNode, br_bp_biNode, br_ci_cNode, br_ei_eNode,
br_si_sNode, br_tsh_gndNode

So at least : 10 nodes versus 16 nodes

note : the Matrix Solving Time is said to vary as
Matrix Size at a power of 3 : NbNodes ** 3

1-2 "@(initial_model)" (done as : "@(initial_step)") :

=> potential error in « hicumL2V2p21.va » depending on how
is implemented "@(initial_model)" :

ex : « hicumL2V2p21.va » uses implemented method :
a: begining of analysis (then error !!)
b: begining of a model (then error !!)
c: begining of a device (then OK !!)

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2- New Models : (+ manual optimisations)

2.1 limiting strategies :

=> type 1 :
strongly limited Forward && Reverse
limiting vbi-vei
limiting vei-vs
limiting Vci for avalanche current
limiting vbi-vci OR vs-vci

=> type 2 :
limiting vbi-vei : strongly limited Forward
limiting vei-vs : weakly limited F && R
limiting Vci : weakly limited F && R
limiting vbi-vci OR vci-vs : str limited Forward

2.2 Models (from 2006 Verilog A code) :

=> all with 5 External nodes ...
=> to have fair time simulations comparisons,
also not using the feature : "V(a,b) <+ exp ;"
in all the new HICUM Verilog A code
(some slight modification done)

=> HICUM level 0 : hicumL0V1p11 ::> HIC206
=> HICUM level 2.1 : hicumL2V2p11 ::> HIC216
=> HICUM level 2.2 : hicumL2V2p21 ::> HIC226
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3- Circuits and Parameters sets to test each models

=>VSRC .CIR : 1 VSRC controling each C,B,E,S

=> ISRC .CIR : ISRC controling DIODE (C,B),(E,S)

=> 21 stages ECL RING Oscilator (ST test circuit ...)

=> 2 Valim : - 2.7 V && - 5.2 V

=> 3 Tail currents :

=> Not saturated : 620 ohms / 1240 ohms

=> Saturated : 620 ohms / 620 ohms

=> Hard saturated : 620 ohms / 400 ohms

=> bandgap cir

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4- Simulations Results

SUMMARY of results : on request , data are available to allow your own validations && verifications ...

(Self Heating ON && 5 ext nodes : except for GUMMEL-POON)

HIC203 (2005) : HICUM Level 0 + Limiting Functions type = 1

HIC2125 (2005) : HICUM Level 2.1 + Lim Functions type = 1

HIC213 (2005) : close of HICUM Level 2.1 + Lim F type = 1

HIC223 (2005) : HICUM Level 2.2 + Lim Functions type = 1

HIC206_1 : HICUM Level 0 + Limiting Functions type = 1

HIC206_2 : HICUM Level 0 + Limiting Functions type = 2

HIC216 : HICUM Level 2.1 + Limiting Functions type = 1

HIC226_1 : HICUM Level 2.2 + Limiting Functions type = 1

HIC226_2 : HICUM Level 2.2 + Limiting Functions type = 2

HIC226_3 : HICUM Level 2.2 + Limiting Functions type = 2
Optim : gcc -O2

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COMMENTS :

4.1- Slight modification in the VERILOGA code of new HICUM model (to speed up simulation time) ...

4.2- MEXTRAM 504.6 (from Veriloga) model
=> low Number of iteration (DC && TRAN)

4.3- VBIC 1.2 (from Veriloga) model
=> low Number of iteration (DC && TRAN)

4.4- All HICUM model gives close numerical results (DC && TRAN) from those previous 2005 VERILOG A codes

4.5- All HICUM model gives better time simulations results (DC && TRAN) from those previous 2005 VERILOG A codes

4.6- HICUM Level 0 model is a lot improved : time simulations results (DC && TRAN) decreased by a factor around 5 (from 2005 VERILOG A code)

4.7- All HICUM model gives low Number of iteration (DC && TRAN) (as it is now in my SPICE from 2005 VERILOG A code) ...

4.7.1 BUT a relatively High loadTime , as compared to the GUMMEL-POON (note: GUMMEL-POON is without self-heating)

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4.7.2 BUT a relatively lower loadTime as compared to the MEXTRAM 504.6

4.7.3 BUT a relatively lower loadTime as compared to the VBIC 1.2

4.7.4 BUT a same kind of loadTime , as compared to the 1rst HICUM 2.1 from 2002 FORTRAN one's ...

4.7.5 HICUM Level 0 model is faster as HICUM Level 2.2 model (around 30% less on loadTime)

4.7.6 more , You may save 30% less on loadTime : by compiling using optimisation option : gcc -O2

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note :

=====

1=> It is difficult , and very often not fair , to compare TRAN simulation times when using different models in the same circuit , when the transistor are saturated ... because this TRAN simulation times is very dependant of the saturation level ... that means that is in fact a lot dependant of the used set devices parameters of the transistors , when saturated ... (ie : I have not , for a same type of process transistor, the equivalent set of parameters for all model to be simulated ...)

2=> NEW « HICUM Level 0 » is around 5 Times faster : Why ?

Mainly (to be compatible to ADMS VerilogA Compiler) :

New VerilogA code uses ONLY MACRO's instead of VerilogA Functions ... resultings in :

=> less C codes ... (for calling parameters ... etc)

=> Optimisations possible ...

=>1 Macro's Call instead of 2 VerilogA Functions Call ... (values of Charges && Capa ...)

NEW « HICUM Level 2.1 » is around 3 Times faster : Why ?

Again ... Mainly :

New VerilogA code uses ONLY MACRO's instead of VerilogA

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5- Remaining Works ...

=> Noise Analysis ...

=> remaining features : "idt ()"

=> How to introduce the Limiting functions needed when Strongly no linear model ??

=> Spice Verilog A Compiler for HP workstation under HPUX

6- Other Developments :

=> a lot of new features & improvement for Spice3F5

- **Spice driven from schematic ...**
- **Subckt Parameters**
- **Process Block (Model Params function of Process Params)**
- **Spice Libraries Compiled**
- **TCLTK compatible**
- **New Spice RF :**
  - **S parameter Analysis & port + nport**
  - **New Harmonic Balance Analysis :**
    - **HB : 1 forced frequency Steady State**
    - **QB : Quasi Periodic 2 forced frequencies Steady State**
    - **CE : Circuit Envelope 2 forced frequencies Transient Time domain**

=> ATELECAD kit : (TCLTK compatible)

=> schematic capture (SPICE driven by schematic capture ...)

=> logic simulation

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7- CONCLUSIONS :

7-1 Simulation Results && Comparisons for new Models , introduced into SPICE (from 2006 Verilog A code) :

=> HICUM level 0 : hicumL0V1p11 ::> HIC206
=> HICUM level 2.1 : hicumL2V2p11 ::> HIC216
=> HICUM level 2.2 : hicumL2V2p21 ::> HIC226
=> MEXTRAM level 504 .6 ::> TS5046
=> VBIC level 1.2 (ADMS) ::> VBIC126

Have been presented and demonstrated ...
********** **********

(freely available on request to validate your own simulators)

7-2 a Straight-forward Stand Alone Validation Method of HICUM Models
Have been presented and demonstrated ...
********** **********

(freely available on request to validate your own simulators)

7-3 New versions of HICUM models give very good behaviour and low Time Simulations results ...

(better results than MEXTRAM 504.6 and VBIC 1.2)

7-4 All Technologies developed into this SPICE can be transferred to other simulators ...
To negotiates Licences , please contact :

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NEW SPICE HICUM Model Validation Steps

1- Verilog A Model compiler Validation 2005 :

1.1 using specific some C stand alone :

for values && numerical derivatives calculation

1.2 Simulation results compared to those using other tools

ex : CADENCE Verilog A Model compiler

(in OP and AC : 7 identical digits)

(for HICUM modeles && MOS EKV 2.6)

2- Verilog A Model compiler Validation 2006 :

2.1 using new Verilog A Model compiler 2006 :

=> recompile previous HICUM modele 2005 (level : 0, 1.1

=> checked that C code are identical

=> also behaviour && numerical Simulations results are identical

2.2 using NEW specific C stand alone executable :

for values numerical OP values : (HICUM level 2.2)

=> introduces Voltages nodes that comes from the simulator to be checked ...

=> the executable computes the currents at transistors nodes

=> then compare to simulators results ...

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GUMMEL-POON	HIC203	HIC2125	HIC213	HIC223	HIC206_1	HIC206_2	HIC216	HIC226_1	HIC226_2	HIC226_3	TS5046	VBIC126
VSRC												
OP	6	9	8	8	8	9	9	8	8	8	10	6
DC	23	47	35	41	43	47	43	41	43	38	45	46
ImpOP	4	10	5	10	10	10	6	10	10	5	7	9
TRAN	594	628	607	677	579	627	607	659	579	556	831	930
AnalTime	0.01	0.41	0.05	0.27	0.11	0.116	0.112	0.154	0.114	0.111	0.171	0.216
loadTime	0.01	0.4	0.05	0.24	0.08	0.0819	0.0799	0.1099	0.0769	0.0819	0.131	0.164
ISRC												
OP	11	10	10	11	11	10	10	11	11	11	11	11
DC	66	84	178	82	85	82	86	82	85	85	86	86
ImpOP	26	26	24	25	25	24	24	25	25	24	26	25
TRAN	539	620	569	641	627	614	613	640	627	624	646	583
AnalTime	0	0.43	0.1	0.39	0.15	0.123	0.119	0.183	0.143	0.131	0.177	0.159
loadTime	0	0.42	0.1	0.36	0.15	0.0909	0.0859	0.1389	0.0989	0.0959	0.120	0.1119

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NO SAT												
ECL Ring Osc												
Valim = 2.7 V												
OP	6	10	8	13	11	10	9	13	11	8	8	8
ImpOP	323	34	11	32	29	34	15	33	29	8	8	17
TRAN	2428	3005	6871	3411	3842	2983	2567	3329	3841	3653	4561	6673
AnalTime	1.84	107.42	28.71	96.96	41.72	22.331	19.12	34.715	31.648	30.180	42.04	70.35
loadTime	0.9	103.52	26.27	94.19	39.21	21.018	18.06	32.166	28.969	27.531	38.90	58.99
NO SAT												
ECL Ring Osc												
Valim = 5.2 V												
OP	9	26	11	28	28	26	9	28	28	8	7	9
ImpOP	(G40)309	52	12	50	52	52	14	51	52	15	10	12
TRAN	2515	3133	7769	4912	4714	3093	2504	3737	4438	4273	4126	7264
AnalTime	2.16	112.85	32.35	140.24	51.52	23.078	18.639	39.191	37.106	35.912	39.51	77.60
loadTime	0.83	108.20	29.53	137.17	48.07	21.778	17.578	36.298	33.912	32.648	34.99	65.14

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SAT													
ECL Ring Osc													
Valim = 2.7 V													
OP	8	17	12	20	17	17	17	20	17	13		9	11
ImpOP	(G40)323	34	14	32	29	34	14	33	29	16		13	8
TRAN	15321	6843	6791	5986	16970	6741	5677	5515	16510	13153		14102	30429
AnalTime	8.94	244.53	28.54	163.65	191.02	50.216	42.629	57.87	139.42	111.16		128.97	317.91
loadTime	4.45	233.63	25.68	159.04	178.87	47.587	40.292	53.30	127.68	102.7		114.80	265.84
SAT													
ECL Ring Osc													
Valim = 5.2V													
OP	8	23	11	26	26	23	10	26	26	10		9	10
ImpOP	326	52	13	50	52	52	13	51	52	15		12	8
TRAN	10657	8899	8118	6393	14323	8888	8181	6375	14317	12204		14045	29374
AnalTime	7.62	315.37	33.9	177.31	57.82	65.74	59.008	65.784	120.33	102.13		131.90	307.13
loadTime	3.36	302.03	30.69	173.40	147.91	62.301	56.747	61.159	109.99	94.19		117.12	257.93

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HARD SAT			10.2 per				9.5 per					
ECL Ring Osc												
Valim = 2.7 V												
OP	17	21	17	23	22	21	19	23	22	16	16	19	11
ImpOP	323	33	14	32	30	33	13	33	30	16	16	15	16
TRAN	13408	9578	11340	11670	17198	9594	8554	8939	18302	16961	16853	23580	44734
AnalTime	8.25	339.45	49.24	333.86	191.72	70.60	64.745	94.787	151.69	140.48	102.173	216.88	476.67
loadTime	3.73	324.07	44.98	324.77	179.43	67.07	60.473	87.977	138.86	128.20	91.53	191.88	402.45
HARD SAT												
ECL Ring Osc												
Valim = 5.2V												
OP	8	22	11	23	22	22	17	23	22	11	11	9	11
ImpOP	326	51	14	50	53	51	12	51	53	15	15	14	16
TRAN	12663	7579	9272	9627	15499	9797	8833	10432	15185	12729	12616	25920	40730
AnalTime	8.85	278.31	40.16	277.11	175.60	71.41	64.492	109.79	130.08	109.27	79.93	246.54	416.89
loadTime	4.08	275.58	36.99	270.55	163.34	67.70	60.989	101.51	116.27	99.38	69.57	215.62	348.839