Device sizing and design optimization

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OUTLINE

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- Process Optimization
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Introduction

- highly competitive semiconductor industry
  => need to reduce time-to-market and increase yield

- cycle time reduction can be achieved by
  - device optimization during process development guided by circuit design feedback
  - circuit optimization based on accurate (physics-based) modeling, incl. device design freedom

  => concurrent engineering: simultaneous process development and circuit design

- link compact device modeling to circuit design and process optimization
  - use predictive modeling capability
  - add generic device sizing method based on lateral *and* vertical technology parameters
  - establish figures of merit (FoMs) related to device and circuit performance

  => optimizer

Optimization methods

- available optimization algorithms:
  - Nelder-Mead simplex method (can converge at local extremum)
  - combined with simulated annealing (search for global extremum)

- FoMs are directly calculated by TRADICA to ensure low simulation time

- FoMs are used as optimization targets (*single* or *joint* FoM)

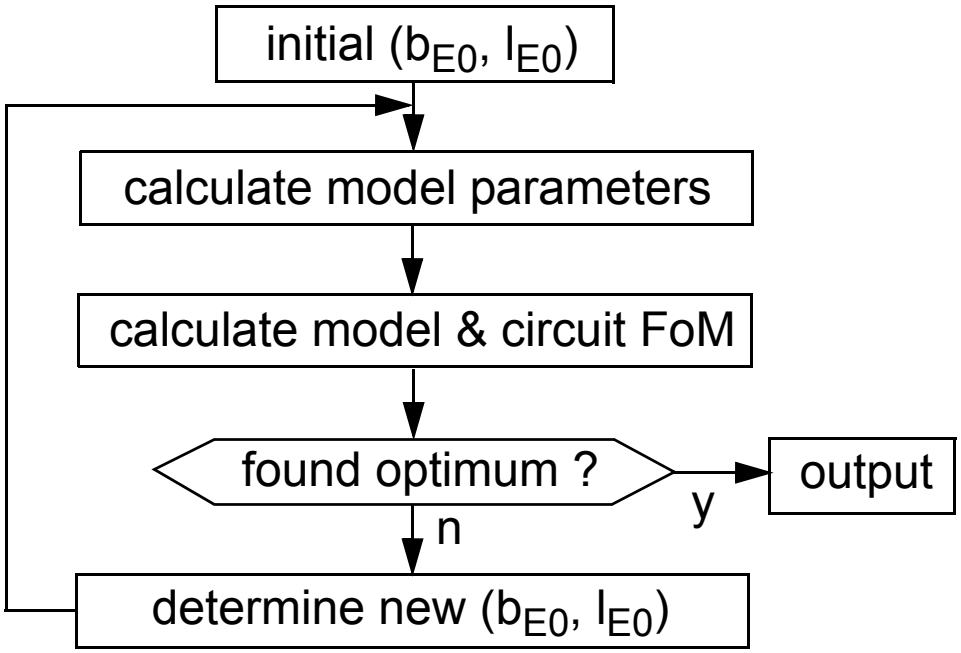
- *joint* FoM: properly arranged (non-)weighted product of single FoMs

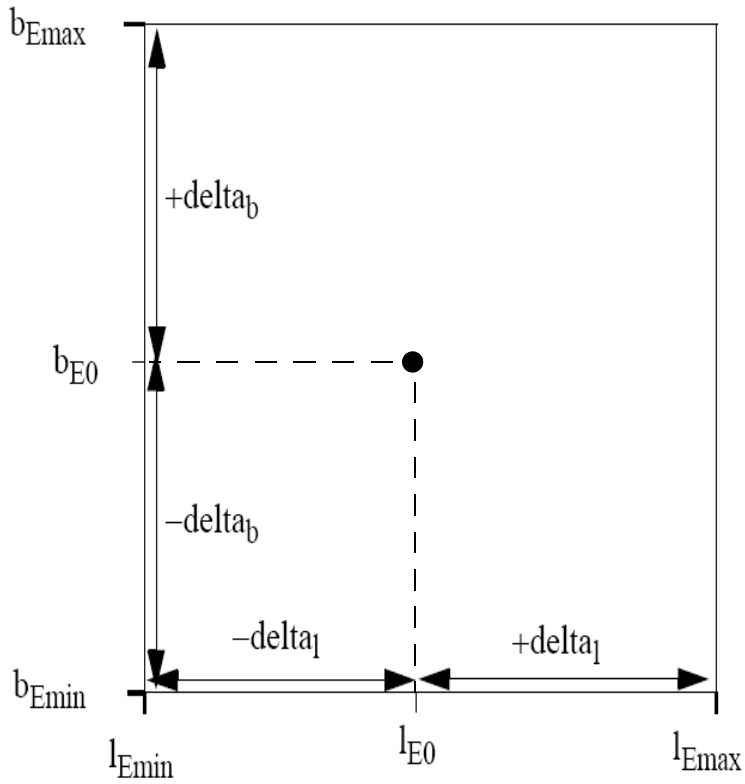
- 2 optimization types:
  - process optimization (max. 14-dimensional)
  - circuit optimization (max. 2-dimensional)

Circuit Optimization via sizing

- only emitter width and/or length can be optimized

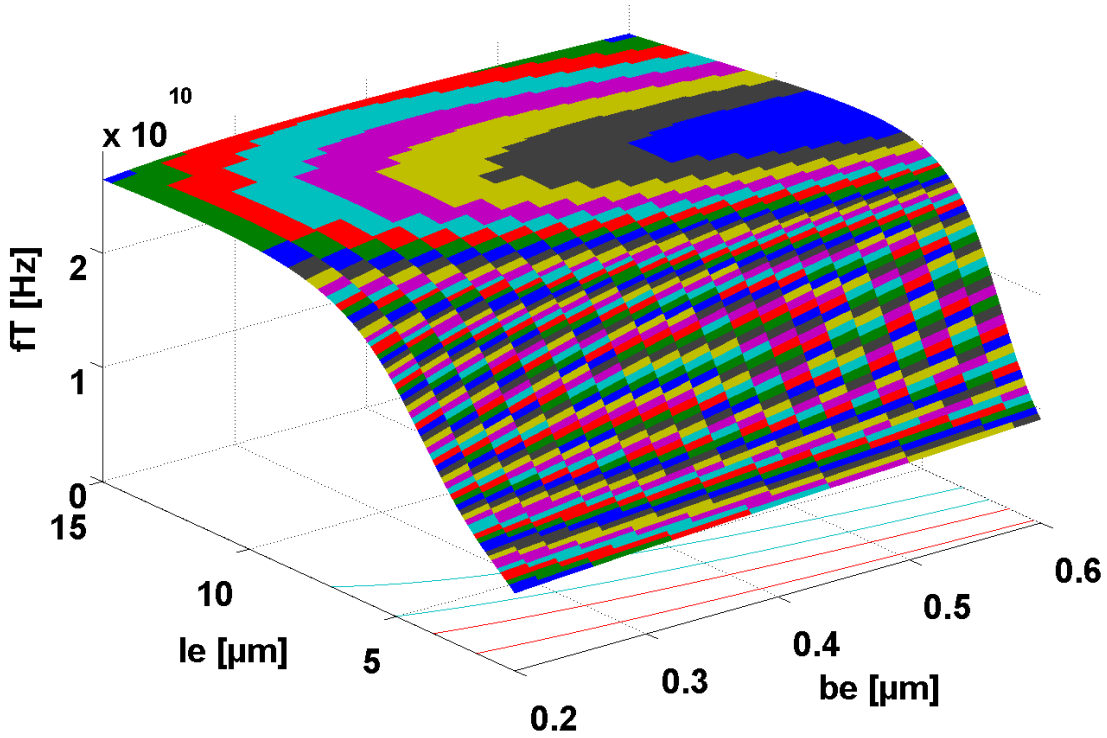
- range is user specified
  - initial values = nominal values
  - FPTOL*delta < "nominal" value





Examples: Sizing for optimum FoM value

transit frequency fT vs. emitter dimensions

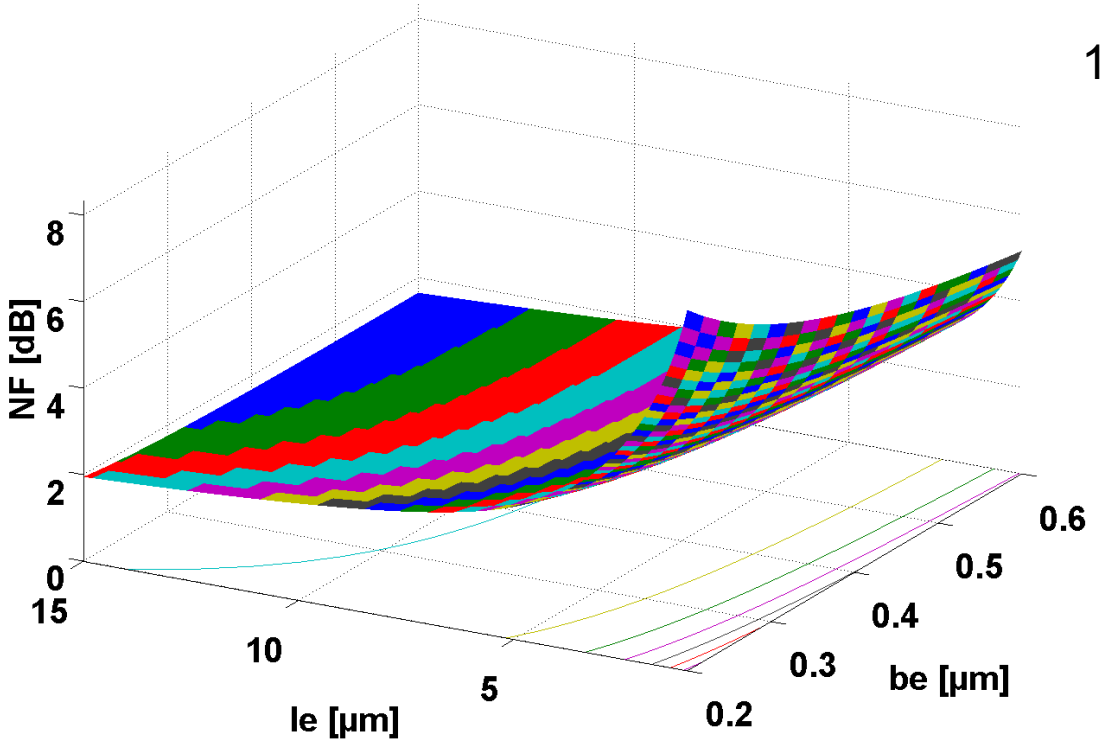


Extremum of type max of FoM fT, spot = 28.94 GHz reached at:

bE0_opt = 0.60µm and lE0_opt = 6.84µm

Examples: Sizing for optimum FoM value (cont'd)

noise figure NF vs. emitter dimensions

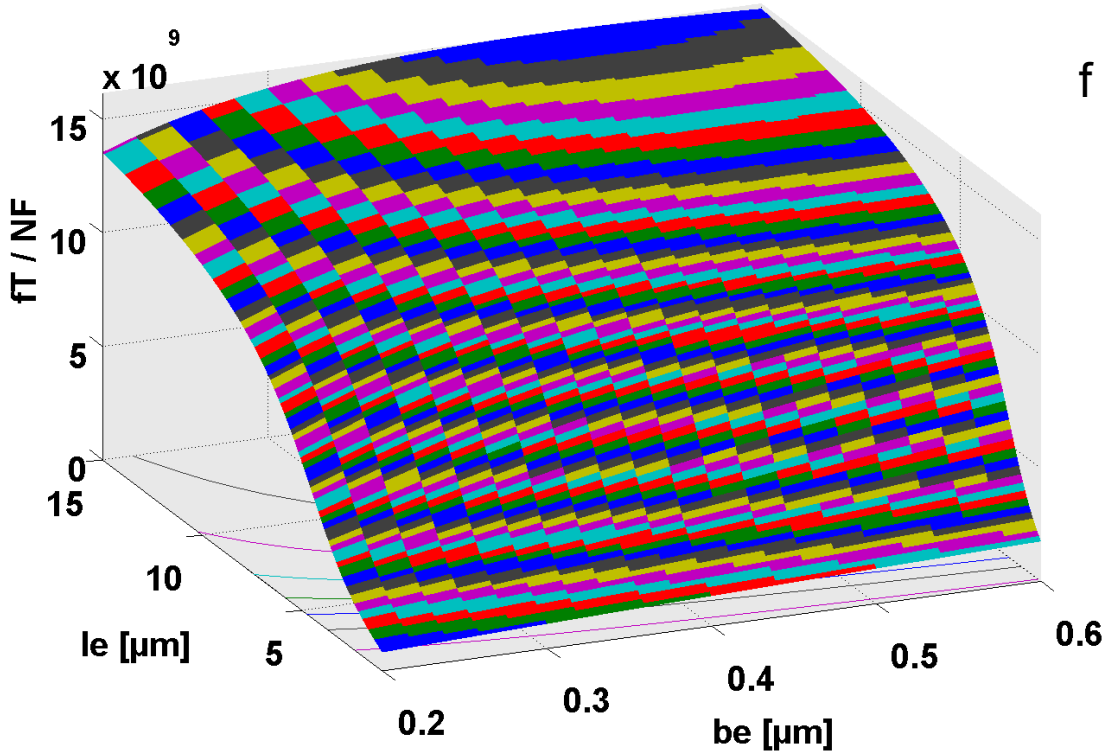


Extremum of type min of FoM NF, spot = 1.76 reached at:

bE0_opt = 0.60µm and lE0_opt = 15.00µm

Examples: Optimum joint FoM

joint fT and NF vs. emitter dimensions



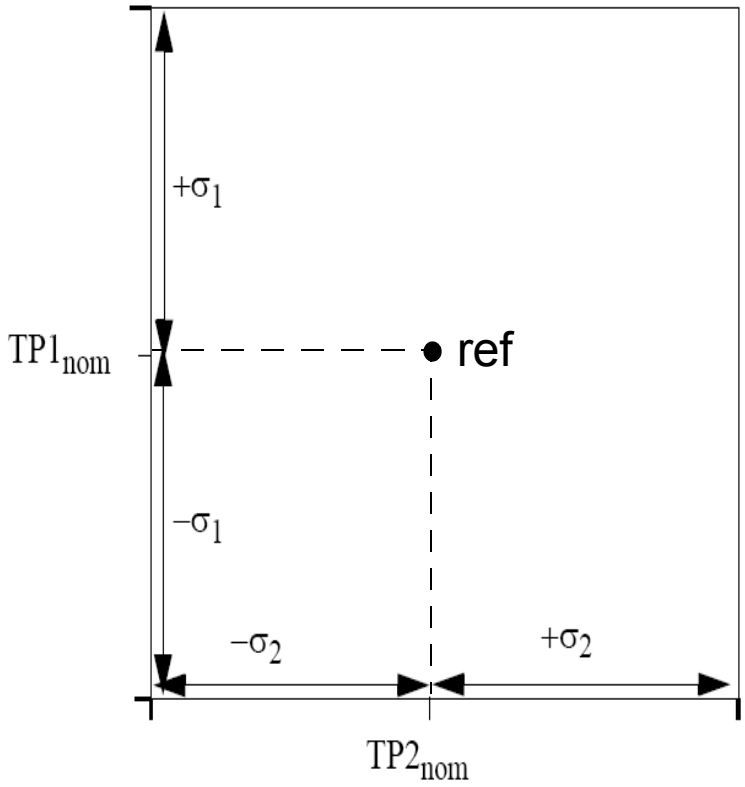
f = 1GHz

Extremum of type joint FoM (max. fT and min. NF) reached at:

bE0_opt = 0.48µm and lE0_opt = 15.00µm

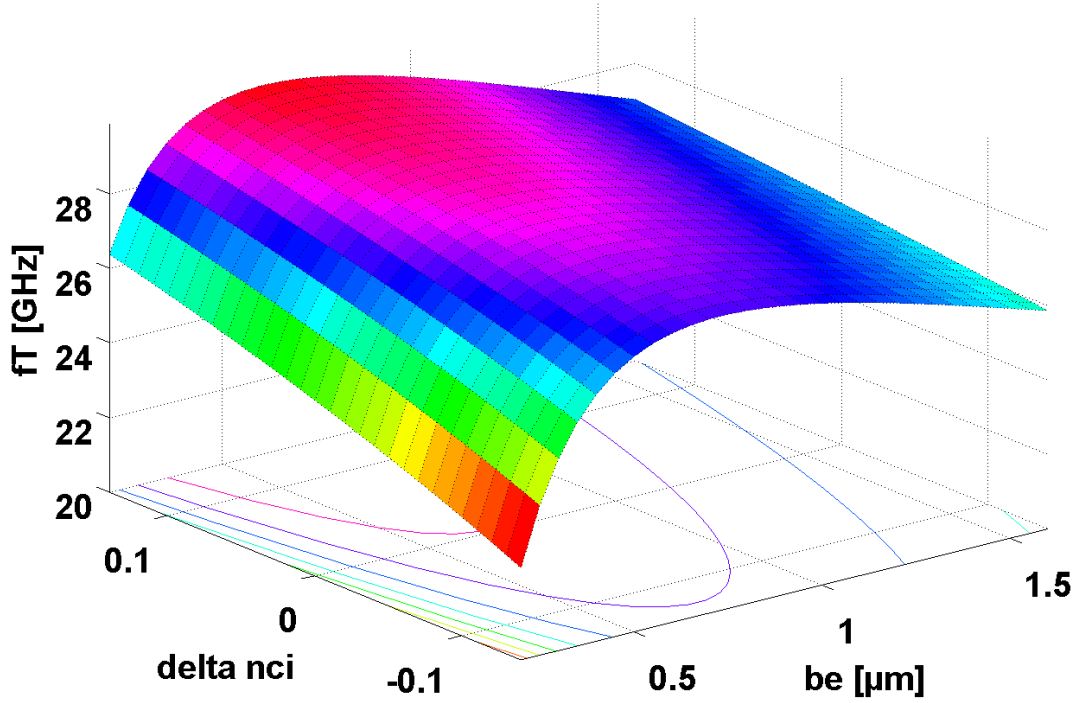
Process Optimization

- only useable if the DTA file originator password is known
- process performance is associated with a reference device configuration and then optimized
- all technology parameters (TPs) are accessible
- nominal value and standard deviation in technology definition
- depending on TP: standard deviation can be relative or absolute
- standard deviation can be altered in the technology definition or scaled by weighting factors and FPTOL



Examples: Sizing for optimium FoM value

transit frequency fT vs. emitter width b_{E0} and internal collector doping conc. N_{Ci}

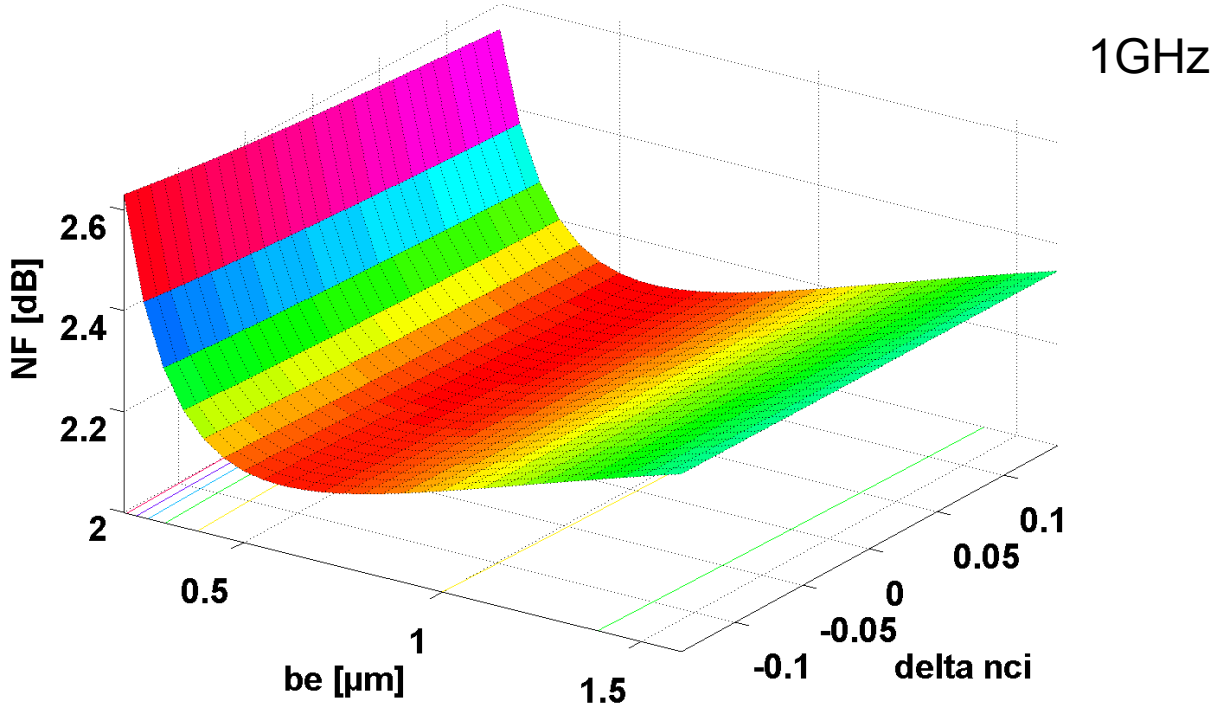


Extremum of type max of FoM fT, spot = 29.89 GHz reached at:

nci_opt = 1.14 and bE0_opt = 0.61µm

Examples: Sizing for optimium FoM value (cont'd)

noise figure NF vs. emitter width b_{E0} and internal collector doping concentration N_{Ci}

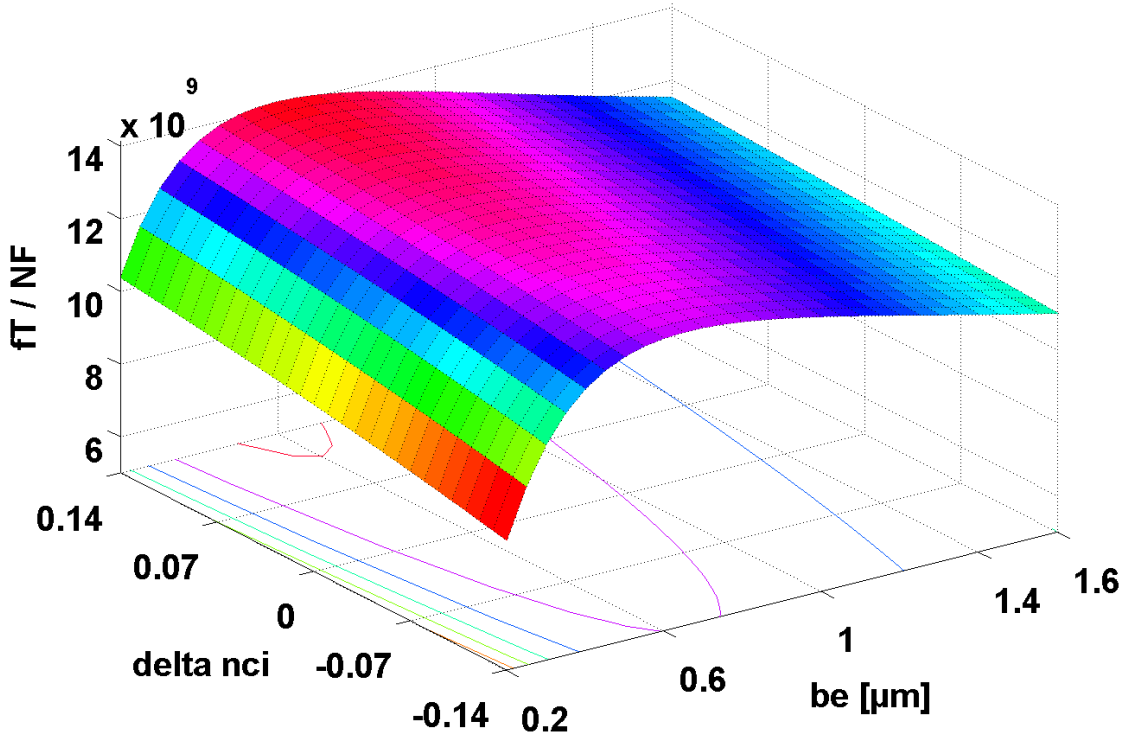


Extremum of type "min of FoM fT", spot = 2.10 reached at:

nci_opt = 1.14 and bE0_opt = 0.59µm

Examples: Optimum joint FoM

joint fT and NF vs. emitter width b_{E0} and internal collector doping concentration N_{Ci}

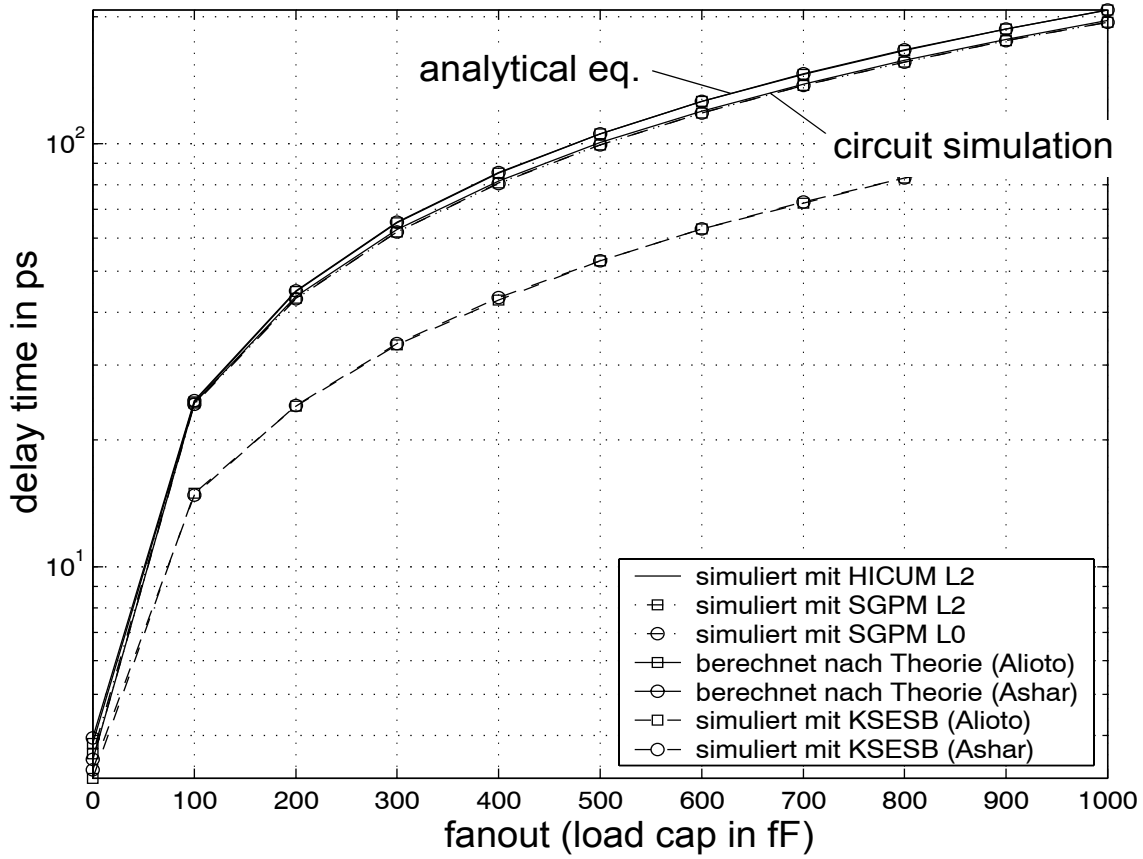


Extremum of type joint FoM (max. fT and min. NF) reached at:

nci_opt = 1.14 and bE0_opt = 0.60µm

Circuit related FoMs

ECL gate delay time vs fanout (fixed tail current)



$t_D(b_{E0}, I_{E0}, N_{Ci}, ...)$

- indication of process performance for "digital" circuits

- similar accuracy found for analytical description of cascode LNA gain(frequency)

Conclusion

- device sizing and optimization based on single and joint FoM

- sizing serves as design aid (no circuit simulator required)
  => initial solution for further circuit optimization by
  - designer
  - automated optimization software (NeoLinear, Wicked)
    (originator password protects confidential technology information in TRADICA DTA file)

- device design optimization enables focused process development

- goal: add more circuit design related FoMs for important building blocks