Improved methodology for modeling the Parasitic Substrate PNP without access to the substrate terminal

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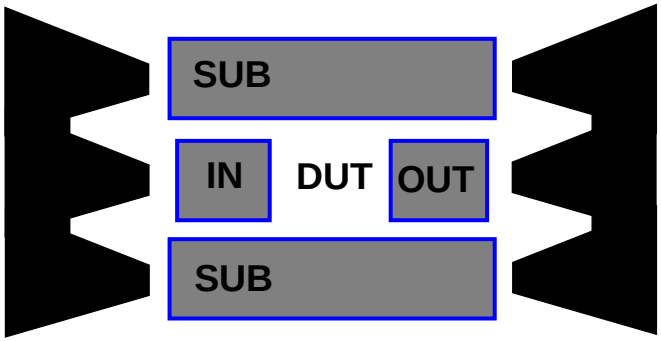
Franck Pourchon, Didier Céli and Christian Raya

Outline

- **Introduction and motivation of this work.**
- **Substrate PNP: where is it located?**
- **Why Substrate PNP needs to be modeled?**
- **First proposal for parameters extraction and limitations (CMRF 2005).**
- **Improved method for parameters extraction and experimental results.**
- **Conclusion.**

Motivation of this work (1/2)

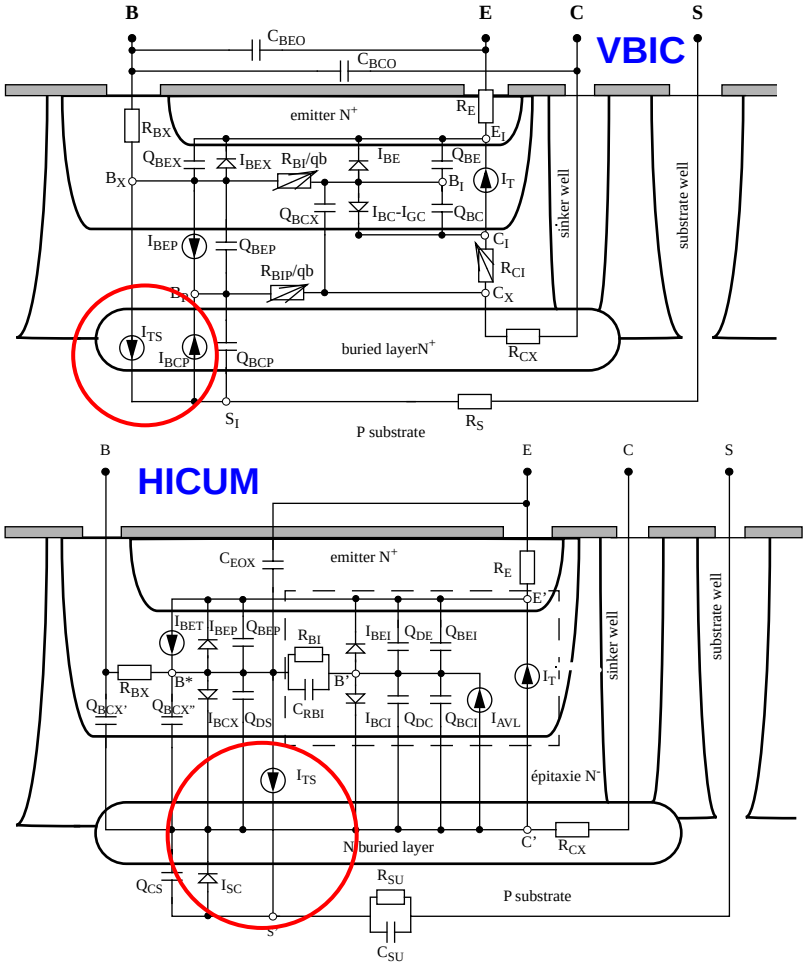
- Bipolar device modeling requires most of the time DC+HF measurements.
- For HF measurements dedicated test structures are layouted, compatible with HF coplanar probes:



- Common-Emitter configuration, HF probes shorten Emitter and Substrate terminal, no way to measure the substrate current!
- To avoid the duplication of test structures (DC+HF structures for each transistor geometries) and duplication of measurements (DC+HF measurements), measurements on HF structures have to be used to model the parasitic PNP.
- In addition, it ensures that HF modeling and parasitic DC modeling will be done on measurements coming from the same transistor!

Motivation of this work (2/2)

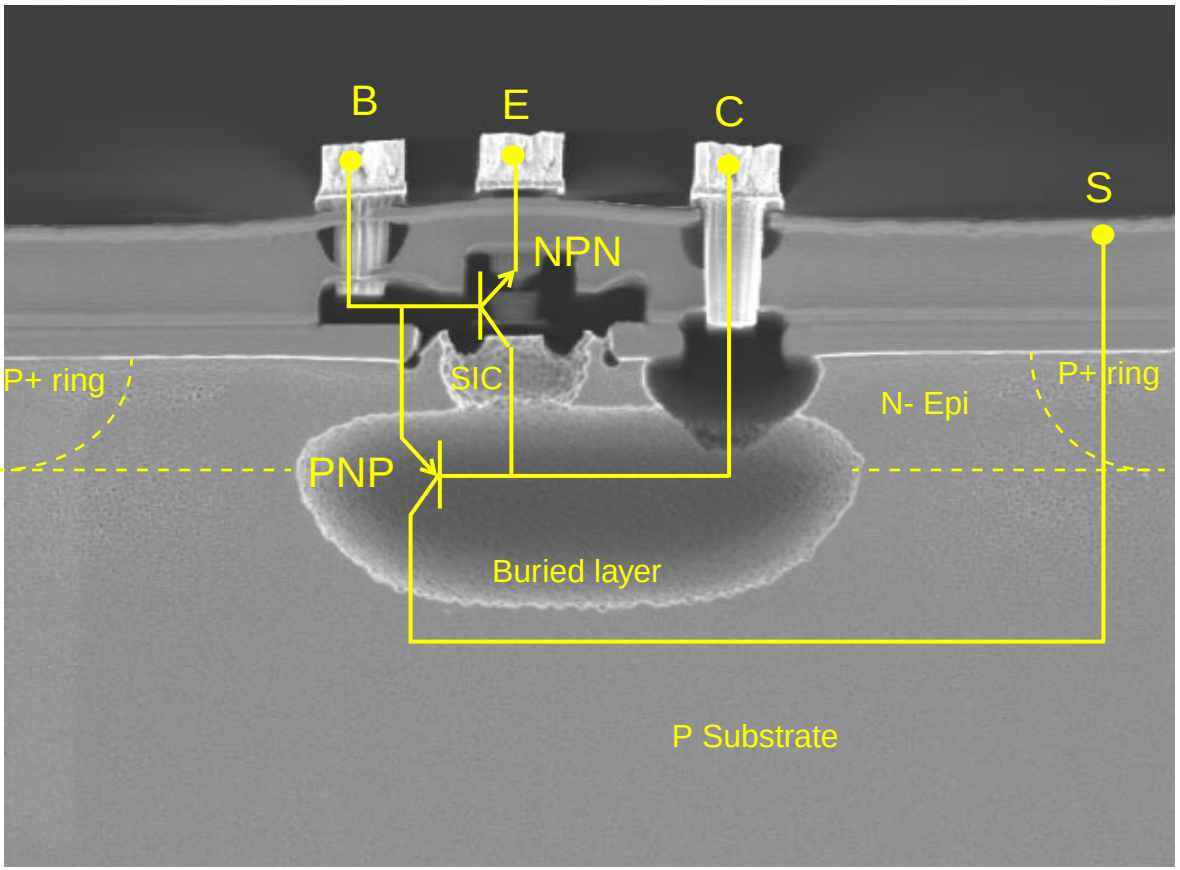
- All modern bipolar models include substrate parasitic currents description!



- A model independent method is proposed to extract these parameters.

Substrate PNP in junction isolated technologies

- Outline
- Introduction
- Where is located the Substrate PNP?
- Why the SPNP needs to be modeled?
- First method description
- Improved method description
- Conclusion



Substrate PNP in deep-trench isolated technologies

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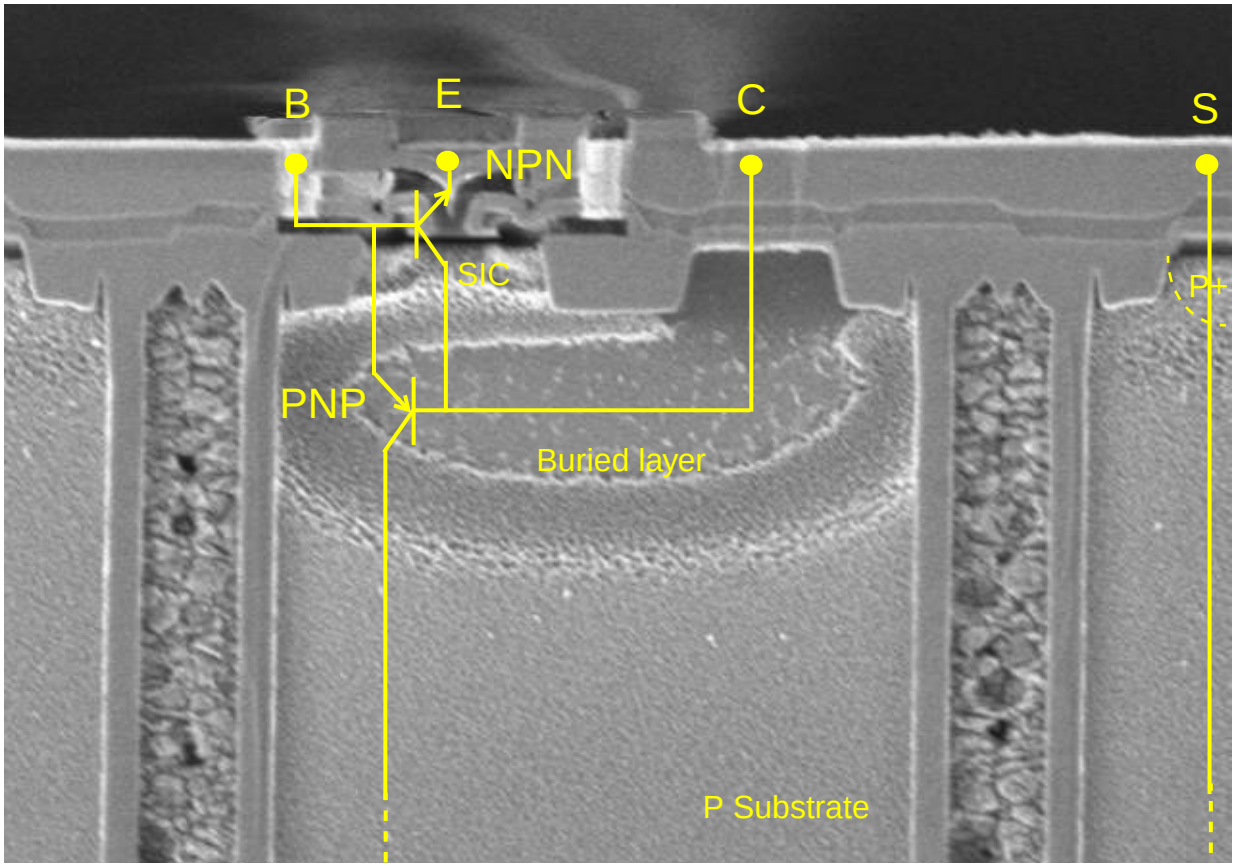
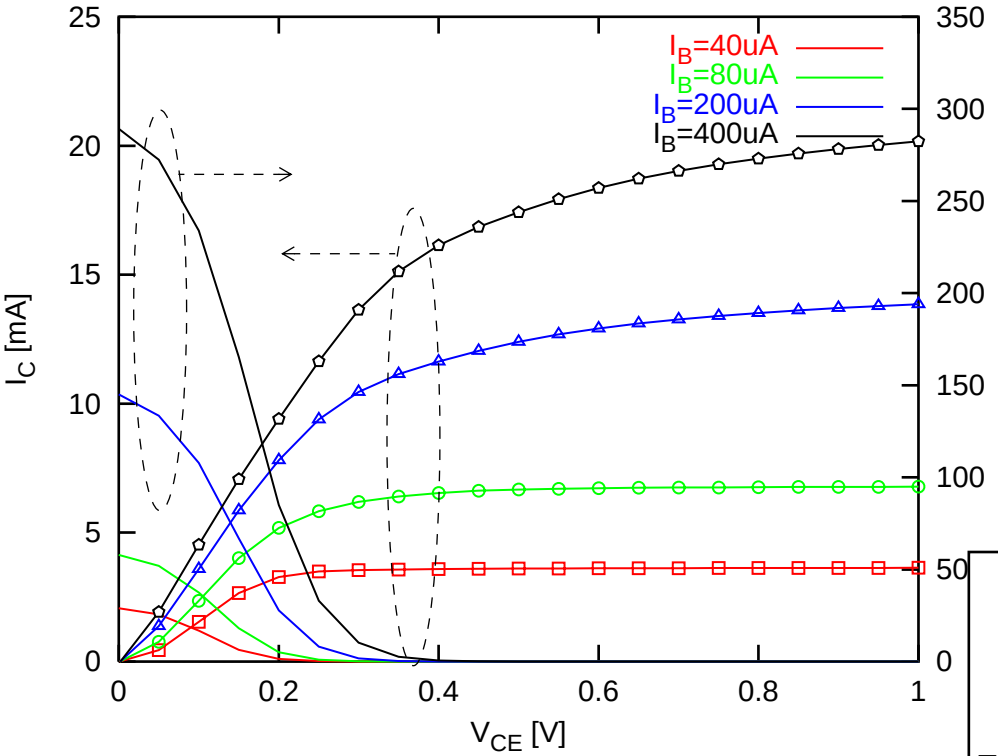


Why the Substrate PNP needs to be modeled?

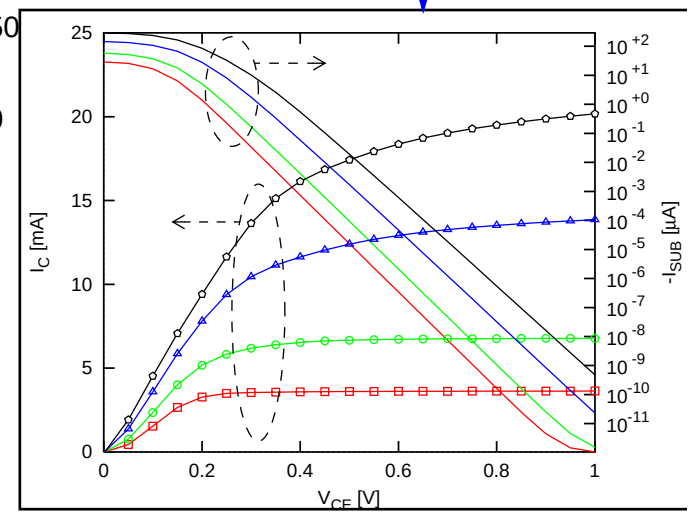
❒ The substrate current is triggered by saturation mode:



Output characteristics: (I_C, I_{SUB}) versus V_{CE}

I_{SUB} in lin scale

I_{SUB} in log scale



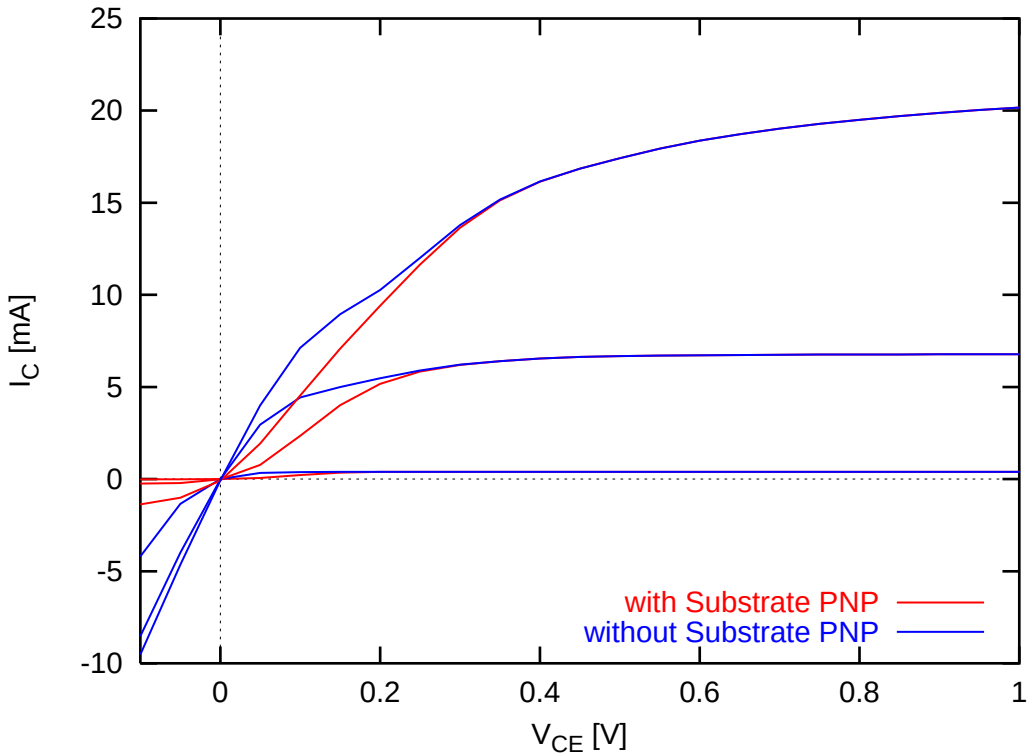
Output characteristics for low V_{CE}:

$V_B > V_C$ the BC junction is forwarded

=> the Substrate PNP is switched on!

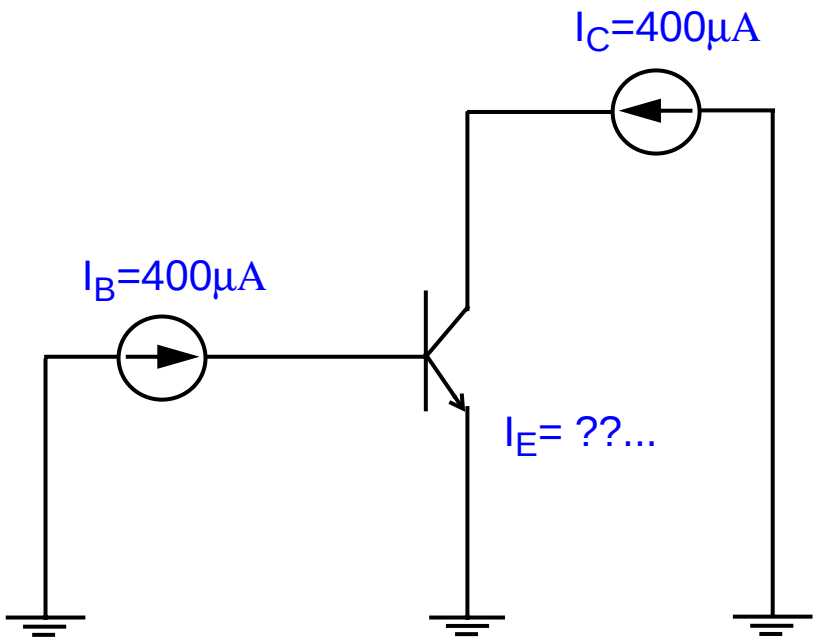
Why the Substrate PNP needs to be modeled?

- The substrate current impact could be seen in the I_C ramp-up in the output characteristics:



Why the Substrate PNP needs to be modeled?

- Forced gain characteristics:



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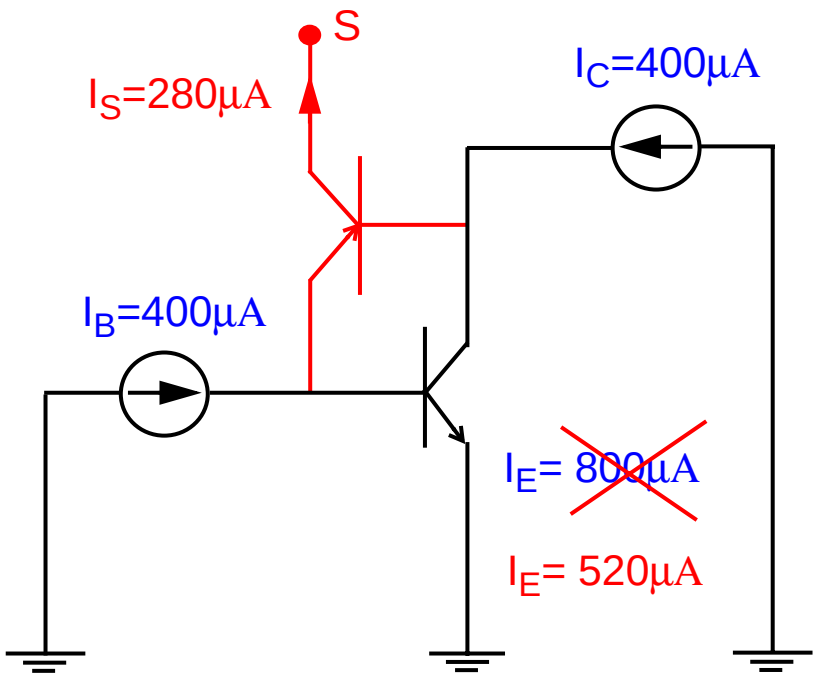
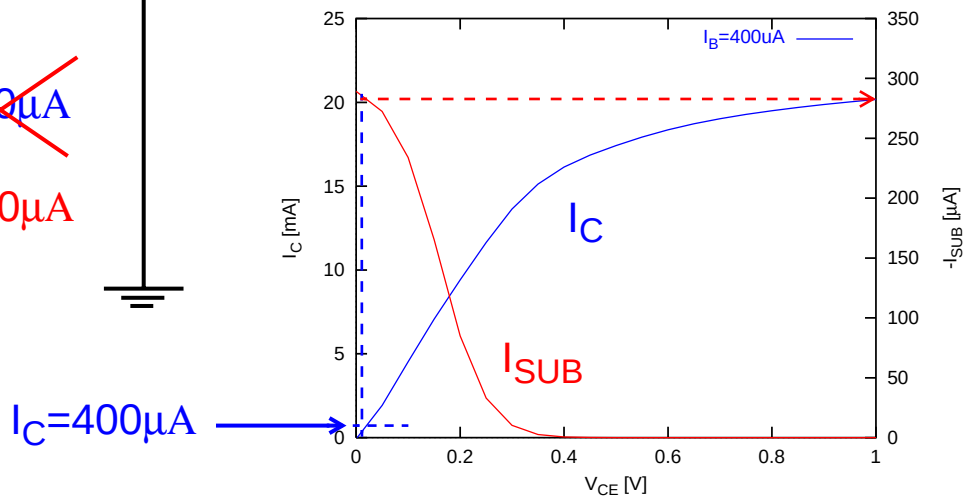
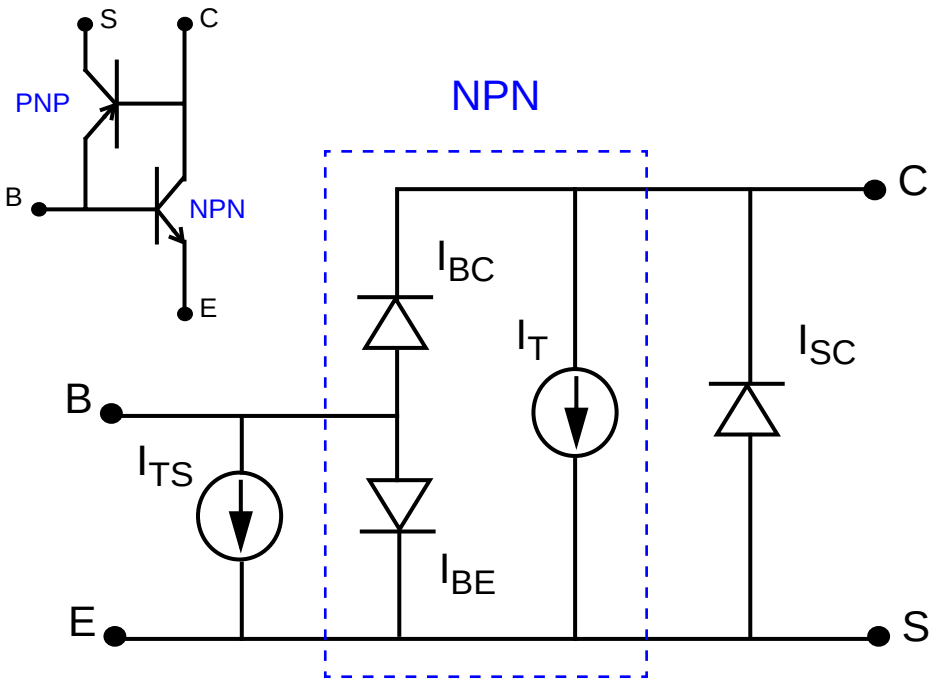
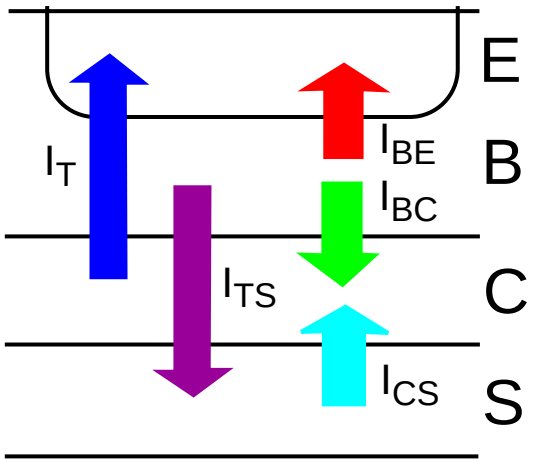




First method description (1/3)

- Common Emitter-Collector configuration:
  - Low current: series resistances neglected, no high-injection effects.
  - The Substrate PNP is modeled with first order model (simple voltage controlled current source without Early effects, high-injection effects, series resistances, etc...), the Collector-substrate junction is modeled with a diode:



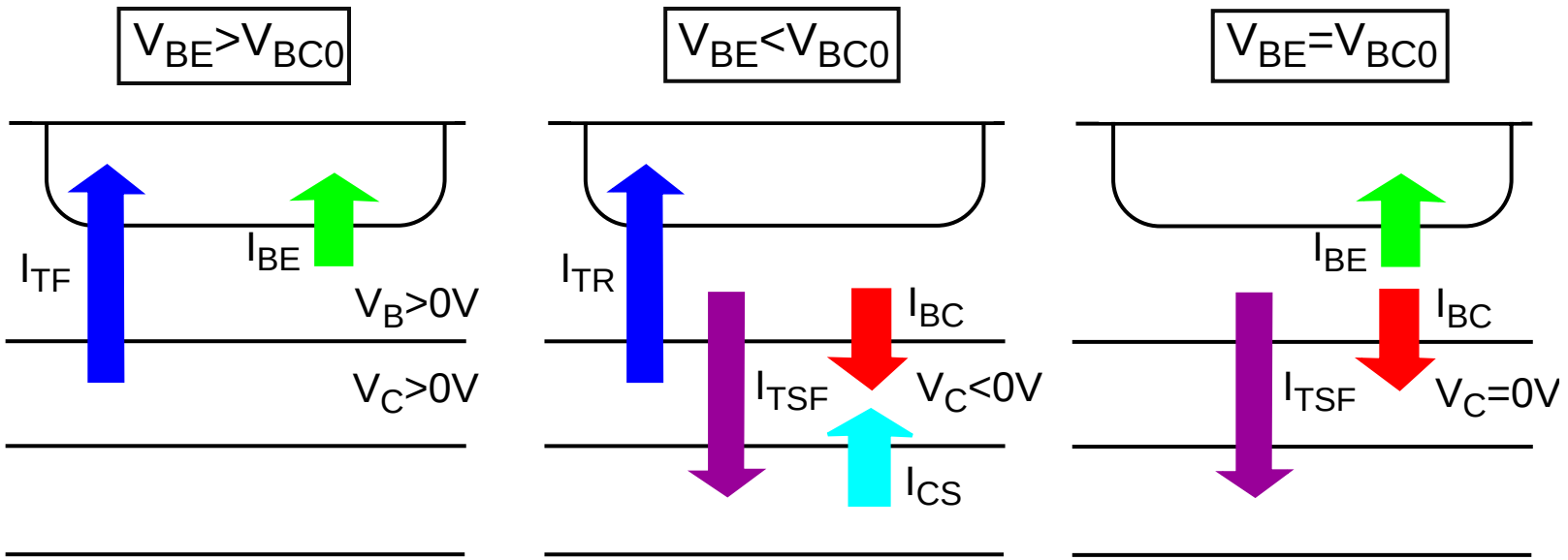


$$I_C = I_T - I_{BC} - I_{SC} \text{ and } I_B = I_{TS} + I_{BE} + I_{BC} \quad (1)$$

First method description (2/3)

- $I_T = I_S \cdot \left(\exp\left(\frac{V_{BE}}{V_T}\right) - \exp\left(\frac{V_{BC}}{V_T}\right) \right)$ and $I_{TS} = I_{TSS} \cdot \left(\exp\left(\frac{V_{BC}}{V_T}\right) - \exp\left(\frac{V_{CS}}{V_T}\right) \right)$

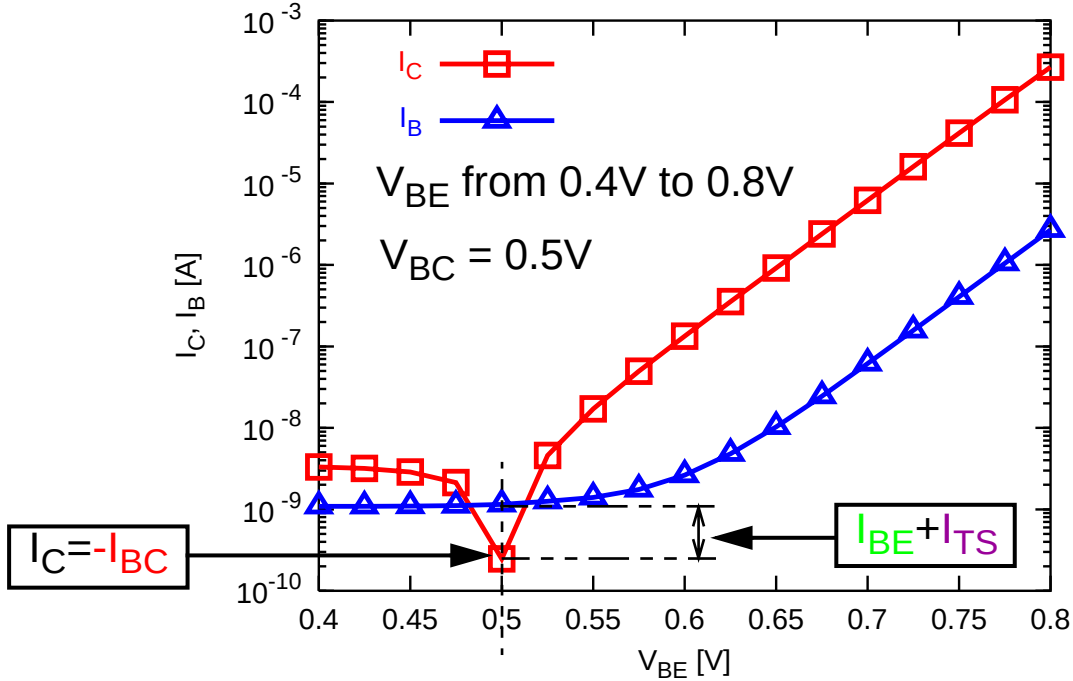
- Saturation mode $V_{BC}=V_{BC0}>0$ (Emitter and Substrate are grounded):



- $I_B = I_{BE}(V_{BE})$
- $I_C = I_{TF}(V_{BE})$
- $I_B = I_{BC}(V_{BC0})+I_{TSF}(V_{BC0})$
- $I_C = I_{TR}(V_{BC0})-I_{BC}(V_{BC0})-I_{CS}$
- $I_B = I_{BC}(V_{BC0})+I_{BE}(V_{BE})+I_{TSF}(V_{BC}$
- $I_C = -I_{BC}(V_{BC0})$

First method description (3/3)

- Practical case (0.35µm technology, with LOCOS isolation):



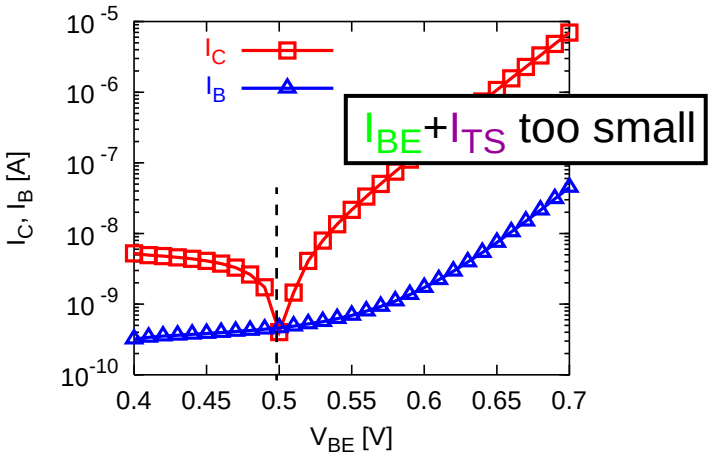
I_{TSS} = 3.246aA

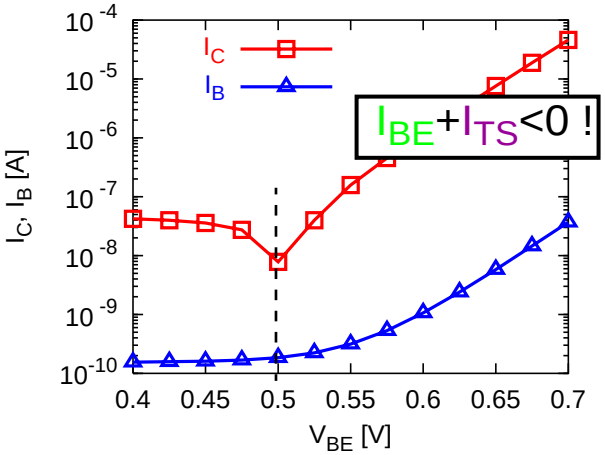
I_{BCS} = 0.993aA

- Retrieving model parameters from measurement at V_{BC0} and V_{BC}=0V:
  - $I_C(V_{BE}=V_{BC0}) = -I_{BC}(V_{BC0}) \Rightarrow I_{BCS} = I_{BC}(V_{BC0})/\exp(V_{BC0}/V_T)$
  - $I_B(V_{BE},V_{BC}=0) = I_{BE}(V_{BE})$
  - $I_B(V_{BE}=V_{BC0})=I_{BC}(V_{BC0})+I_{BE}(V_{BE})+I_{TSF}(V_{BC0}) \Rightarrow I_{TSS}=I_{TSF}(V_{BC0})/\exp(V_{BC0}/V_T)$

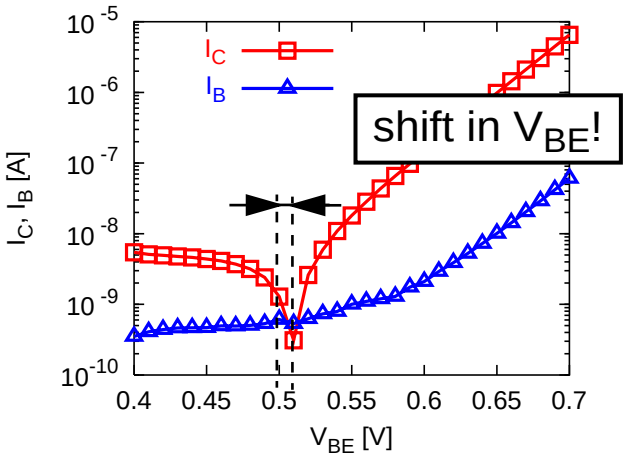
First method limitations

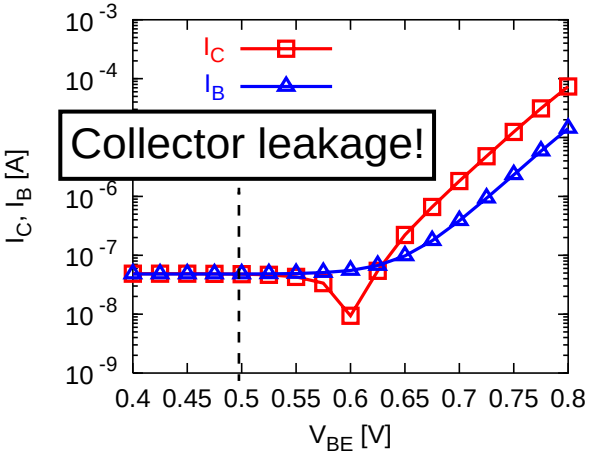
- Measurement inacuracy if substrate current is extremely low:





- Measurement issues (independant from the method):

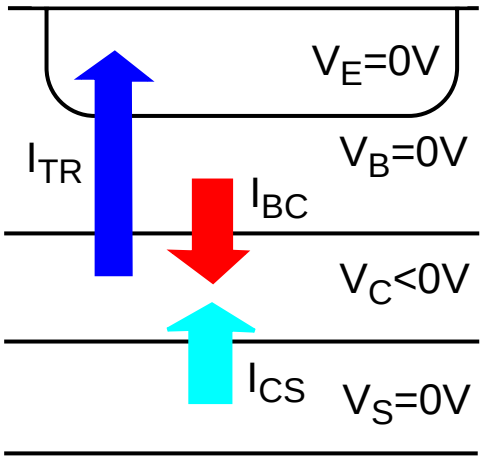




- The calculation of I_{BC} is too sensitive to the measurement precision!

Improved method description (1/3)

- Saturation mode $V_{BC}=V_{BC0}>0$ and $V_{BE}=0V$:



- $I_B(V_{BE}=0,V_{BC}=V_{BC0}) = I_{BC}(V_{BC0})$

$\Rightarrow \boxed{I_{BCS} = I_{BC}(V_{BC0})/\exp(V_{BC0}/V_T)}$

- $I_C(V_{BE}=0,V_{BC}=V_{BC0}) = I_{TR}(V_{BC0})-I_{BC}(V_{BC0})-I_{SC}(V_{SC0})$

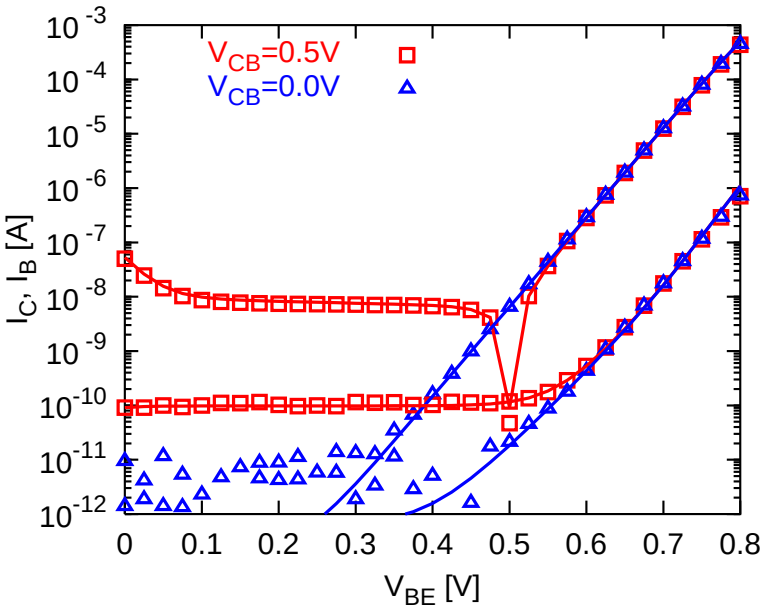
$\Rightarrow \boxed{I_{SC} = I_{SC}(V_{SC0})/\exp(V_{SC0}/V_T)}$

- $I_C(V_{BE}=V_{BC0},V_{BC}=0) = I_{TF}(V_{BE})= -I_{TR}(V_{BC0})$

- To sum-up the measurement conditions:
  - For $V_{BC}=0V$:
    - **For $V_{BE} = V_{BC}$, I_C and I_B are measured: $I_{BE}(V_{BE}=V_{BC0})$ and $I_{TF}(V_{BE}=V_{BC0})$ are known**
  - For $V_{BC} = V_{BC0}$:
    - **For $V_{BE} = 0V$, I_C and I_B are measured: $I_{BC}(V_{BC0})$ and $I_{CS}(V_{SC0}=V_{BC0})$ are known**
    - **For $V_{BE} = V_{BC}$, I_B is measured: $I_{TS}(V_{BC0})$ is known**

Improved method description (2/3)

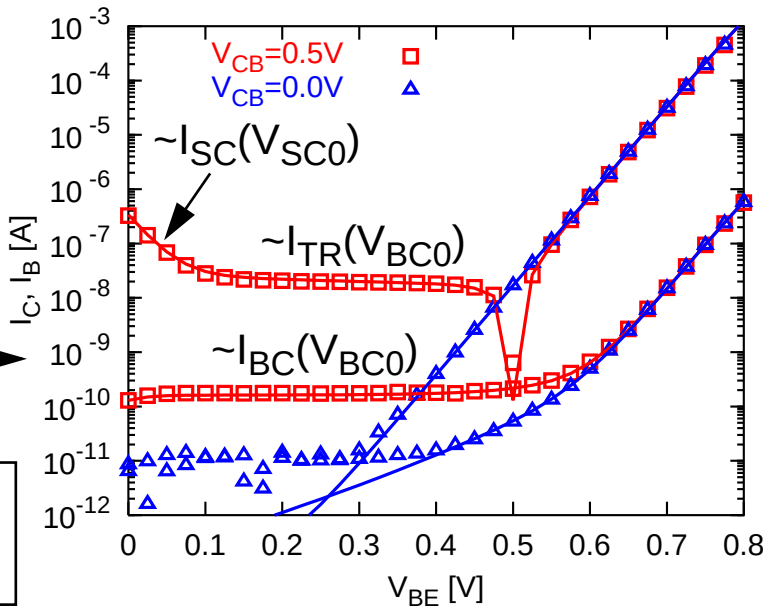
❒ Practical case:



I_{TSS} = 0.02aA
I_{BCS} = 0.37aA
I_{SCS} = 0.2fA

HS 0.13µm technology with deep-trench isolation

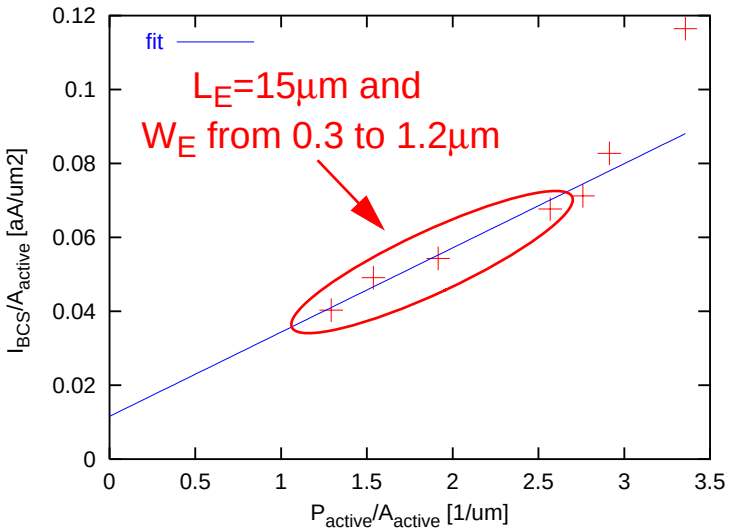
LC & HS 0.13µm technology without deep-trench

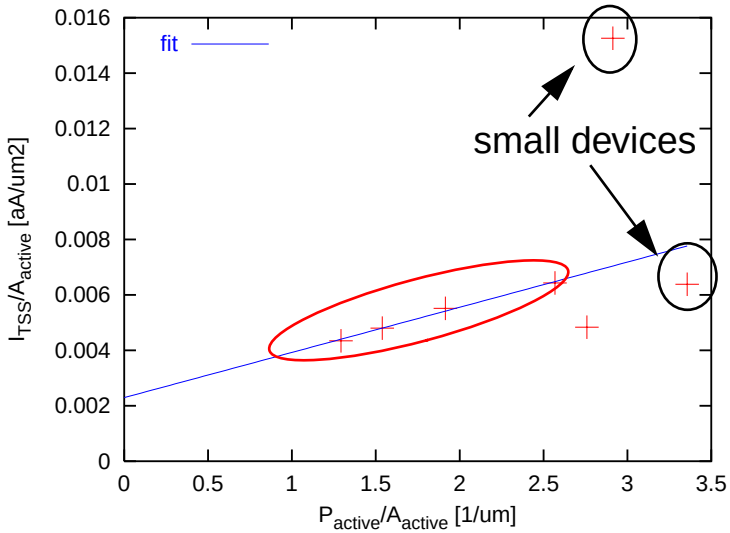


I_{TSS} = 0.13aA
I_{BCS} = 0.52aA
I_{SCS} = 1.2fA

Improved method description (3/3)

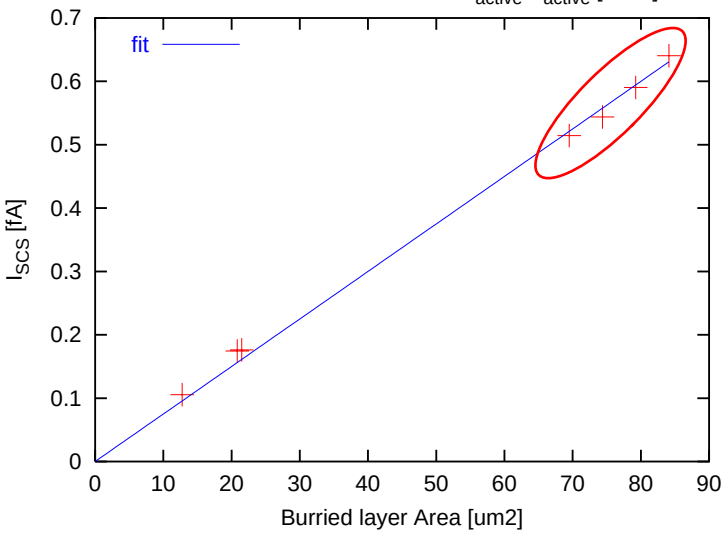
❒ Geometry scaling for 0.13µm technology devices with deep-trench:





L_E = from 2 to 15µm

W_E = from 0.3 to 1.2µm



Conclusion

- Two methods have been developed to extract parasitic substrate PNP model parameter and BC and SC diode parameters using DC data from HF measurements in a straigth forward manner.
- These methods have been applied successfully to several technologies, junction isolated or deep-trench isolated and scaling has been studied.