Review of Some HICUM Geometry Scaling Laws: Issue and Proposal

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Purpose

- Contrary to MOS models, bipolar models are not scalable
  - Not scalable means that the scaling rules are not *hard-coded* in the model equations.
- If we want to make scalable bipolar models, 2 main approaches [1]

  (i) Coding of scaling equations in simulator scripts

  (ii) Use separate specific program like TRADICA
- Each of these solutions have their pros and cons

  (i) Limited language capability, IP is open to external users.

  (ii) *Magic black box* where default geometry scaling equations are hidden to modeling engineers.
- Nevertheless, in the two cases we need to know (no detailed publication on this subject)
  - How to scale the model parameters to the dimensions of the devices.
  - How to determine specific parameters.
- Our goal is

  (i) to review some (limited time) HICUM geometry scaling laws, as we think they are,

  (ii) to discuss possible issues and

  (iii) to propose solutions...

Overview of HICUM Geometry Scaling Equations

- Effective emitter area
  - Definition
  - Parameter extraction
- Low collector current and depletion capacitances
  - Description of existing geometry scaling laws
  - Possible issue
  - Proposal and results
- Low Base-Emitter current
  - Description of existing scaling laws
  - Possible issue
  - Proposal and results
- Weak avalanche current
  - Description of existing geometry scaling laws
  - Issue
  - Proposal and results

Effective Emitter Area [2],[3]

Definition and extraction method

- Original concept allowing to model the peripheral transfer current without additional component (current source).

- The effective (electrical) emitter area, A_{E*}, is defined so that the total transfer current I_T flows through an extended internal transistor, via the parameter γ_C, without any peripheral component

$$I_T = I_{TA} + I_{TP} + 4I_{TC} = \underbrace{J_{TA} \cdot A_{E0}}_{\text{Area}} + \underbrace{J_{TP} \cdot P_{E0}}_{\text{Perimeter}} + \underbrace{4I_{TC}}_{\text{Corner}} = J_{TA} \cdot A_{E*}$$

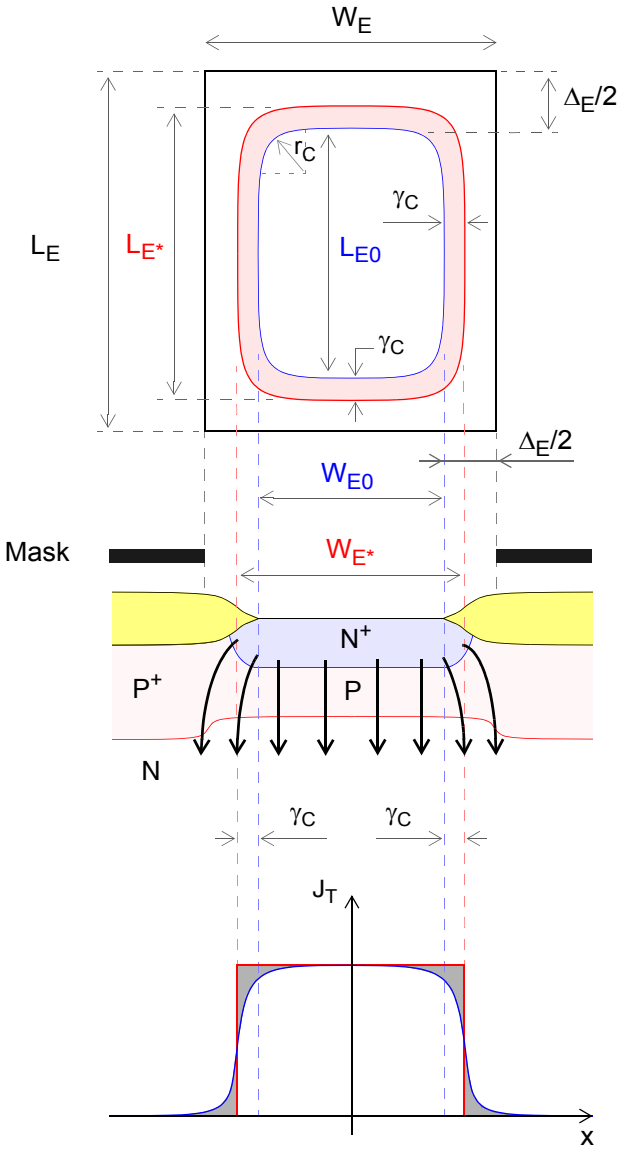
where the effective emitter area A_{E*} is given by

$$A_{E*} = W_{E*} \cdot L_{E*} = (L_{E0} + 2 \cdot \gamma_C) \cdot (W_{E0} + 2 \cdot \gamma_C)$$

- For small devices, 3-D effects can be improved by taken into account the corner rounding caused by lithography. In this case the effective emitter area becomes (Appendix A)

$$A_{E*} = W_{E*} \cdot L_{E*} - (4 - \pi) \cdot r_{c*}^{\,2} \quad \text{where} \quad r_{c*} = r_c + \gamma_C$$

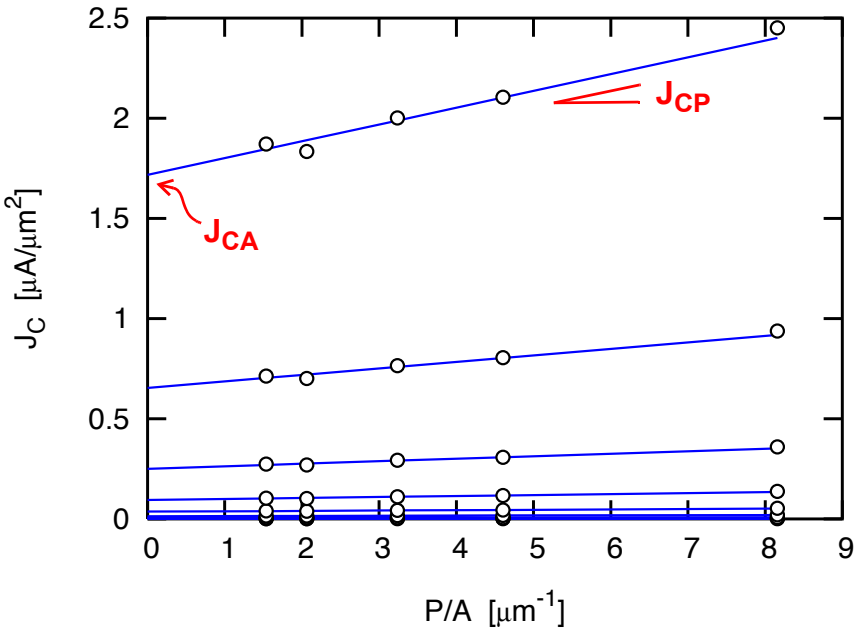
- Then to compute the model parameters for 2-D (and 3-D) transistors, all area specific elements (currents, charges) occurring in the Generalized Integral Charge-Control Relation (GICCR) must be multiplied by this effective emitter area.

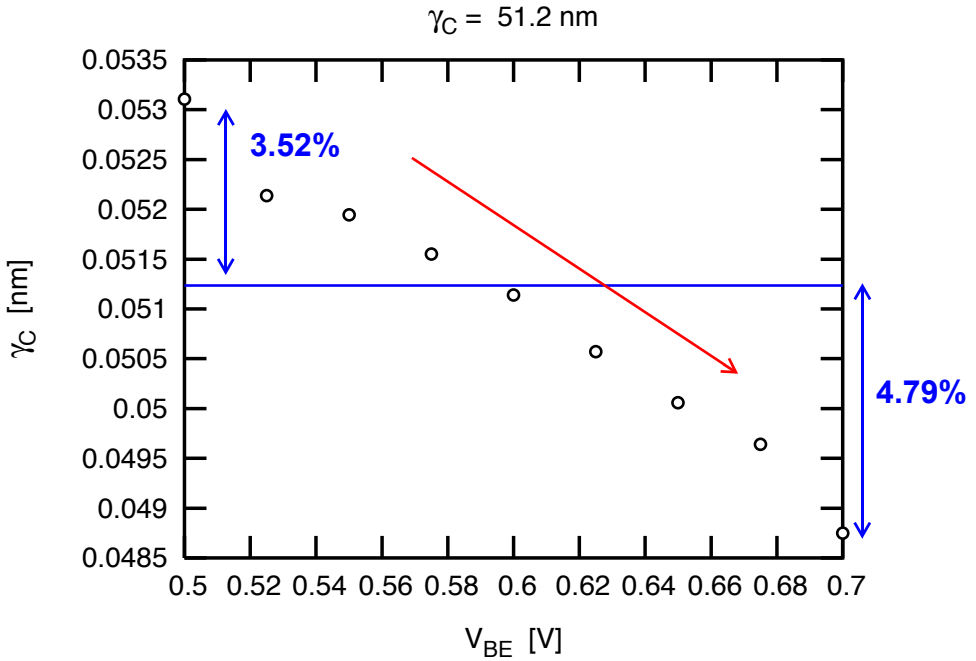


- The extended emitter width and length γ_C can be easily determined from the ratio of specific perimeter to area collector current
  - At low current densities ($V_{BE} < 0.7$ V and $V_{BC} = 0$V), we can write (corner rounding neglected, $L_E >> W_E$)

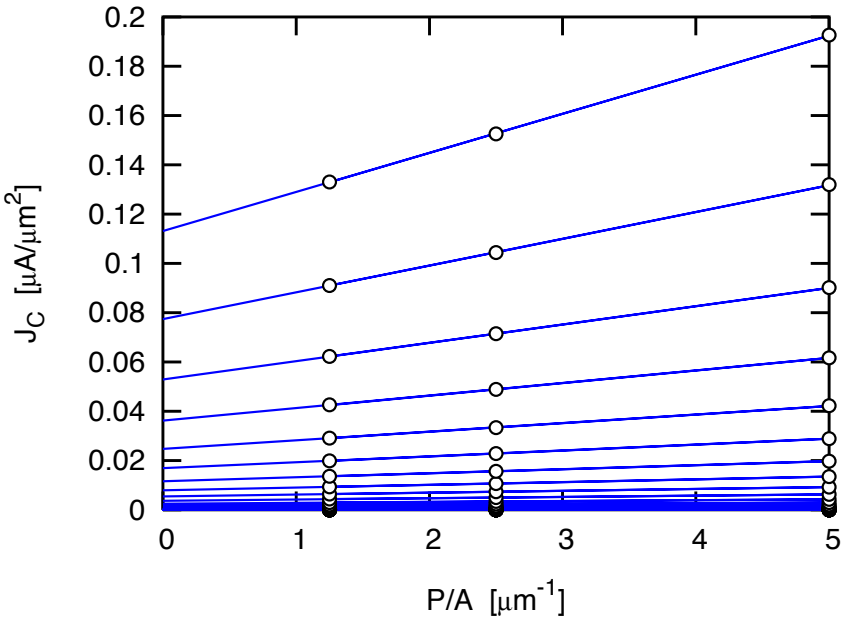
$$\begin{cases} I_T \approx I_C = I_{CA} + I_{CP} + 4I_{TC} = J_{CA} \cdot A_{E0} + \boxed{J_{CP} \cdot P_{E0}} + 4I_{TC} \\ I_T \approx I_C = I_{CA} \cdot A_{E*} = I_{CA} \cdot W_{E*} \cdot L_{E*} = I_{CA} \cdot (L_{E0} + 2\gamma_C) \cdot (W_{E0} + 2\gamma_C) = J_{CA} \cdot A_{E0} + \boxed{J_{CA} \cdot \gamma_C \cdot P_{E0}} + 4J_{CA} \cdot \gamma_C^2 \end{cases}$$

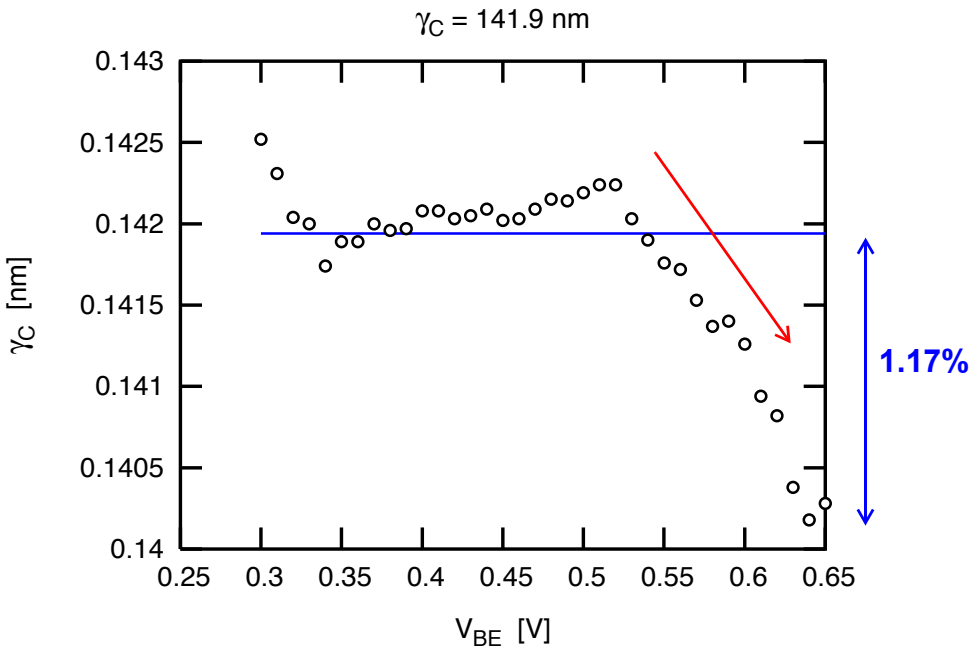
  - That allows to calculate γ_C $\quad \boxed{\gamma_C = \dfrac{J_{CP}}{J_{CA}}}$
  - Experimental results (HS transistors, W_E = 0.25, 0.45, 0.65, 1.05, 1.45 µm, L_E = 12.65 µm)





- TCAD results from process and device simulations (HV transistors, W_E = 0.4, 0.8, 1.6 µm, L_E = 12 µm)





Comments and possible issues

- At low current densities γ_C is not exactly a constant, slight decrease with V_{BE}
- Cause
  - Combination of measurement inaccuracy and correctness of extraction method?
  - Internal depletion charges not exactly proportional to the effective emitter area?
  - Model limitation? γ_C could be bias depend (investigation in progress)

Forward Transfer Current

- Study at low current densities and V_{BC} = 0V
- Geometry scaling equations
  - At low low current densities and V_{BC} = 0V, the collector current is close to the forward transfer current and can be written

$$I_C \approx I_{TF} = \frac{\mathbf{C_{10}} \cdot e^{\frac{V_{BEi}}{V_T}}}{\mathbf{Q_{p0}} + \mathbf{h_{jEi}} \cdot Q_{jEi}} \qquad (1)$$

The internal BE depletion charge Q_{jEi} is related to the internal depletion capacitance C_{jEi}, which is, by definition of the effective emitter area, (*normally*) proportional to A_{E*}

$$Q_{jEi} = A_{E*} \cdot Q_{jEA} \qquad (2)$$ where Q_{jEA} is the BE specific area depletion charge (C/m²)

  - Always by definition of the effective emitter area, I_{TF} is proportional to A_{E*} according to

$$I_{TF} = A_{E*} \cdot J_{TFA}$$ where J_{TFA} is the specific area forward transfer current (A/m²)

  - Therefore, J_{TFA} can be written

$$J_{TFA} = \frac{I_{TF}}{A_{E*}} = \frac{\mathbf{C_{10}} \cdot e^{\frac{V_{BEi}}{V_T}}}{A_{E*} \cdot (\mathbf{Q_{p0}} + \mathbf{h_{jEi}} \cdot Q_{jEi})} = \frac{\mathbf{C_{10}} \cdot e^{\frac{V_{BEi}}{V_T}}}{A_{E*} \cdot (\mathbf{Q_{p0}} + \mathbf{h_{jEi}} \cdot A_{E*} \cdot Q_{jEA})} = \frac{\mathbf{C_{10}} \cdot e^{\frac{V_{BEi}}{V_T}}}{A_{E*}^2 \cdot \left(\frac{\mathbf{Q_{p0}}}{A_{E*}} + \mathbf{h_{jEi}} \cdot Q_{jEA}\right)} = \frac{C_{10A} \cdot e^{\frac{V_{BEi}}{V_T}}}{Q_{p0A} + \mathbf{h_{jEi}} \cdot Q_{jEA}}$$

- In conclusion, the specific area forward transfer current J_{TFA} is given by

$$J_{TFA} = \frac{C_{10A} \cdot e^{\frac{V_{BEi}}{V_T}}}{Q_{p0A} + \mathbf{h_{jEi}} \cdot Q_{jEA}} \qquad (3)$$

where C_{10A} and Q_{p0A} are respectively the specific GICCR constant (AC/m^4) and the specific zero-bias hole charge (C/m^2).

This expression is identical to (1) where the model parameters have been replaced by their specific values.

Parameter extraction

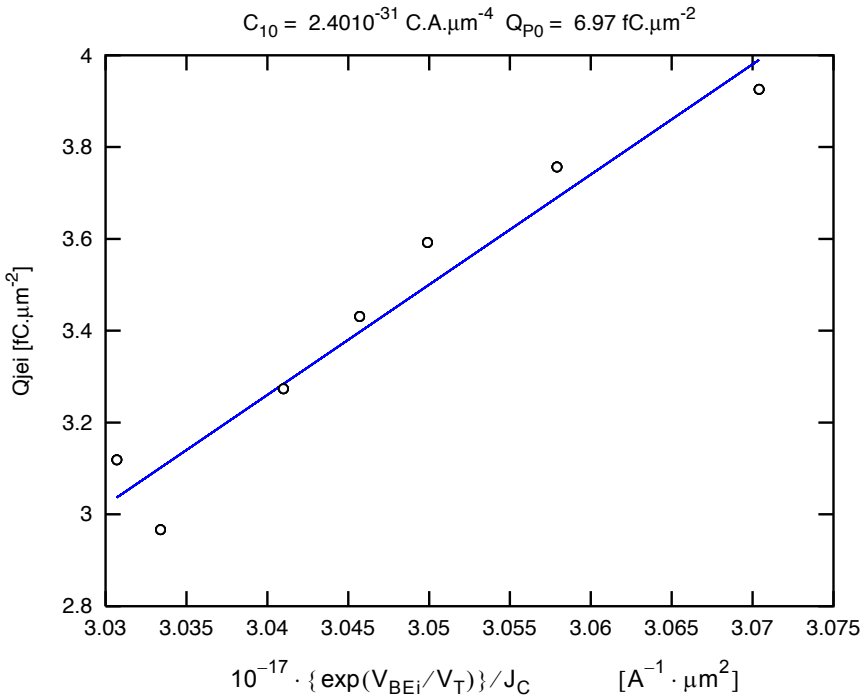
- Re-arranging (3) gives

$$Q_{jEA} = \frac{C_{10A}}{\mathbf{h_{jEi}}} \cdot \frac{e^{\frac{V_{BEi}}{V_T}}}{J_{TFA}} - \frac{Q_{p0A}}{\mathbf{h_{jEi}}}$$

where Q_{jEA} is calculated from the specific parameters of the BE depletion capacitance.

Therefore, Q_{jEA} vs. $e^{\frac{V_{BEi}}{V_T}} / J_{TFA}$ is a straight line. The slope **s** allows to calculate C_{10A}, and the intercept **i** allows to know Q_{P0A}. At this step (and even after! [4]), $\mathbf{h_{jEi}}$ is assumed to be equal to 1

$$\begin{cases} C_{10A} = \mathbf{s} \cdot \mathbf{h_{jEi}} = \mathbf{s} \\ Q_{p0A} = -\mathbf{i} \cdot \mathbf{h_{jEi}} = -\mathbf{i} \end{cases}$$



Possible issues

- The main issues comes from the fact that the specific parameters (area and perimeter components) of BE junction capacitance are determined from the actual emitter dimensions on wafer and that after the internal and external BE junction capacitance are generated from the effective emitter area:
  - Possible negative external BE junction capacitance
  - External potential and grading factor different than extracted values, needed to be re-calculated for each emitter size.
- The BE depletion capacitance, related to the actual emitter dimensions, is given by (2D device)

$$C_{JE}(V) = C_{JEA}(V) + C_{JEP}(V) = \overline{C_{JEA}}(V) \cdot A_{E0} + \overline{C_{JEP}}(V) \cdot P_{E0}$$

where C_{JEA} and C_{JEP} are respectively the area and perimeter components of the BE junction capacitance. $\overline{C_{JEA}}$ and $\overline{C_{JEP}}$ being respectively the specific area and perimeter components. From their bias dependence, we can write

$$C_{JE}(V) = \frac{\mathbf{C_{JEA0}} \cdot A_{E0}}{\left\{1 - \frac{V}{\mathbf{V_{DEA}}}\right\}^{\mathbf{z_{EA}}}} + \frac{\mathbf{C_{JEX0}} \cdot P_{E0}}{\left\{1 - \frac{V}{\mathbf{V_{DEX}}}\right\}^{z_{EX}}} \quad (4)$$

- In order to be compatible with the HICUM geometry scaling laws and to be consistent with the GICCR (all collector current flows through an effective electrical emitter area A_{E*}, without perimeter component), $C_{JE}(V)$ must be expressed from the effective area as follows

$$C_{JE}(V) = C_{JEi}(V) + C_{JEx}(V) = \underbrace{\overline{C_{JEA}}(V) \cdot A_{E*}}_{\text{Internal transistor}} + \underbrace{\overline{C_{JEP}}(V) \cdot P_{E0} - \overline{C_{JEA}}(V) \cdot (A_{E*} - A_{E0})}_{\text{External transistor}} \quad (5)$$

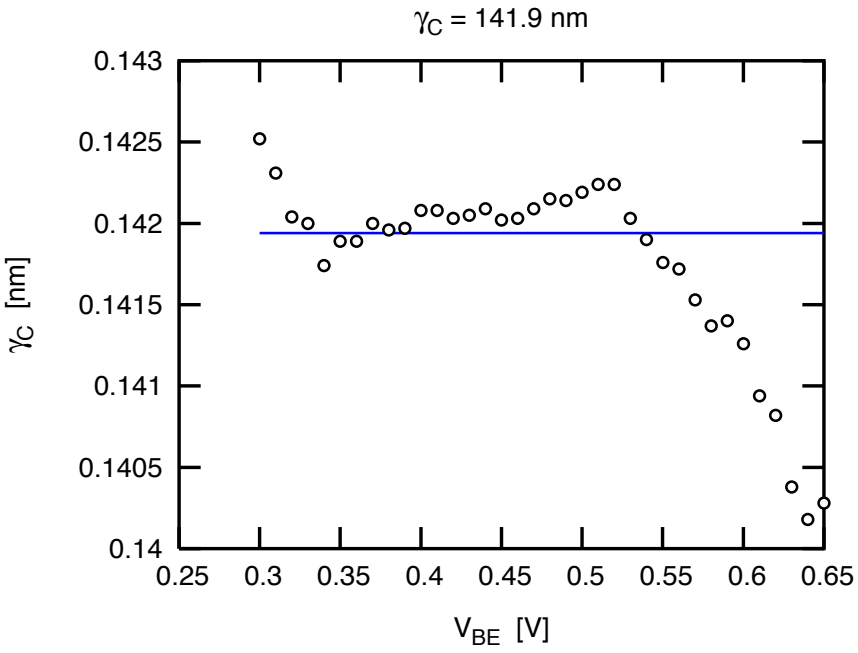
- 1st issue: depending on the technology, the external part of the BE junction capacitance can be negative

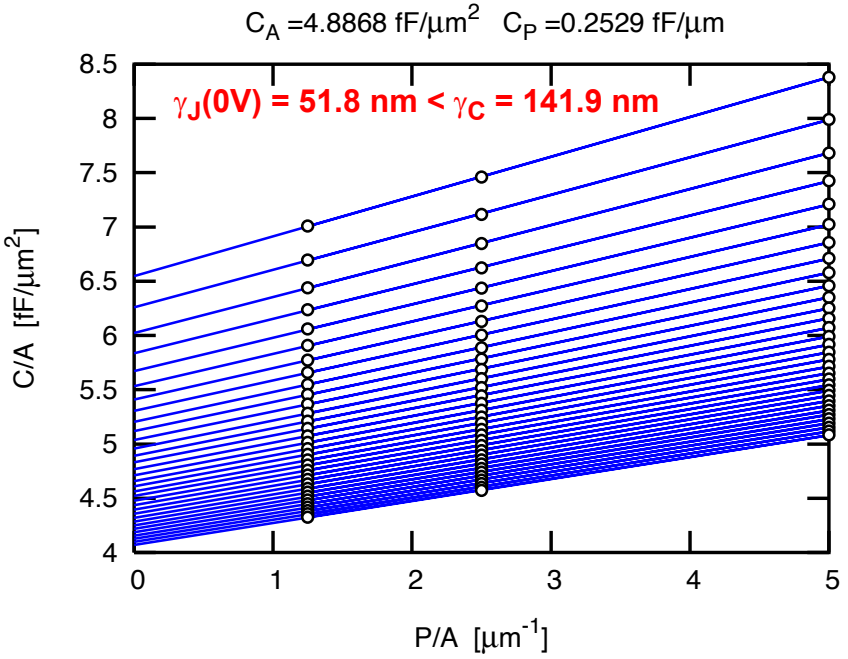
$$\overline{C_{JEP}}(V)\cdot P_{E0} - \overline{C_{JEA}}(V)\cdot (A_{E*} - A_{E0}) = \overline{C_{JEP}}(V)\cdot P_{E0} - \overline{C_{JEA}}(V)\cdot (A_{E0} + \gamma_C \cdot P_{E0} - A_{E0}) =$$

$$\overline{C_{JEP}}(V)\cdot P_{E0} - \overline{C_{JEA}}(V)\cdot \gamma_C \cdot P_{E0} = \overline{C_{JEA}}(V)\cdot P_{E0}\cdot \left\{ \frac{\overline{C_{JEP}}(V)}{\overline{C_{JEA}}(V)} - \gamma_C \right\} = \overline{C_{JEA}}(V)\cdot P_{E0}\cdot (\gamma_J - \gamma_C)$$

where $\gamma_J = \dfrac{\overline{C_{JEP}}(V)}{\overline{C_{JEA}}(V)}$ is defined as the ratio of specific perimeter to area BE junction capacitance.

- if $\gamma_J < \gamma_C$ the external BE junction capacitance becomes negative!
- TCAD results from process and device simulation (HV transistors, W_E = 0.4, 0.8, 1.6 µm, L_E = 12 µm)





- 2nd issue: the built in potential and the grading factor must be re-calculated for each transistor dimension. If is it feasible and done (?) in program like TRADICA, it is more complex to implemented in language simulators.

  - Moreover, if γ_J is close to γ_C, the re-calculated built-in voltage and grading factor can have non-physical value. From (4) and (5) we can write

$$C_{JE}(V) = \underbrace{\frac{C_{JEA0} \cdot A_{E*}}{\left\{1 - \frac{V}{V_{DEA}}\right\}^{Z_{EA}}}}_{\text{Internal transistor}} + \underbrace{\frac{C_{JEX0} \cdot P_{E0}}{\left\{1 - \frac{V}{V_{DEX}}\right\}^{Z_{EX}}} - \frac{C_{JEA0} \cdot (A_{E*} - A_{E0})}{\left\{1 - \frac{V}{V_{DEA}}\right\}^{Z_{EA}}}}_{\text{External transistor}}$$

$$= \frac{\mathbf{C_{JEI0}}}{\left\{1 - \frac{V}{\mathbf{V_{DEI}}}\right\}^{\mathbf{Z_{EI}}}} + \frac{\mathbf{C_{JEP0}}}{\left\{1 - \frac{V}{\mathbf{V_{DEP}}}\right\}^{\mathbf{Z_{EP}}}}$$

  - For the internal transistor, the model parameters of the BE junction capacitance are directly related to the extracted specific parameters. It is no more true for the external transistor. V_{DEP} and Z_{EP} are not equal to the extracted specific parameters V_{DEX} and Z_{EX}. They are respectively function of V_{DEX}, V_{DEA} and Z_{EX}, Z_{EA} and must be re-calculated for each transistor dimensions.

Solution and proposal

TRADICA approach

- From the information we have, if $\gamma_J < \gamma_C$, it would seem that

$$\begin{cases} C_{JEi}(V) = \overline{C_{JEA}}(V) \cdot A_{E0} + \overline{C_{JEP}}(V) \cdot P_{E0} \\ C_{JEx}(V) = 0 \end{cases}$$

- Using this approach poses a problem, because Q_{jEi} is no more proportional to A_{E*}, and consequently I_{TF} is also no more proportional to A_{E*}.

- Therefore the exposed method used to determine the specific parameters Q_{P0A} and C_{10A} is no more valid.

- How to overcome this problem?

Proposal

- Contrary to (5) we defined the internal and the external BE junction capacitance from the actual emitter area and perimeter $C_{JE}(V) = C_{JEi}(V) + C_{JEx}(V) = \underbrace{\overline{C_{JEA}}(V) \cdot A_{E0}}_{\text{Internal transistor}} + \underbrace{\overline{C_{JEP}}(V) \cdot P_{E0}}_{\text{External transistor}}$

- Therefore Q_{jEi} is directly related to the emitter area A_{E0} through $Q_{jEi} = A_{E0} \cdot Q_{jEA}$ where Q_{jEA} is calculated from the area components (C_{JEA}, V_{DEA}, Z_{EA}) of the BE depletion capacitance.

- The expression of J_{TFA} becomes

$$J_{TFA} = \frac{I_{TF}}{A_{E*}} = \frac{\mathbf{C_{10}} \cdot e^{\frac{V_{BEi}}{V_T}}}{A_{E*} \cdot (\mathbf{Q_{p0}} + \mathbf{h_{jEi}} \cdot Q_{jEi})} = \frac{\mathbf{C_{10}} \cdot e^{\frac{V_{BEi}}{V_T}}}{A_{E*} \cdot (\mathbf{Q_{p0}} + \mathbf{h_{jEi}} \cdot A_{E0} \cdot Q_{jEA})} = \frac{\frac{\mathbf{C_{10}}}{A_{E*}^2} \cdot e^{\frac{V_{BEi}}{V_T}}}{\frac{\mathbf{Q_{p0}}}{A_{E*}} + \mathbf{h_{jEi}} \cdot \frac{A_{E0}}{A_{E*}} \cdot Q_{jEA}}$$

$$= \frac{C_{10A} \cdot e^{\frac{V_{BEi}}{V_T}}}{Q_{p0A} + \boxed{\mathbf{h_{jEi}} \cdot \frac{A_{E0}}{A_{E*}}} \cdot Q_{jEA}}$$

- In order to be consistent with the HICUM scaling approach, I_{TF} must be proportional to A_{E*}, we have to define a new unitary (or specific) parameter $\mathbf{h_{jEu}}$ such as

$$\boxed{\mathbf{h_{jEu}} = \mathbf{h_{jEi}} \cdot \frac{A_{E0}}{A_{E*}} = \text{constant}}$$

- We can finally write

$$J_{TFA} = \frac{C_{10A} \cdot e^{\frac{V_{BEi}}{V_T}}}{Q_{p0A} + \mathbf{h_{jEu}} \cdot Q_{jEA}}$$

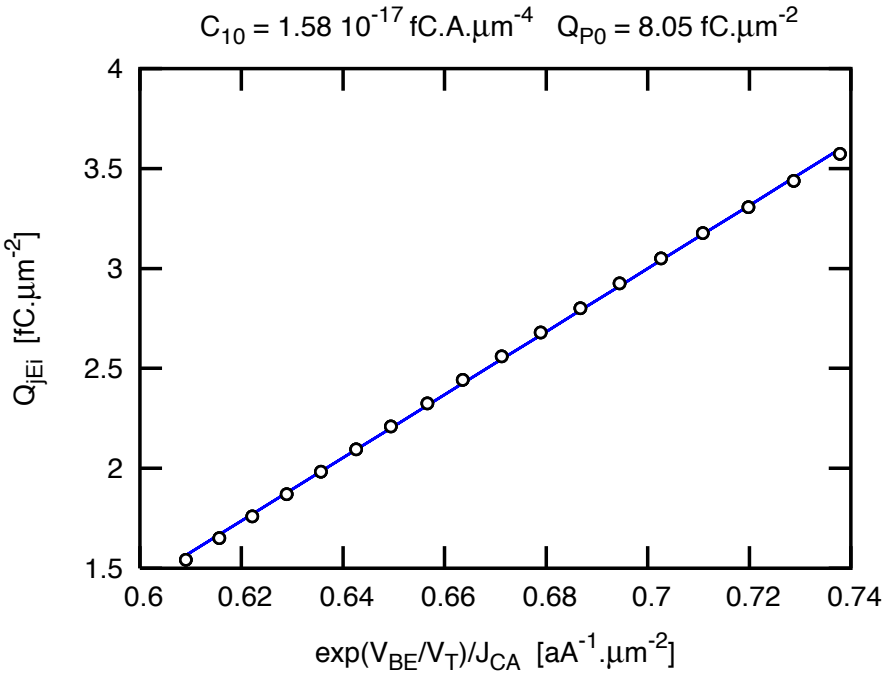
- This equation is identical to the previous equation (3), expect that now Q_{JEA} is now expressed from A_{E0} and not from A_{E*}. That allows to avoid negative Q_{JEA} value.

Parameter extraction and results

- Identical methodology to the one describes previously

$$Q_{jEA} = \frac{C_{10A}}{\mathbf{h_{jEu}}} \cdot \frac{e^{\frac{V_{BEi}}{V_T}}}{J_{TFA}} - \frac{Q_{p0A}}{\mathbf{h_{jEu}}}$$

Q_{jEA} vs. $e^{\frac{V_{BEi}}{V_T}} / J_{TFA}$ is a straight line. The slope **s** allows to calculate C_{10A}, and the intercept **i** allow to know Q_{P0A}.



- Here again $\mathbf{h_{jEu}}$ is assumed to be equal to 1

$$\begin{cases} C_{10A} = \mathbf{s} \cdot \mathbf{h_{jEu}} = \mathbf{s} \\ Q_{p0A} = -\mathbf{i} \cdot \mathbf{h_{jEu}} = -\mathbf{i} \end{cases}$$

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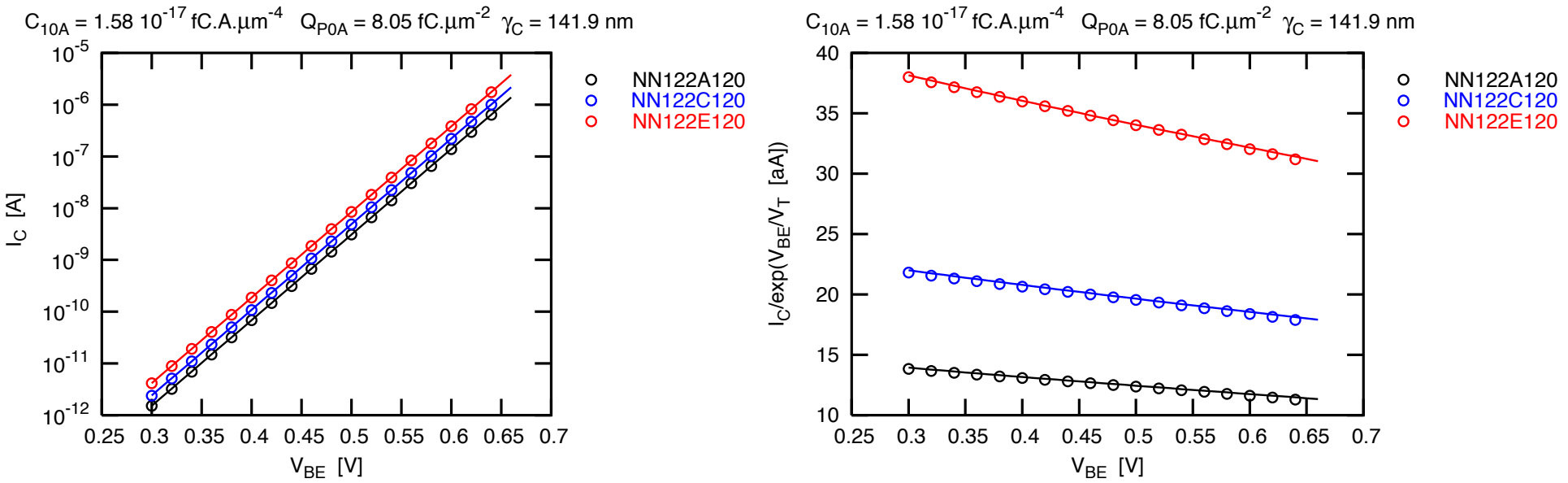


- Scaling law for the collector current at low current densities and V_{BC} =0V

$$I_C \approx J_{TFA} \cdot A_{E*} = \frac{C_{10A} \cdot A_{E*}^2 \cdot e^{\frac{V_{BEi}}{V_T}}}{Q_{p0A} \cdot A_{E*} + \mathbf{h_{jEu}} \cdot Q_{jEA} \cdot A_{E*}} = \frac{C_{10} \cdot e^{\frac{V_{BEi}}{V_T}}}{Q_{p0} + \mathbf{h_{jEu}} \cdot \frac{Q_{jEi}}{A_{E0}} \cdot A_{E*}} = \frac{C_{10} \cdot e^{\frac{V_{BEi}}{V_T}}}{Q_{p0} + \mathbf{h_{jEi}} \cdot Q_{jEi}}$$

- With this new approach $\mathbf{h_{jEi}}$ is now geometry dependent and is defined, for each transistor geometry, by

$$\mathbf{h_{jEi}} = \mathbf{h_{jEu}} \cdot \frac{A_{E*}}{A_{E0}}$$

- We can extend this study to the BC junction ($V_{BC} < 0$ V) in order to obtain the general expression of the transfer I_T current at low current densities

$$I_T = J_{TFA} \cdot A_{E^*} = \frac{\mathbf{C_{10}} \cdot e^{\frac{V_{BEi}}{V_T}}}{\mathbf{Q_{p0}} + \mathbf{h_{jEi}} \cdot Q_{jEi} + \mathbf{h_{jCi}} \cdot Q_{jCi}}$$

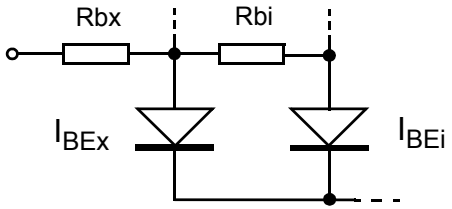
Where the new geometry scaling rules are defined by

$$\begin{cases} \mathbf{C_{10}} = \mathbf{C_{10A}} \cdot A_{E^*}^2 \\ \mathbf{Q_{P0}} = \mathbf{Q_{POA}} \cdot A_{E^*} \\ \mathbf{Q_{jEi}} = \mathbf{Q_{jEA}} \cdot A_{E0} = f(\mathbf{C_{JEA}}, \mathbf{V_{DEA}}, \mathbf{Z_{EA}}) \cdot A_{E0} \\ \mathbf{Q_{jCi}} = \mathbf{Q_{jCA}} \cdot A_{C0} = f(\mathbf{C_{JCA}}, \mathbf{V_{DCA}}, \mathbf{Z_{CA}}) \cdot A_{C0} \\ \mathbf{I_S} = \frac{\mathbf{C_{10}}}{\mathbf{Q_{P0}}} = \frac{\mathbf{C_{10A}}}{\mathbf{Q_{P0A}}} \cdot A_{E^*} = \mathbf{J_{SA}} \cdot A_{E^*} \\ \mathbf{h_{jEi}} = \mathbf{h_{jEu}} \cdot \frac{A_{E^*}}{A_{E0}} \\ \mathbf{h_{jCi}} = \mathbf{h_{jCu}} \cdot \frac{A_{E^*}}{A_{C0}} \end{cases}$$

Base-Emitter Current

Model

- Low current densities and V_{BC} = 0 V
- In HICUM/L2, the BE current is described by 2 diodes. One diode used to describe the internal BE current I_{BEi}, the second for the extrinsic BE current I_{BEX}. These 2 diodes are spitted across the intrinsic base resistance.



- Each of these 2 diodes are composed of an ideal current (non-ideality factor close to 1), and a recombination current (non-ideality factor close to 2).

$$\begin{cases} I_{BEi} = I_{BEA} + I_{REA} = \mathbf{I_{BEIS}} \cdot \left(e^{\frac{V_{BEi}}{\mathbf{M_{BEI}} \cdot V_T}} - 1 \right) + \mathbf{I_{REIS}} \cdot \left(e^{\frac{V_{BEi}}{\mathbf{M_{REI}} \cdot V_T}} - 1 \right) \\ I_{BEx} = I_{BEP} + I_{REP} = \mathbf{I_{BEPS}} \cdot \left(e^{\frac{V_{BEi}}{\mathbf{M_{BEP}} \cdot V_T}} - 1 \right) + \mathbf{I_{REPS}} \cdot \left(e^{\frac{V_{BEi}}{\mathbf{M_{REP}} \cdot V_T}} - 1 \right) \end{cases}$$

Geometry scaling rules

- No (?) official (published) document describing the scaling laws used, in TRADICA, for the base currents.

- If the introduction of an effective emitter area, using γ_C, is very clever for describing the geometry dependence of the transfer current. The notion of an effective area for the base current, using γ_B, is more questionable:

- 1st issue: as the BE current is modeled by 2 diodes (contrary to the transfer current which is modeled by only one current source), there is no interest to define and effective area for the base current.

- 2nd issue: if the internal base current is referenced to the effective emitter area A_{E*} and if $\gamma_B < \gamma_C$, we can demonstrate (same demonstration than for the BE depletion capacitance) that the extrinsic BE current, I_{BEx}, will be negative

$$\begin{cases} I_{BEi} = J_{BEA} \cdot A_{E*} \\ I_{BEx} = J_{BEA} \cdot P_{E0} \cdot (\gamma_B - \gamma_C) \end{cases}$$

- 3rd issue: In fact, contrary to the transfer current, it is not possible to introduce the notion of effective area for the base current. Indeed, if we define the parameter γ_B, allowing to introduce the effective emitter area for the base current, as the ratio of the perimeter specific BE current, J_{BP}, to the area BE specific current, J_{BA}

$$\gamma_B = \frac{J_{BEP}}{J_{BEA}}$$

This parameter is not constant with V_{BE} due to the fact that the non-ideality factor of the area and perimeter currents are not identical

$$\begin{cases} J_{BEA} \approx J_{BEAS} \cdot e^{\frac{V_{BEi}}{\mathbf{M_{BEA}} \cdot V_T}} \\ J_{BEP} \approx J_{BEPS} \cdot e^{\frac{V_{BEi}}{\mathbf{M_{BEP}} \cdot V_T}} \end{cases}$$

therefore

$$\gamma_B = \frac{J_{BEP}}{J_{BEA}} = \frac{J_{BEPS}}{J_{BEAS}} \cdot e^{\frac{V_{BEi}}{V_T} \cdot \left\{ \frac{1}{\mathbf{M_{BEP}}} - \frac{1}{\mathbf{M_{BEA}}} \right\}}$$

is not a constant and is a function of V_{BE} if $\mathbf{M_{BEA}} \neq \mathbf{M_{BEP}}$.

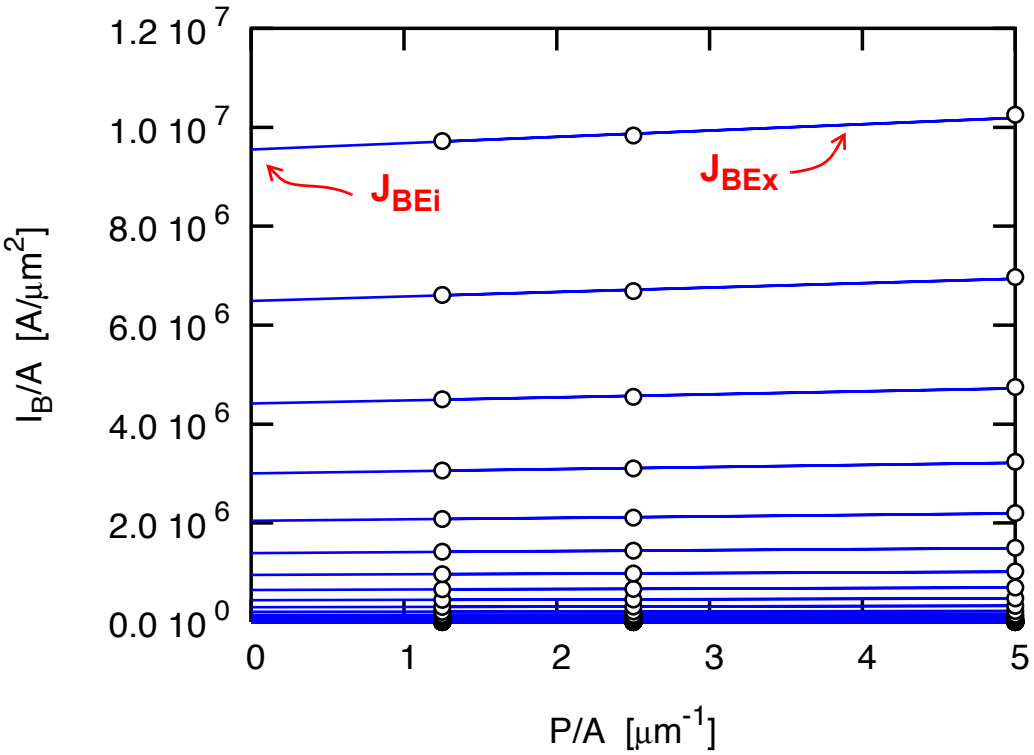
New proposed geometry scaling rules and parameter extraction

- The base current is split on 2 components I_{BEi} and I_{BEX} respectively related to the actual BE area and perimeter

$$I_{BE} = I_{BEi} + I_{BEx} = J_{BEi} \cdot A_{E0} + J_{BEx} \cdot P_{E0}$$

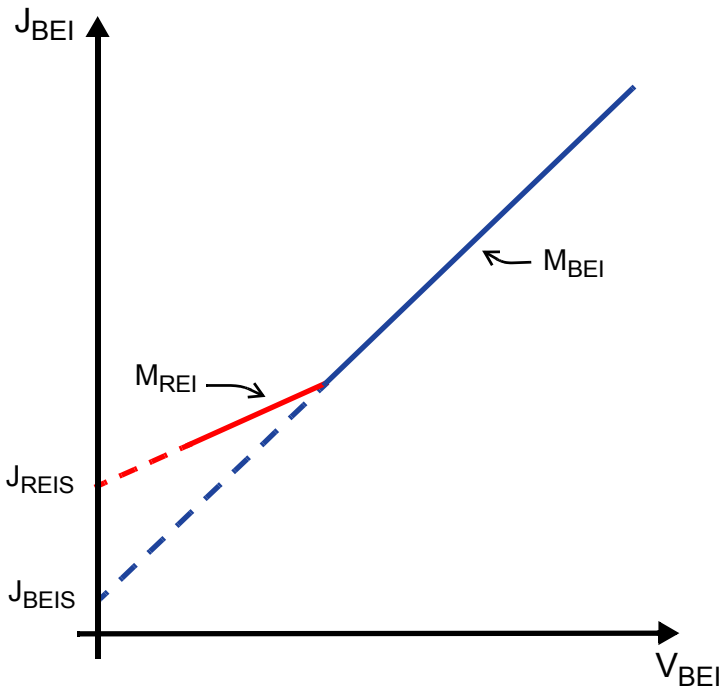
- J_{BEI} and J_{BEX} can be easily determinated (from 2D transistors with variable emitter width), at each V_{BE} (V_{BC}=0V), by plotting I_{BE}/A_{E0} vs. P_{E0}/A_{E0}

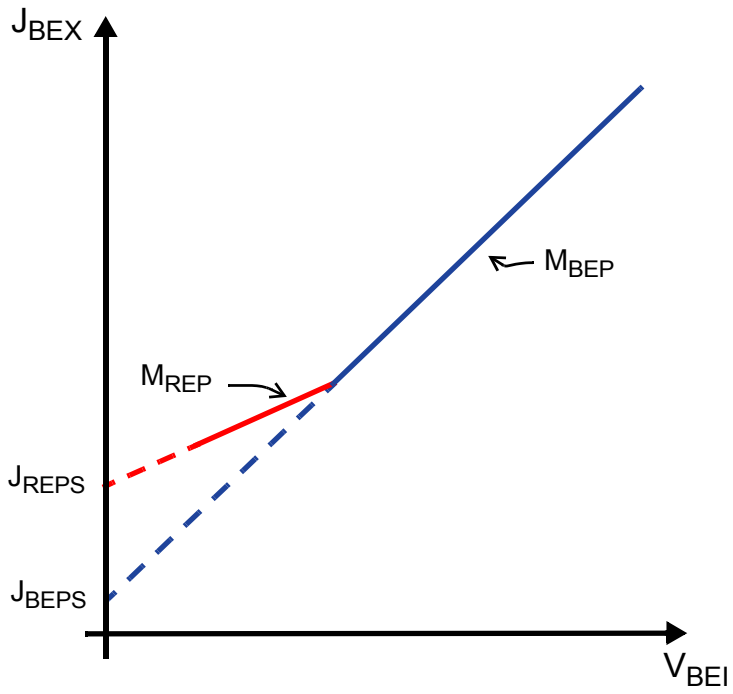
$$\frac{I_{BE}}{A_{E0}} = J_{BEi} + J_{BEx} \cdot \frac{P_{E0}}{A_{E0}}$$



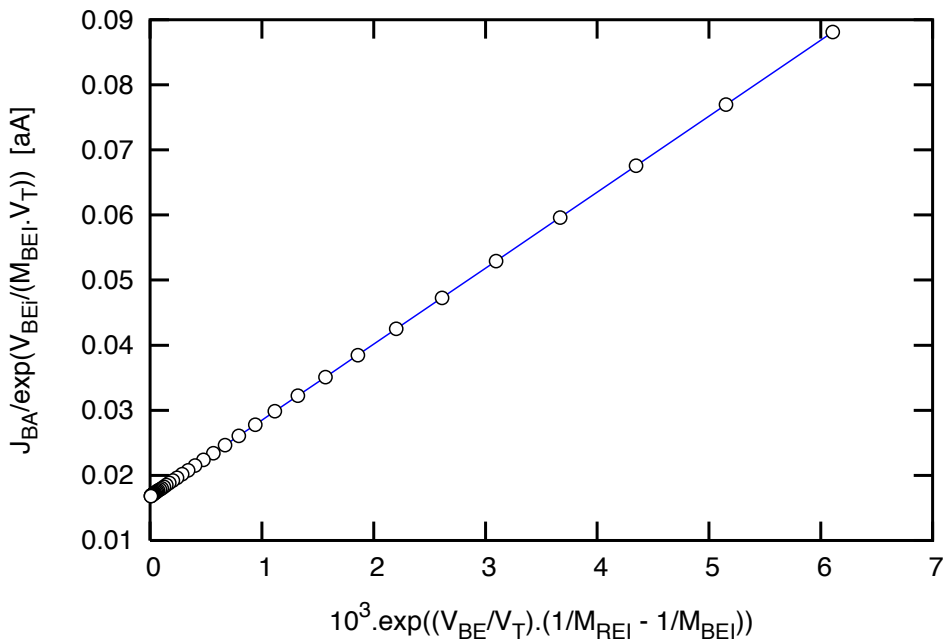
- Formulation of the internal and external BE specific currents J_{BEI} and J_{BEX}

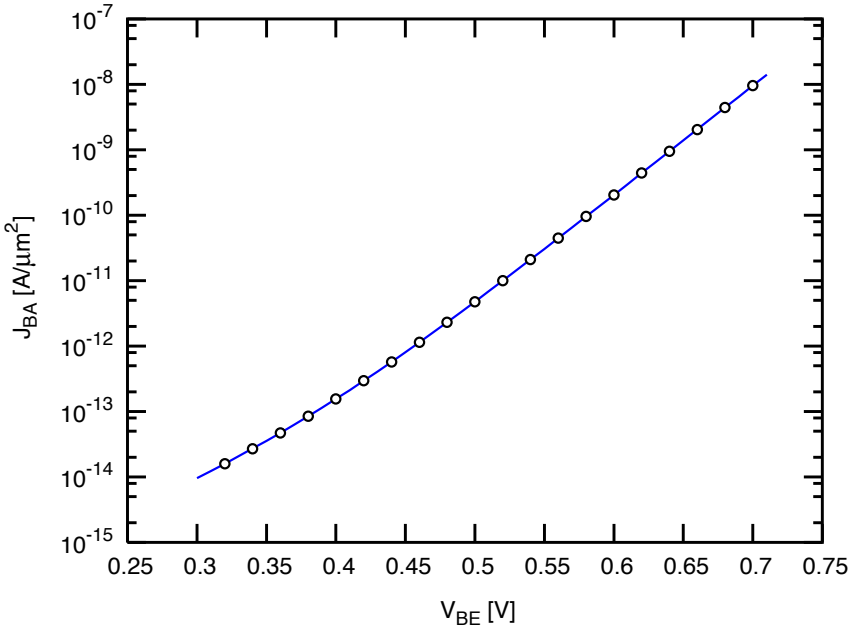
$$\begin{cases} J_{BEi} = J_{\mathbf{BEIS}} \cdot \left(e^{\frac{V_{BEi}}{\mathbf{M_{BEI}} \cdot V_T}} - 1 \right) + J_{\mathbf{REIS}} \cdot \left(e^{\frac{V_{BEi}}{\mathbf{M_{REI}} \cdot V_T}} - 1 \right) \\ J_{BEX} = J_{\mathbf{BEPS}} \cdot \left(e^{\frac{V_{BEi}}{\mathbf{M_{BEP}} \cdot V_T}} - 1 \right) + J_{\mathbf{REPS}} \cdot \left(e^{\frac{V_{BEi}}{\mathbf{M_{REP}} \cdot V_T}} - 1 \right) \end{cases}$$





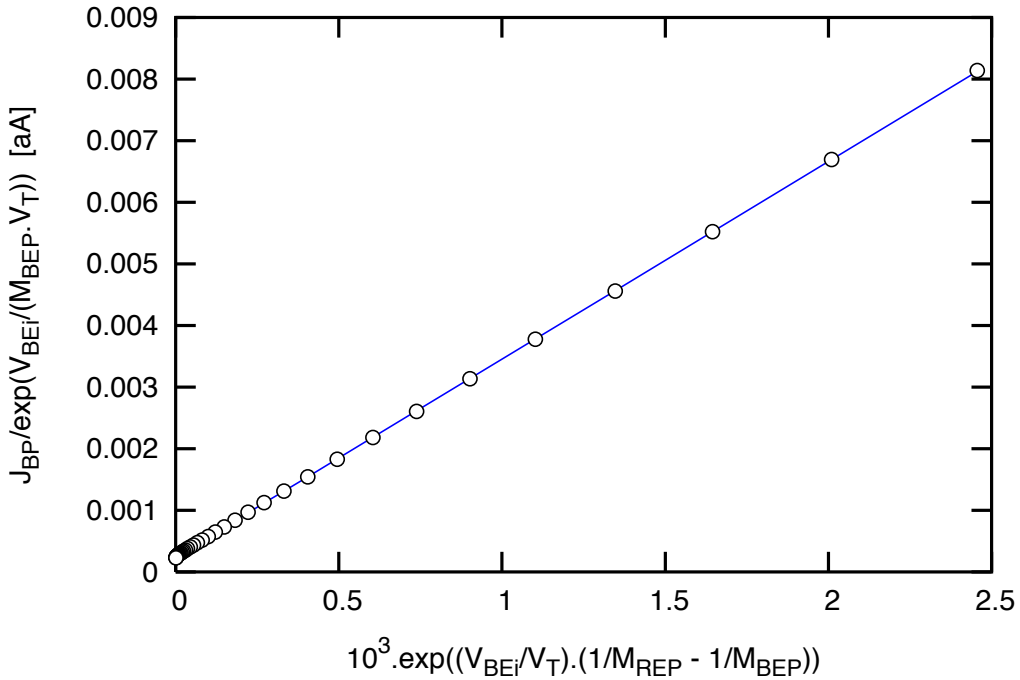
- Determination of the intrinsic BE specific parameters J_{BEIS}, J_{REIS}, M_{BEI}, M_{REI}
  - Direct extraction without global optimization, the key point to obtain both accurate and physics based model parameters.
  - Assuming V_{BEI} greater than few V_T, we can write $\frac{J_{BEi}}{e^{\frac{V_{BEi}}{M_{BEI} \cdot V_T}}} = J_{BEIS} + J_{REIS} \cdot e^{\frac{V_{BEi}}{V_T} \cdot \left\{ \frac{1}{M_{REI}} - \frac{1}{M_{BEI}} \right\}}$
  - Therefore, if M_{BEI} and M_{REI} are known, this characteristic is linear, the slope allows to determine J_{REIS} and the intercept J_{BEIS}.
  - How to determine M_{BEI} and M_{REI}? M_{BEI} and M_{REI} are determined by dichotomy, for each couple (M_{BEI}, M_{REI}), the correlation coefficient r of the characteristic is calculated. The selected couple (M_{BEI}, M_{REI}) is the one which maximize r (best alignment of the measured data).

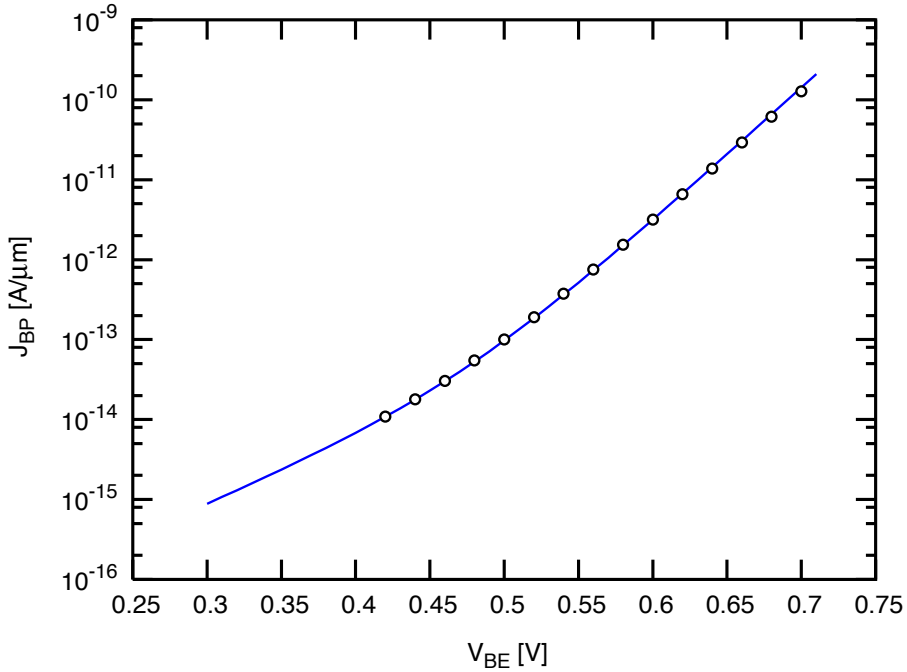




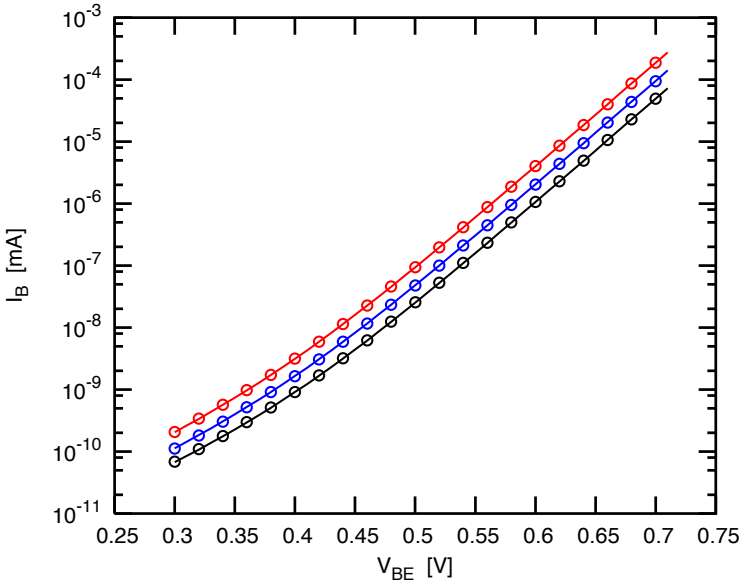
- Determination of the extrinsic BE specific parameters J_{BEPS}, J_{REPS}, M_{BEP}, M_{REP}

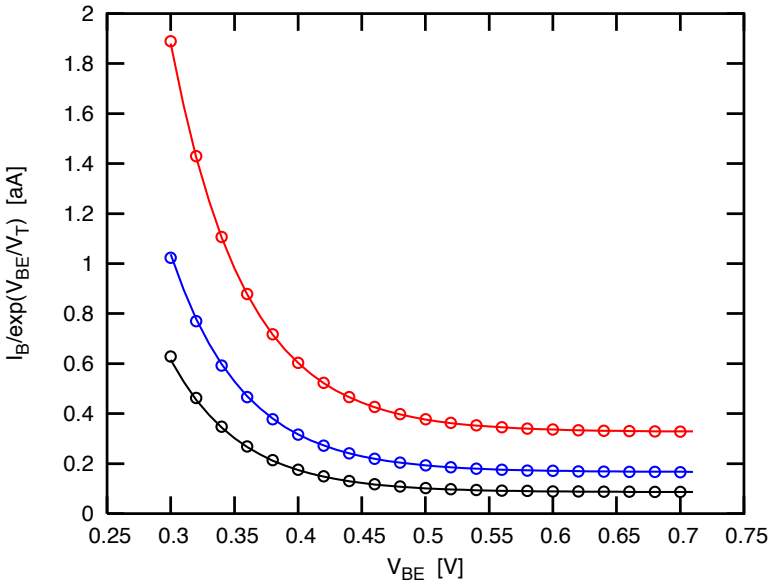
  - Same principle on the characteristic $\frac{J_{BEx}}{e^{\frac{V_{BEi}}{M_{BEP} \cdot V_T}}} = J_{BEPS} + J_{REPS} \cdot e^{\frac{V_{BEi}}{V_T} \cdot \left\{ \frac{1}{M_{REP}} - \frac{1}{M_{BEP}} \right\}}$

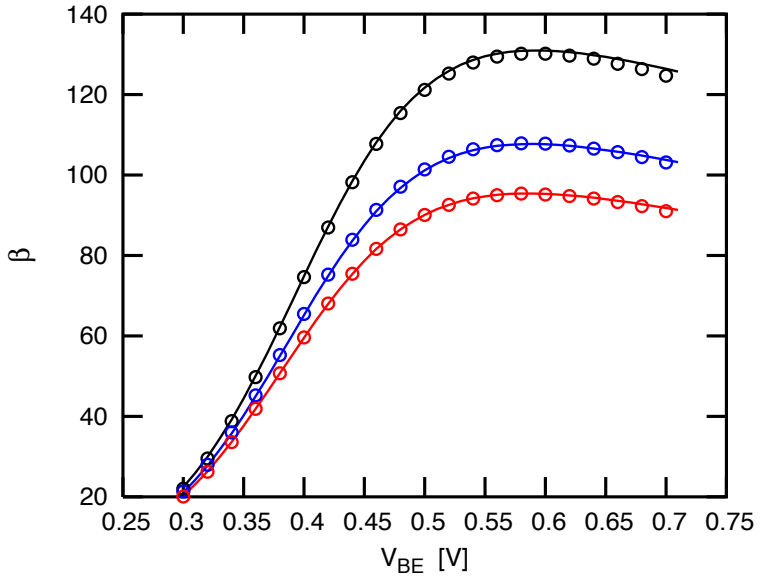




- TCAD results from process and device simulation (HV transistors, W_E = 0.4, 0.8, 1.6 µm, L_E = 12 µm)







Weak Avalanche Current

Geometry scaling rules

- Same comment than for the base current, to our knowledge, there is no published document describing the geometry scaling laws for the weak avalanche current.
- In HICUM/L2, the weak avalanche current is given by

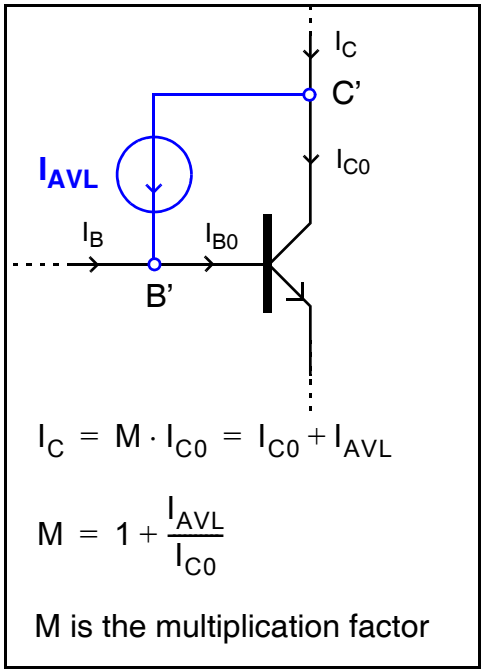
$$I_{AVL} = I_{TF} \cdot \mathbf{F_{AVL}} \cdot (V_{DCi} - V_{B'C'}) \cdot \exp\left\{\frac{-\mathbf{Q_{AVL}}}{C_{JCi} \cdot (V_{DCi} - V_{B'C'})}\right\}$$

- In first approximation, we assume that both I_{AVL} and I_{TF} are scaled to the effective emitter area A_{E*} (default TRADICA approach?)

$$\begin{cases} I_{TF} = J_{TF} \cdot A_{E*} \\ I_{AVJ} = J_{AVL} \cdot A_{E*} \end{cases}$$

- Normally both Q_{AVL} and C_{JCI} are scaled to the same dimension, whichever this dimension, we have

$$\frac{Q_{AVL}}{C_{JCi}} = \frac{\overline{Q_{AVL}}}{\overline{C_{JCi}}} = \text{cst}$$



- In conclusion, the multiplication factor M defined by

$$M = 1 + \frac{I_{AVL}}{I_{C0}} \approx 1 + \frac{I_{TF} \cdot \mathbf{F_{AVL}} \cdot (V_{DCi} - V_{B'C'}) \cdot e^{\frac{-\mathbf{Q_{AVL}}}{C_{JCi} \cdot (V_{DCi} - V_{B'C'})}}}{I_{TF}} = 1 + \mathbf{F_{AVL}} \cdot (V_{DCi} - V_{B'C'}) \cdot e^{\frac{-\overline{Q_{AVL}}}{\overline{C_{JCi}} \cdot (V_{DCi} - V_{B'C'})}} \quad (6)$$

must be constant

Scalable parameter extraction

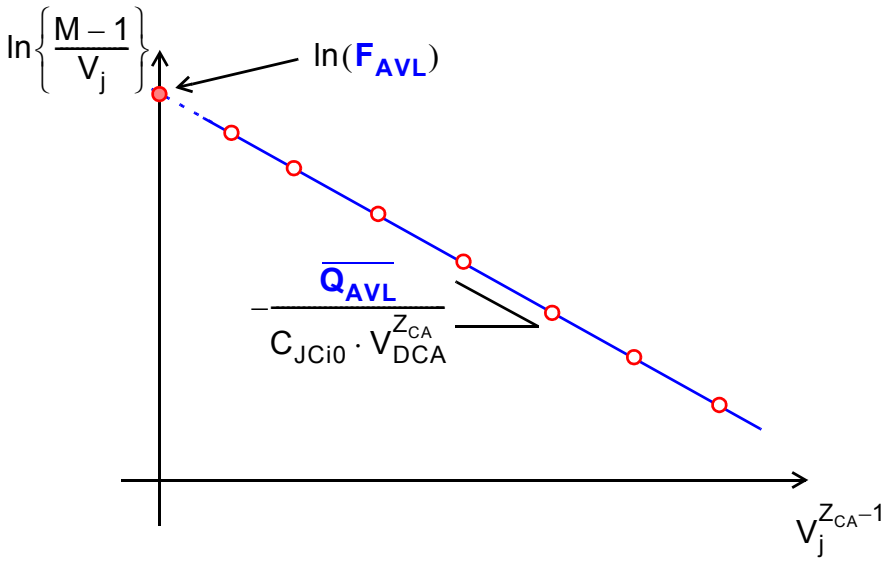
- The same method than the one described in [5] can be used. For M > 1 (avalanche region) and defining $V_J = V_{DCi} - V_{B'C'}$, (6) can be written

$$\ln(M-1) = \ln(\mathbf{F_{AVL}}) + \ln(V_j) - \frac{\overline{\mathbf{Q_{AVL}}}}{\overline{C_{JCi}} \cdot V_j} \quad (7)$$

Substituting in (7) the expression of $\overline{C_{JCi}}$ leads to the final expression

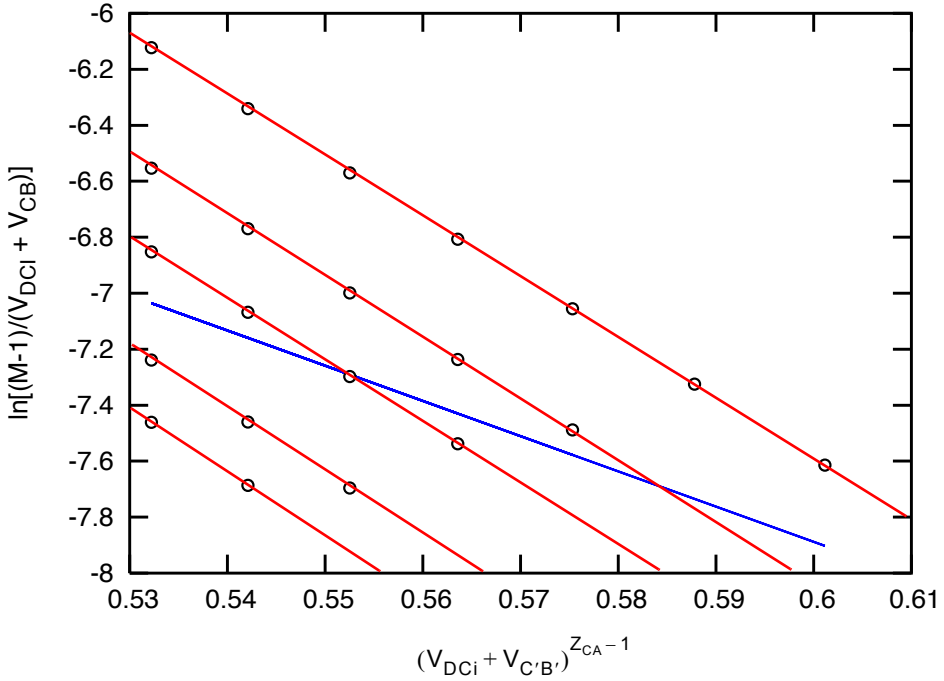
$$\ln\left\{\frac{M-1}{V_j}\right\} = \ln(\mathbf{F_{AVL}}) - \frac{\overline{\mathbf{Q_{AVL}}}}{\overline{C_{JCi0}} \cdot V_{DCA}^{Z_{CA}}} \cdot V_j^{Z_{CA}-1} \quad (8)$$

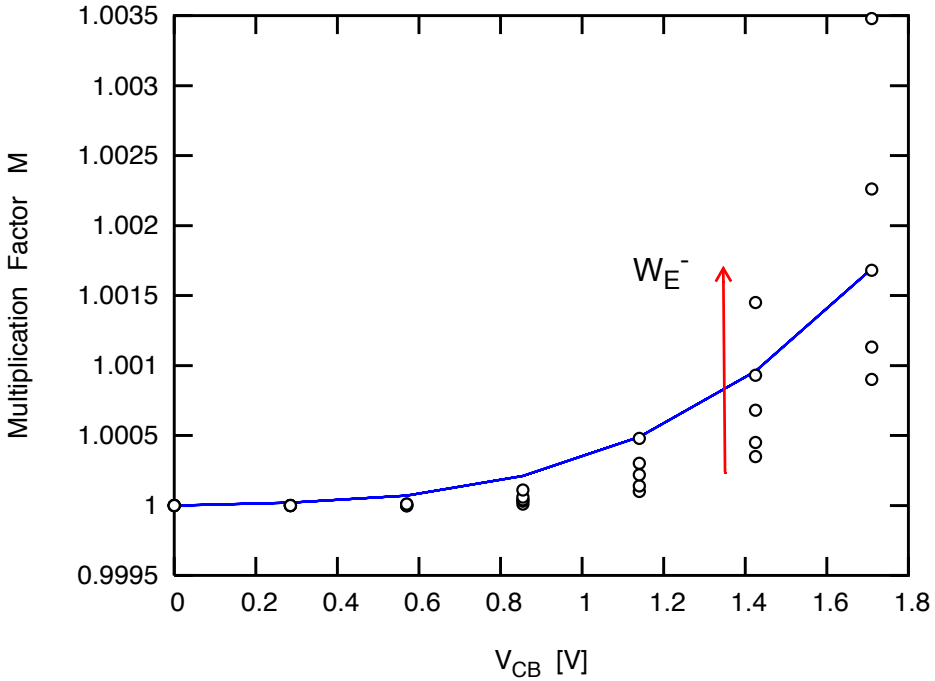
- Therefore, the characteristic $\ln\left\{\frac{M-1}{V_j}\right\}$ versus $V_j^{Z_{CA}-1}$ must be a straight line. The intercept allows to determine $\mathbf{F_{AVL}}$ and the slope $\overline{\mathbf{Q_{AVL}}}$.



Experimental results (see also [6])

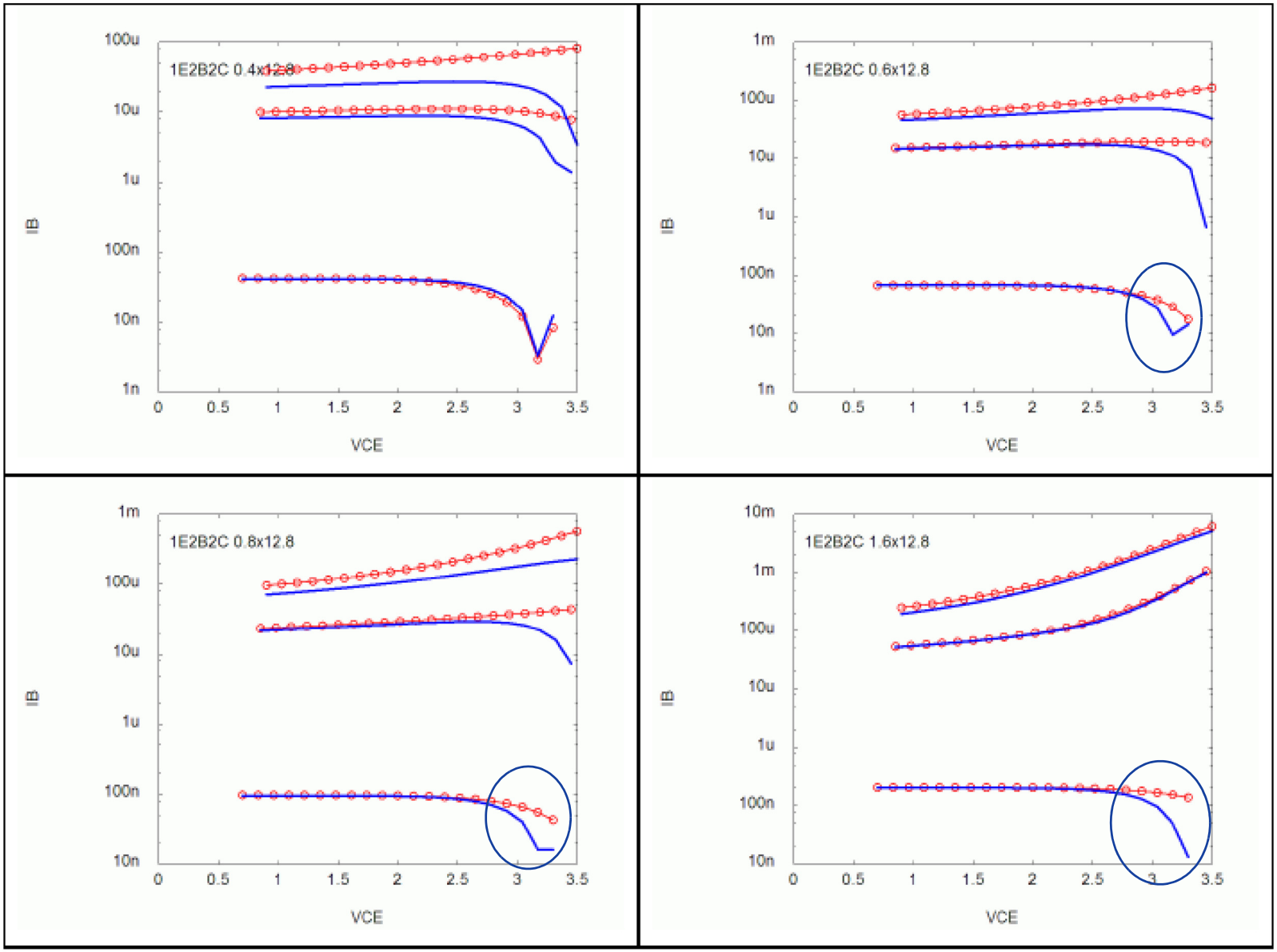
- HS transistors, W_E = 0.25, 0.45, 0.65, 1.05, 1.45 μm, L_E = 12.65 μm



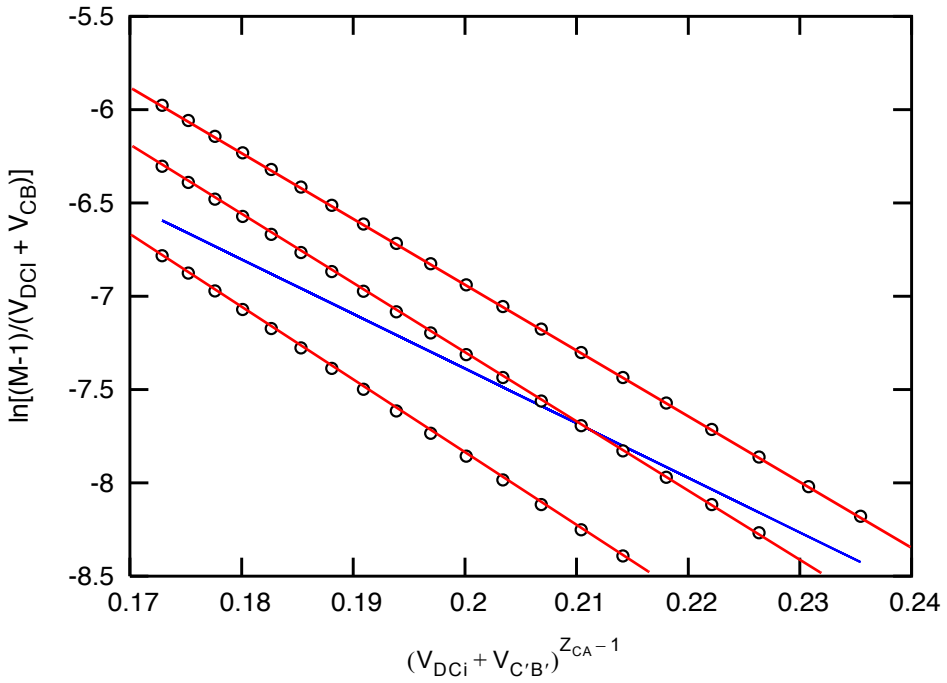


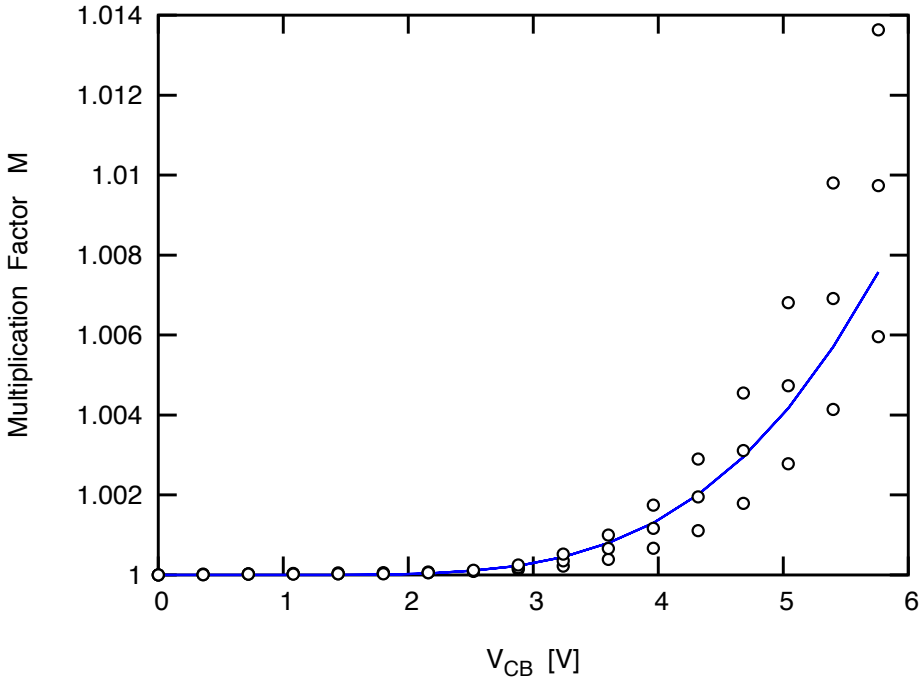
- Contrary to what expected, the multiplication factor M is not independent of the emitter dimensions. M increases when the emitter width decreases.
  - Why? Is it due to non-scalable process or non-scalable model, or wrong geometry scaling rules?
- It is interesting to notice that in fact the characteristics $\ln\{(M-1)/V_j\}$ vs. $V_j^{Z_{CA}-1}$ are all parallel, that demonstrates (i) that **Q_{AVL}** is scalable (slope of the characteristics identical), (ii) that (effective) **F_{AVL}** (deduced from the intercept) is geometry dependent. Why?.

Similar results obtained by XMOD using TRADICA [7]



Same results observed from TCAD simulations





- That partially eliminate the possibility of non-scalable process.
- It remains 2 possibilities (i) non-scalable model or we apply wrong geometry scaling rules.

Analysis and proposal

- If M is not independent on the geometry, from (6) that means that I_{AVL} is not scaled to the effective emitter area A_{E*}.
- This behavior was already shown in [6], where it was found that γ_{AVL} was different from γ_C.

- Therefore, in order to have a scalable multiplication factor, we define an effective area for the avalanche current such as

$$A_{AVL} = (W_{E0} + 2 \cdot \gamma_{AVL}) \cdot (L_{E0} + 2 \cdot \gamma_{AVL})$$

where γ_{AVL} is equal to the ratio of the specific perimeter to the specific area avalanche current $\gamma_{AVL} = \frac{J_{AVLP}}{J_{AVL}}$

- (6) can be re-written

$$M - 1 = \frac{I_{AVL}}{I_{C0}} \approx \frac{J_{AVL} \cdot A_{AVL}}{J_{TF} \cdot A_{E*}} \approx \frac{J_{TF} \cdot A_{AVL} \cdot \mathbf{F_{AVLu}} \cdot (V_{DCi} - V_{B'C'}) \cdot e^{\frac{-\overline{Q_{AVL}}}{\overline{C_{JCi}} \cdot (V_{DCi} - V_{B'C'})}}}{J_{TF} \cdot A_{E*}} \quad (9)$$

$$= \frac{\mathbf{A_{AVL}}}{\mathbf{A_{E*}}} \cdot \mathbf{F_{AVLu}} \cdot (V_{DCi} - V_{B'C'}) \cdot e^{\frac{-\overline{Q_{AVL}}}{\overline{C_{JCi}} \cdot (V_{DCi} - V_{B'C'})}}$$

- Substituting in (9) the expression of $\overline{C_{JCi}}$, and after some calculation, leads to the final expression

$$\ln\left\{\frac{\mathbf{A_{E*}}}{\mathbf{A_{AVL}}} \cdot \left\{\frac{M-1}{V_j}\right\}\right\} = \ln(\mathbf{F_{AVLu}}) - \frac{\overline{Q_{AVL}}}{\overline{C_{JCi0}} \cdot V_{DCA}^{Z_{CA}}} \cdot V_j^{Z_{CA}-1} \quad (10)$$

Similar to (8) by adding the red term.

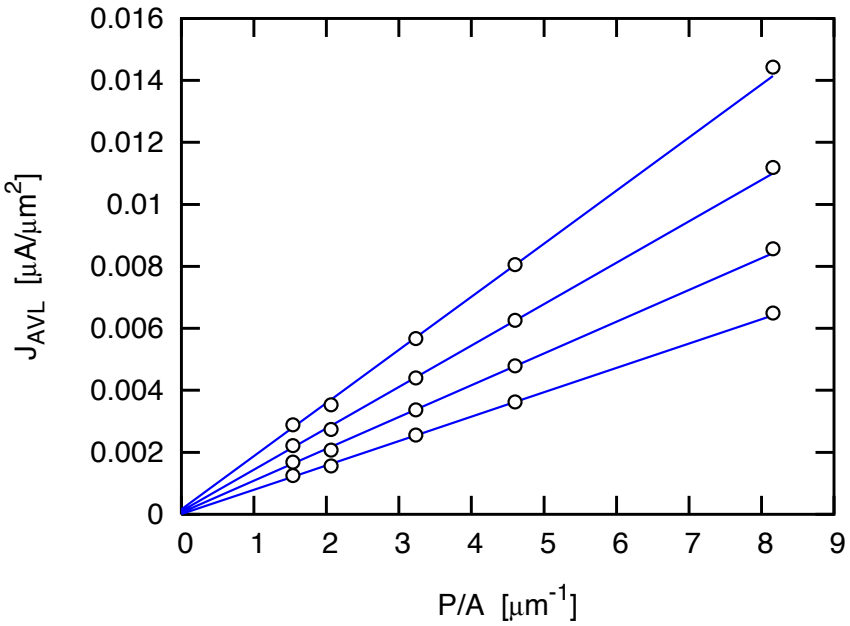
Parameter extraction

- Same straight forward method. Equation (10) must be a straight line, the intercept allows to determine F_{AVLu} and the slope $\overline{Q_{AVL}}$.

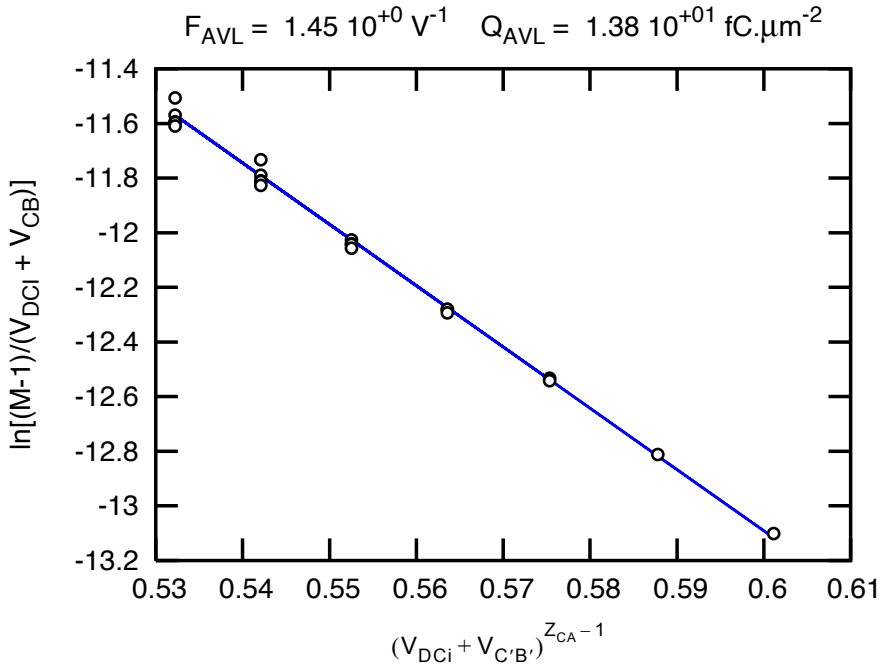
Results

- HS transistors, W_E = 0.25, 0.45, 0.65, 1.05, 1.45 µm, L_E = 12.65 µm

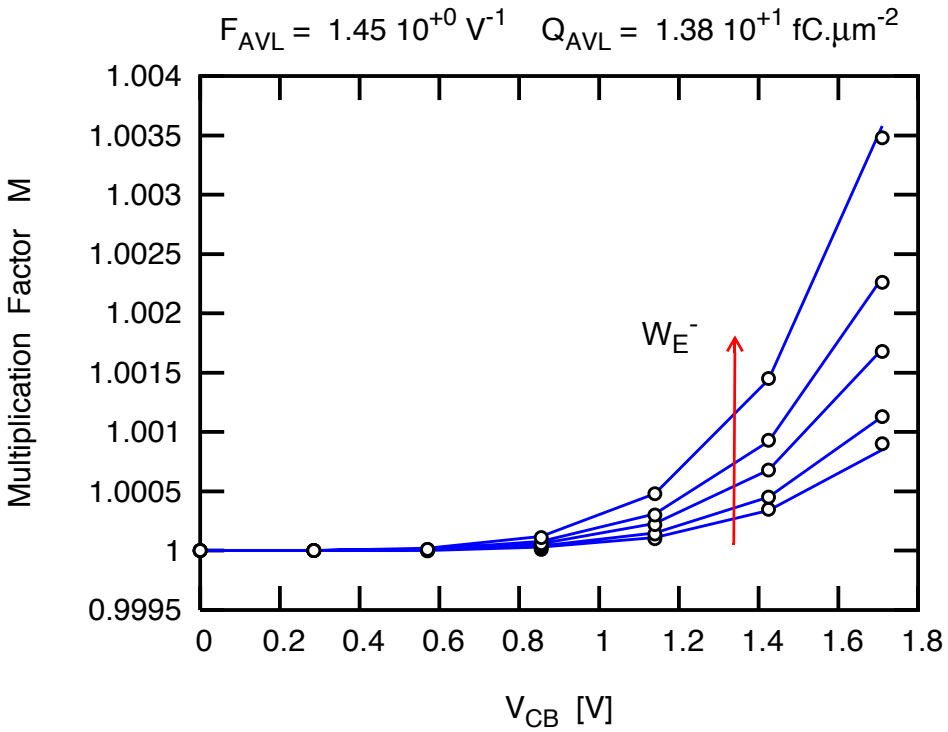
γ_{AVL} determination



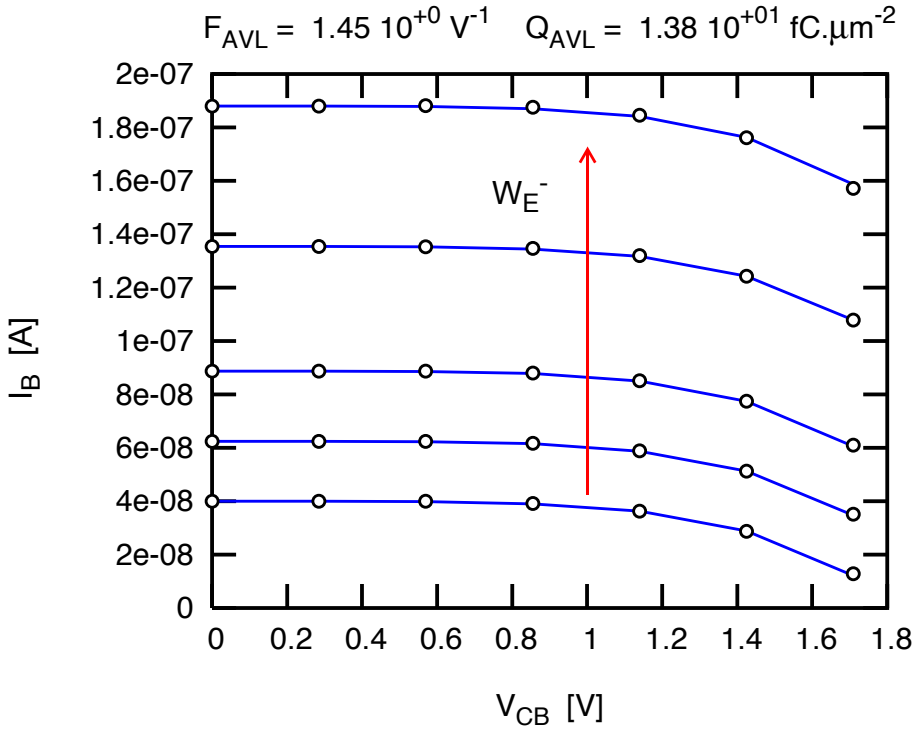
F_{AVLu} and $\overline{Q_{AVL}}$ determination



Multiplication factor



Base current



New geometry scaling laws

$$\begin{cases} Q_{AVL} = A_{C0} \cdot \overline{Q_{AVL}} \\ F_{AVL} = \dfrac{A_{AVL}}{A_{E*}} \cdot F_{AVLu} \end{cases}$$

new!

A_{C0} is the area used to determine the area component of the BC junction capacitance.

Now F_{AVL} is geometry dependant and it is a function of A_{AVL}/A_{E*}

Summary and Comments

- Some geometry scaling rules for HICUM/L2 have been investigated
  - Collector and base current at low current densities.
  - BE and BC depletion capacitances.
  - Weak avalanche current.

- Depending on the technology, the *standard* HICUM geometry scaling laws can pose problems
  - Negative external components.
  - Non-scalable avalanche current.

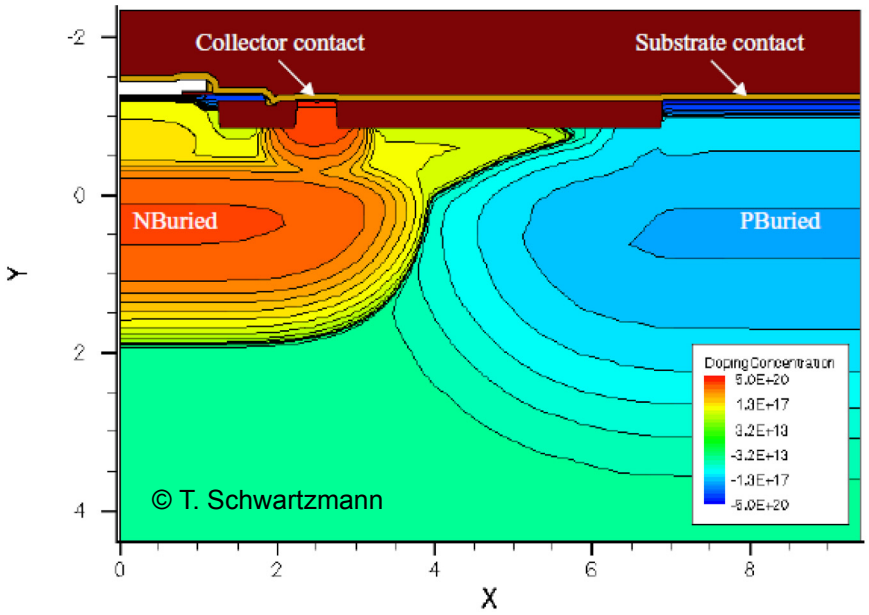
- To avoid these problems, solutions were proposed
  - Feedback, and comments are welcome.

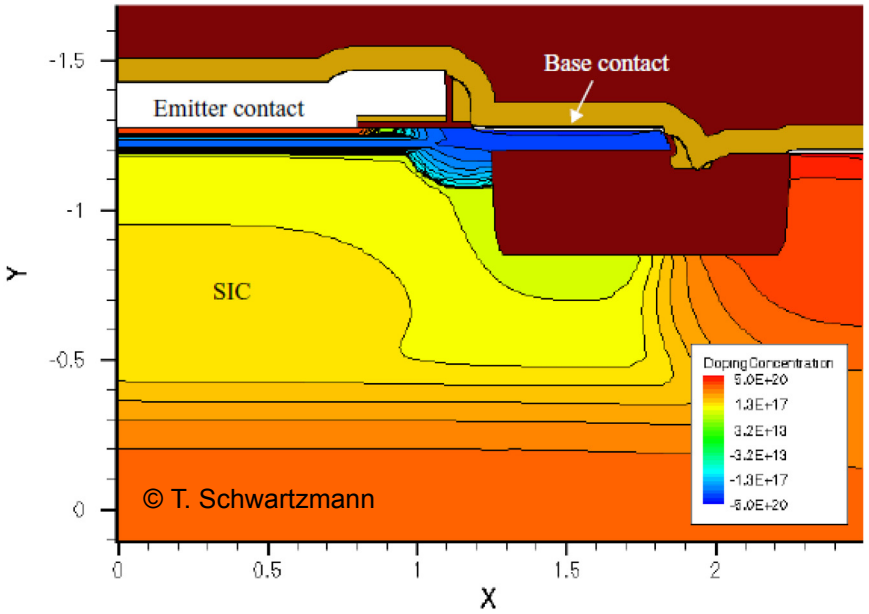
- Work in progress
  - Investigation of other geometry scaling laws (BC and substrate currents, transit time, ...).
  - Detection and study of non-standard geometry scaling effects [9], like WPE (Well Proximity Effects).

- Pending issues
  - h_{JEiu} and h_{JCiu} determination. Today there are assumed to be equal to 1.
  - Validation of the partition of the BE and BC depletion capacitances across the base resistance.
  - Suggestions and help would be welcome...

Acknowledgement

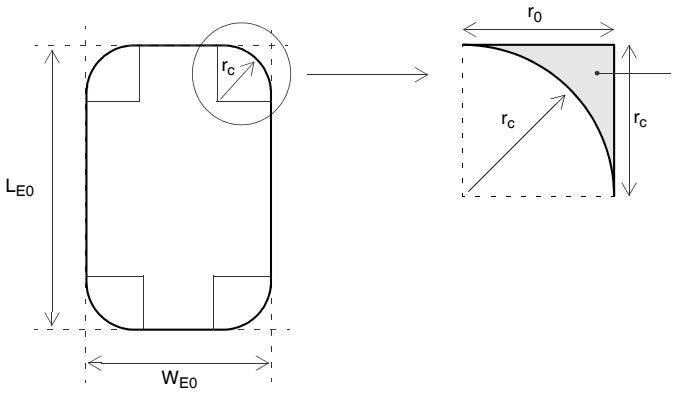
- Thanks to A. Pakfar and T. Schwartzmann [8] for the process and device simulation data used in this presentation.



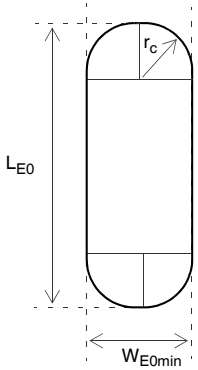


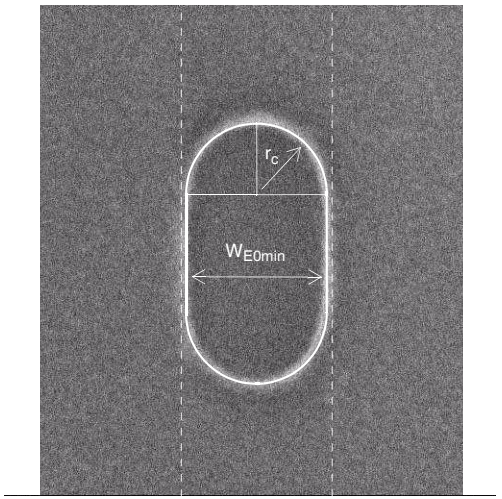
Appendix A Corner Rounding Effects

Actual emitter area A_{E0} and P_{E0} calculation



$$\text{Area} = r_c^2 - \frac{\pi \cdot r_0^2}{4} = r_c^2 \cdot \left(1 - \frac{\pi}{4}\right)$$





- By taking into account the corner rounding, the actual emitter area A_{E0} and perimeter P_{E0} can be expressed as

$$\begin{cases} A_{E0} = W_{E0} \cdot L_{E0} - 4 \cdot r_c^2 \cdot \left(1 - \frac{\pi}{4}\right) = W_{E0} \cdot L_{E0} - \underbrace{r_c^2 \cdot (4 - \pi)}_{\text{Corner rounding}} \\ P_{E0} = 2 \cdot (W_{E0} + L_{E0}) - 4 \cdot 2 \cdot r_c + 2 \cdot \pi \cdot r_c = 2 \cdot (W_{E0} + L_{E0}) - \underbrace{2 \cdot (4 - \pi) \cdot r_c}_{\text{Corner rounding}} \end{cases}$$

- By default r_c is set to $r_c = \frac{W_{E0min}}{2}$, where W_{E0min} is the minimum emitter width allowed in the process.

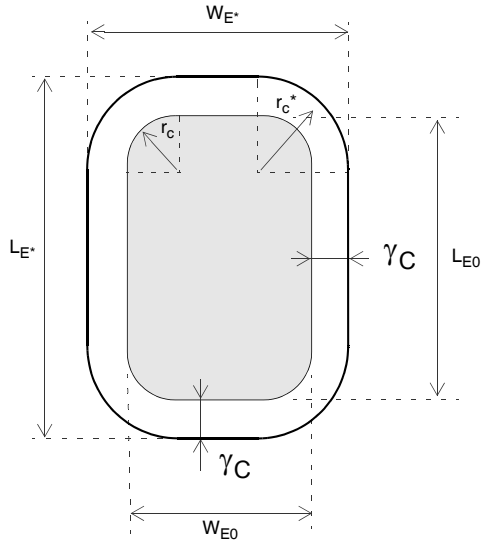
Effective emitter area A_{E*} calculation

- Taken into account the corner rounding, the effective emitter area A_{E*} is expressed as (see A_{E0} calculation)

$$A_{E*} = W_{E*} \cdot L_{E*} - (4-\pi) \cdot r_{c*}^{\,2}$$

Knowing that

$$\begin{cases} W_{E*} = W_{E0} + 2\gamma_C \\ L_{E*} = L_{E0} + 2\gamma_C \\ r_{c*} = r_c + \gamma_C \end{cases}$$



A_{E*} can be rewritten

$$\begin{aligned} A_{E*} &= (W_{E0} + 2\gamma_C) \cdot (L_{E0} + 2\gamma_C) - (4-\pi) \cdot (r_c + \gamma_C)^2 \\ &= W_{E0} \cdot L_{E0} + 2\gamma_C \cdot (W_{E0} + L_{E0}) + 4\gamma_C^2 - (4-\pi) \cdot (r_c^2 + 2\gamma_C r_c + \gamma_C^2) \\ &= \underbrace{W_{E0} \cdot L_{E0} - (4-\pi) \cdot r_c^2}_{A_{E0}} + \underbrace{\{2 \cdot (W_{E0} + L_{E0}) - 2 \cdot (4-\pi) \cdot r_c\} \cdot \gamma_C}_{P_{E0}} + 4\gamma_C^2 - (4-\pi) \cdot \gamma_C^2 \end{aligned}$$

- That leads finally to

$$A_{E*} = A_{E0} + \gamma_C \cdot P_{E0} + \pi \cdot \gamma_C^2$$

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[4] D. Céli, "About h_{jEi} Parameter Extraction", Bipolar Arbeitskreis, Erfurt, October 2006.

[5] D. Céli and D. Berger, "Direct Extraction of Base-Collector Weak Avalanche HICUM Model Parameters", HICUM User's Meeting, Minneapolis, September 2001.

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[7] XMOD, "HICUM Scalable Models for STM BC7RF Process", MINEFI 2005.

[8] T. Schwartzmann, TM07_036, Internal ST report, February 2007.

[9] M. Schröter, S. Lehmann and D. Céli, "Non-Standard Geometry Scaling Effects in High-Frequency SiGe Bipolar Transistors", WCM, NSTI Nanotech 2007, vol. 3, pp. 603-608, May 2007