Non-standard geometry scaling effects in SiGe HBTs

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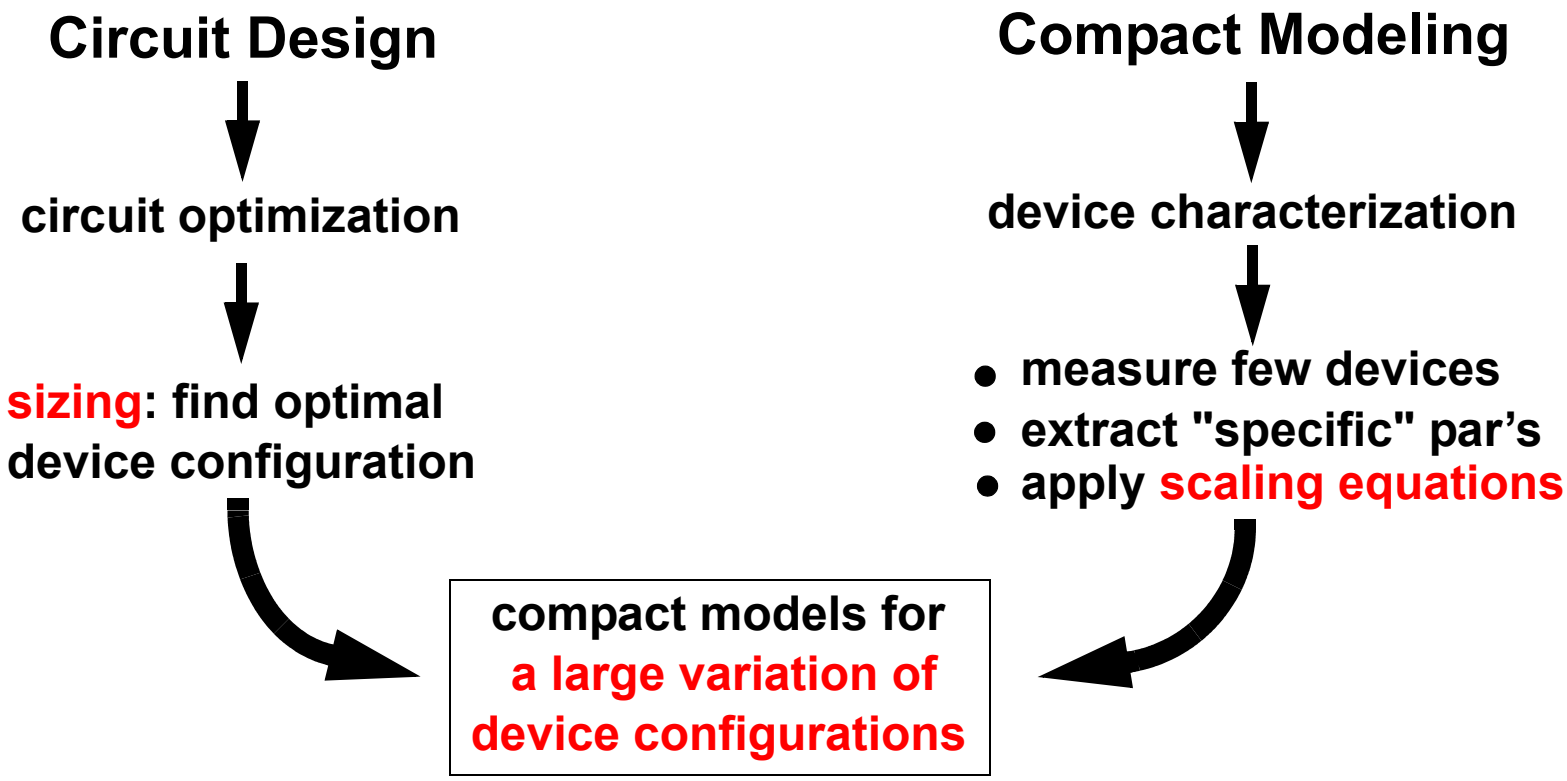
Introduction

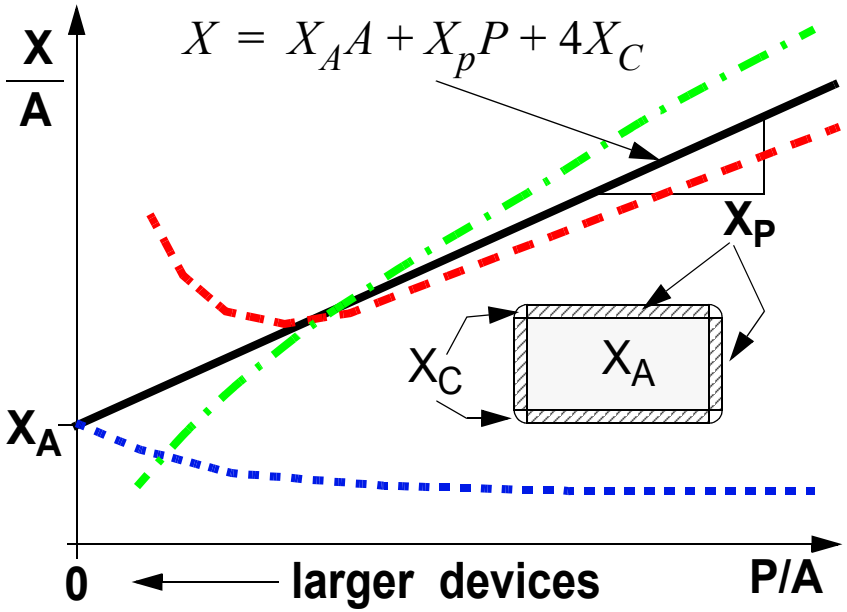


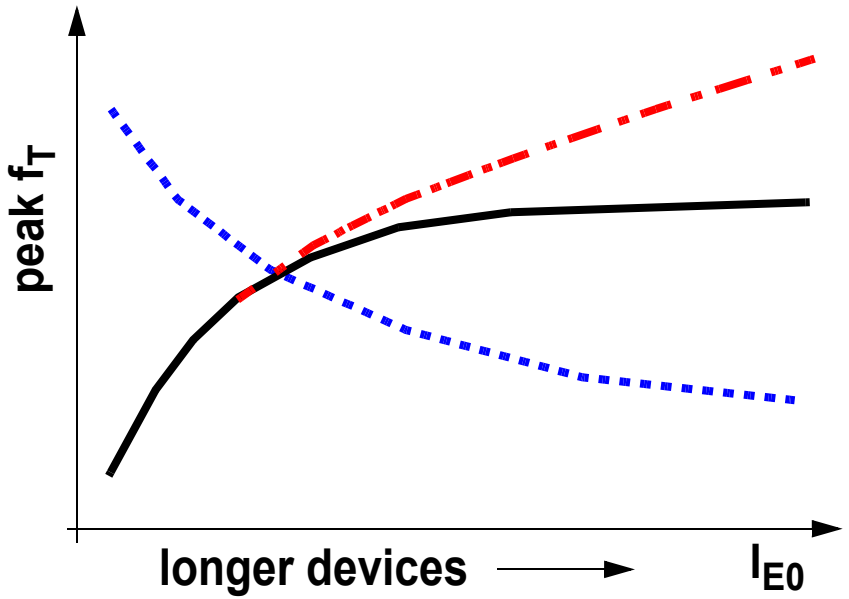
- also: predictive and statistical modeling and design

⇒ **accurate physics-based modeling of geometry scaling effects**

Geometry scaling behavior

- existing geometry scalable models are based on "standard" scaling equation
- in advanced SiGe HBT process technologies: deviations are observed





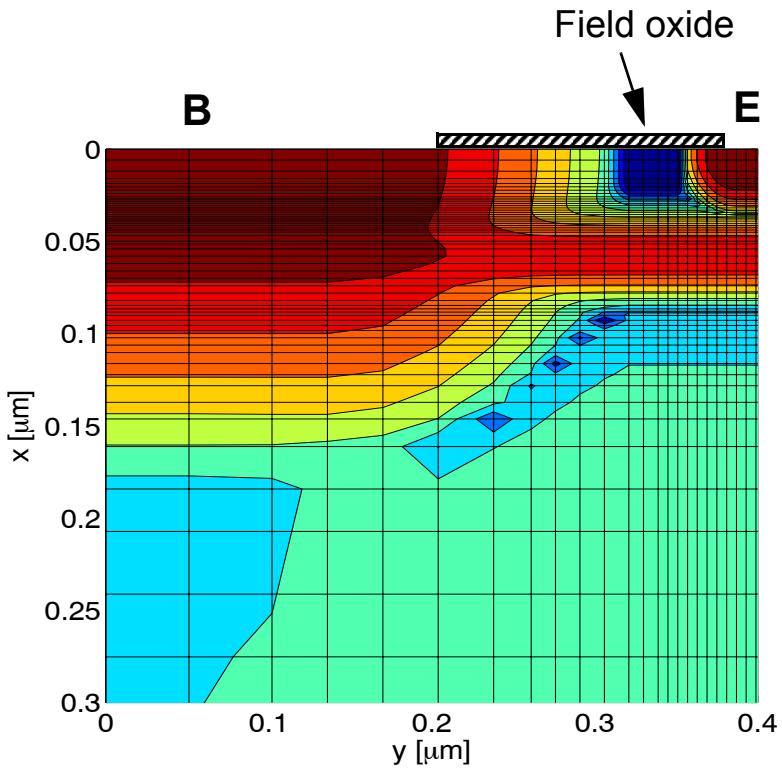
$\Rightarrow$ **accurate modeling of non-standard scaling requires**

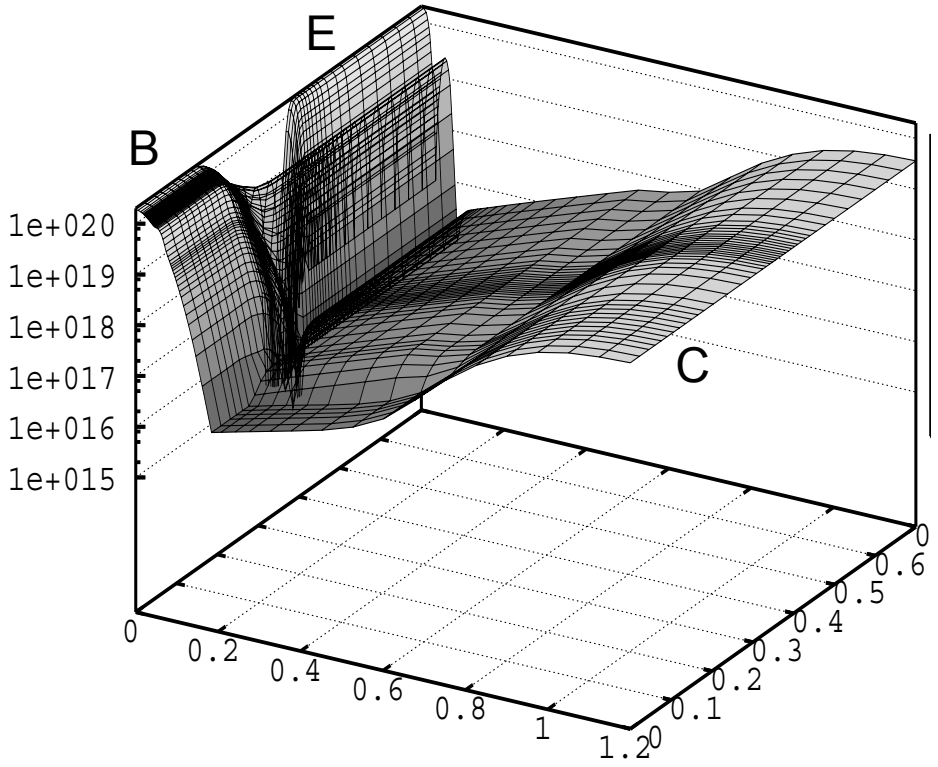
- quantification of impact
- understanding of origin
- suitable scaling equations

Device structures and investigated effects

device simulation of 50GHz production process

- Emitter width: b_{E0} = (0.25, 0.45, 0.65, 1.05, 1.45) µm, unit E length
- reference ("REF") structure: doping and Ge profile do not vary with E width

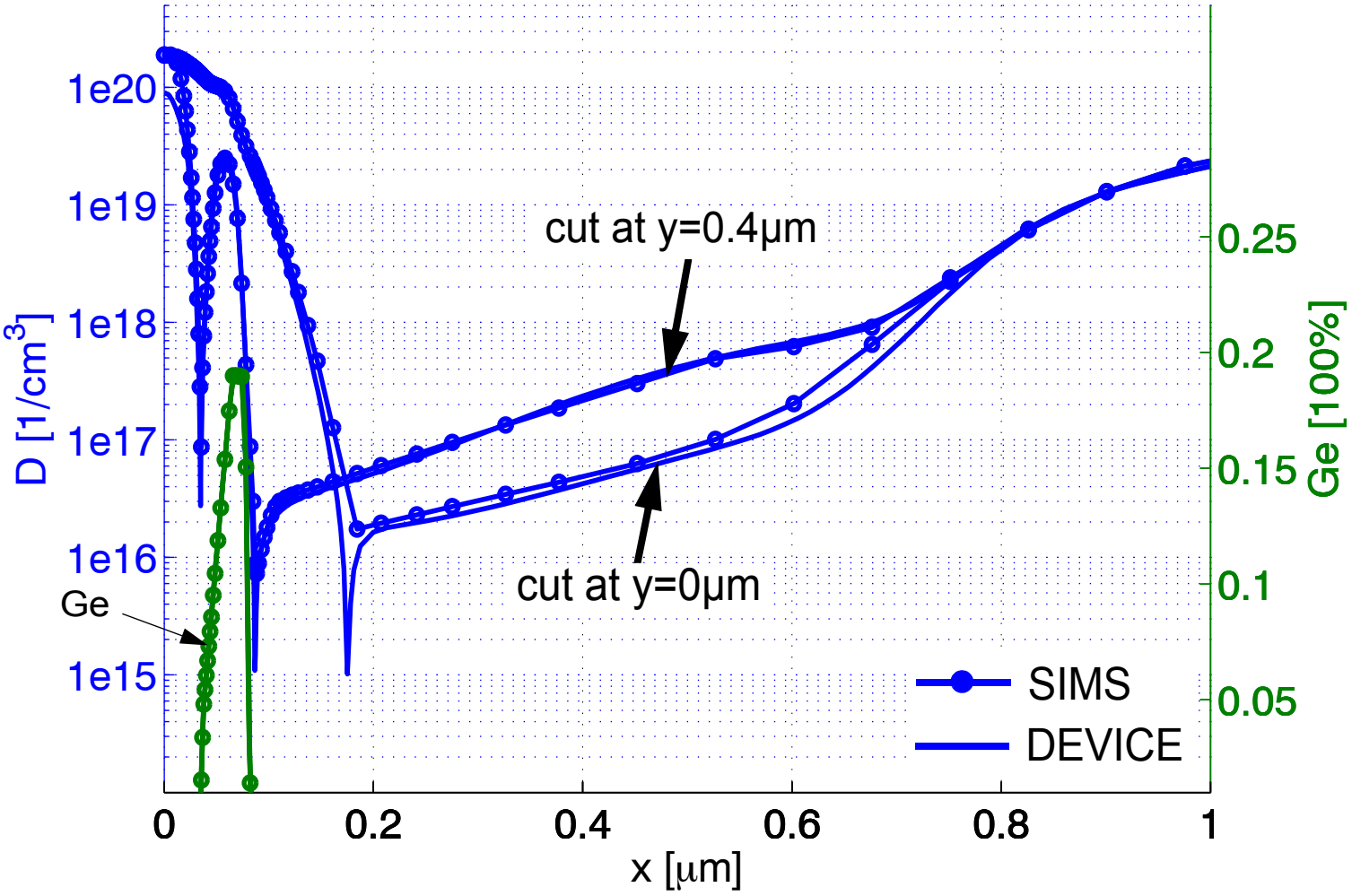




=> reference structure characteristics obey standard scaling rules

Doping profile of reference structure based on SIMS

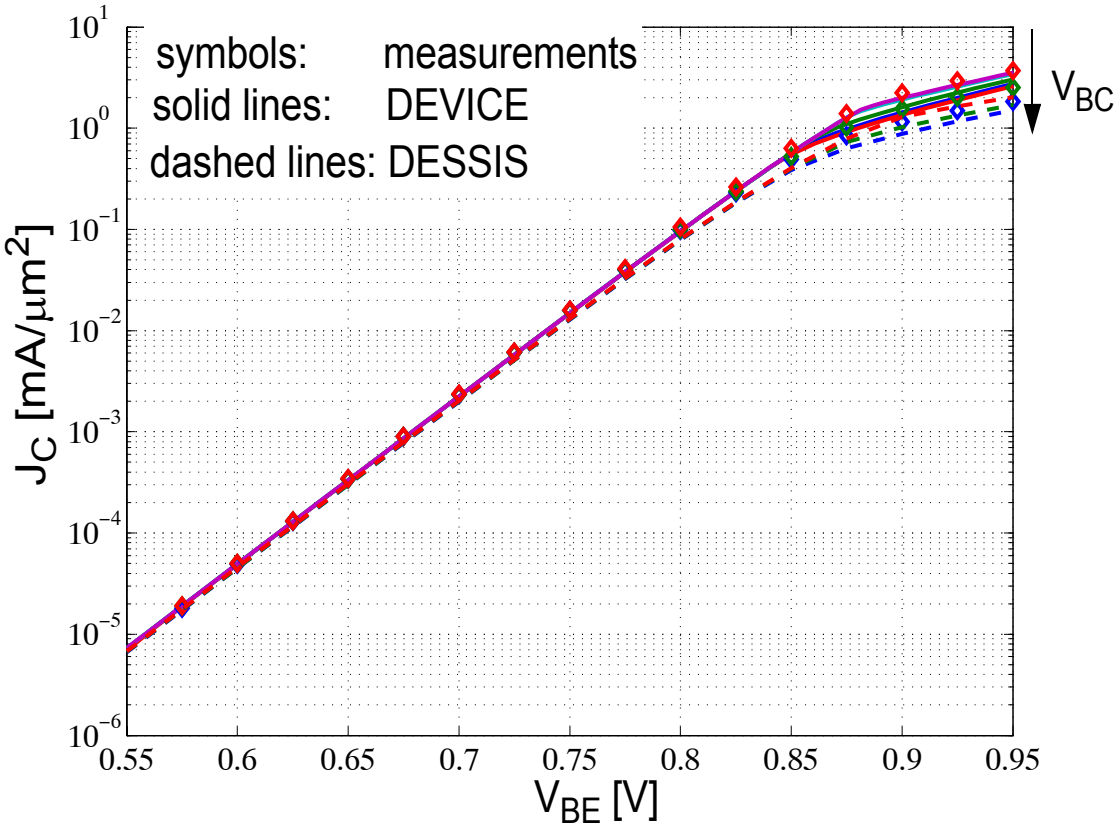
1D Profiles under emitter (y = 0.4μm) and external base (y = 0μm)



DEVICE simulator calibration (reference structure)

based on measurements, comparison also with DESSIS

Gummel plot $V_{BC}/V = 0.5, 0, 1.241$

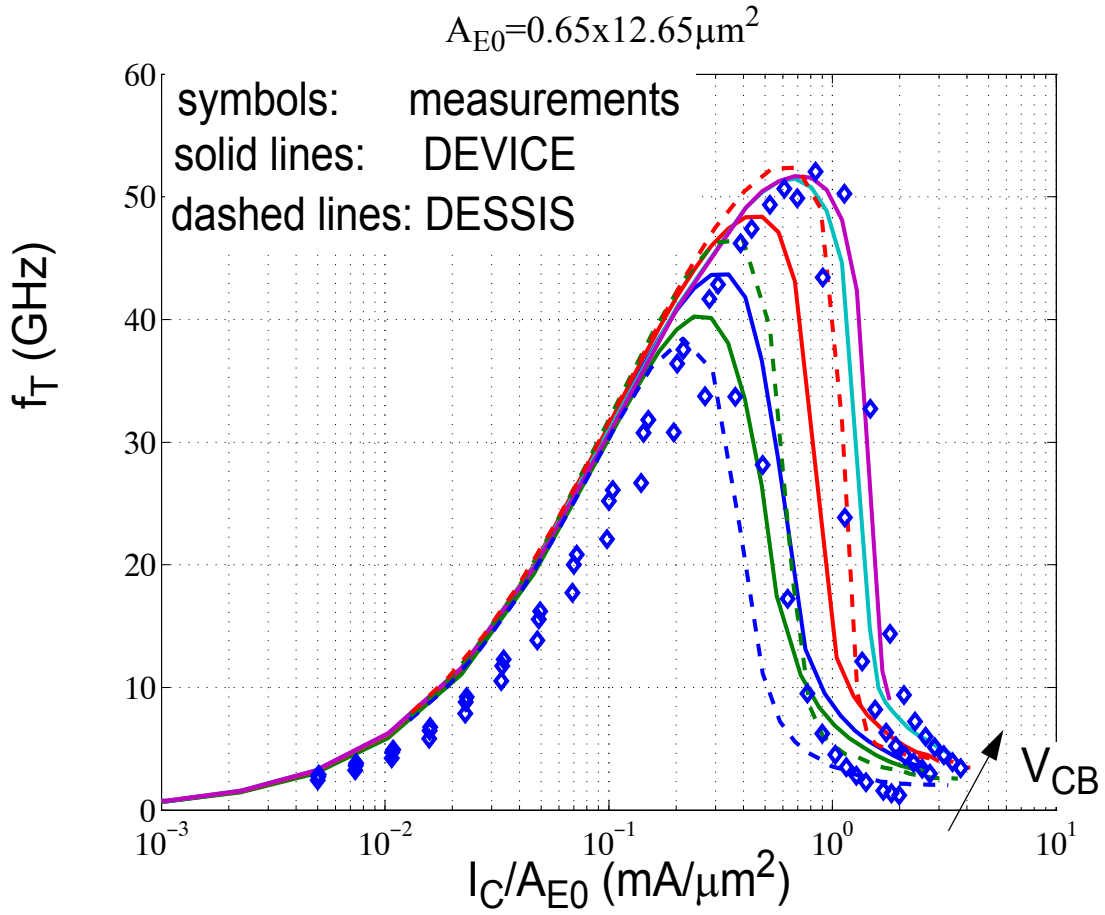


- excellent agreement for low and medium injection
- at high injection:
  - self-heating not included
  - DESSIS with lumped emitter series resistance
- similar agreement also for other characteristics:
  C-V, f_T (incl. parasitics)

$\Rightarrow$ acceptable agreement with experimental data over large bias range

Simulator calibration (cont'd)

transit frequency: comparison DEVICE, measurements, DESSIS

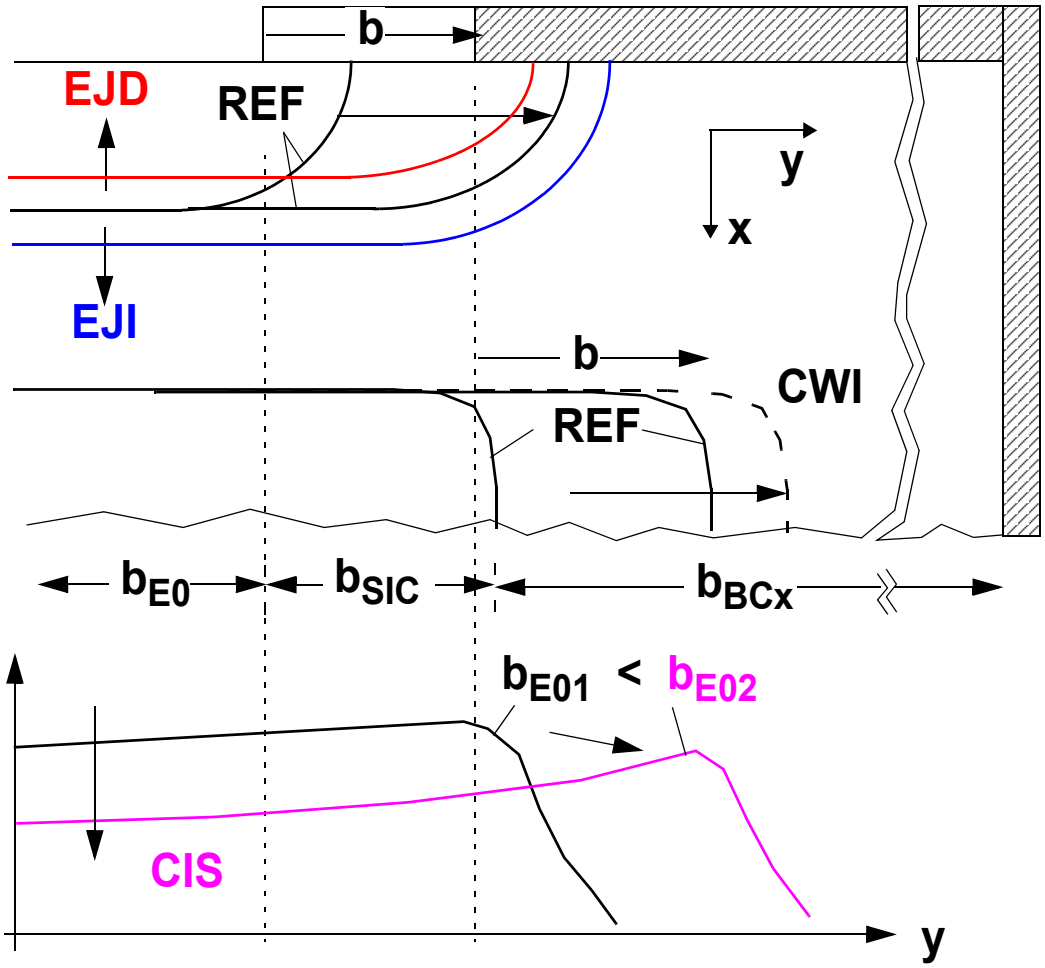


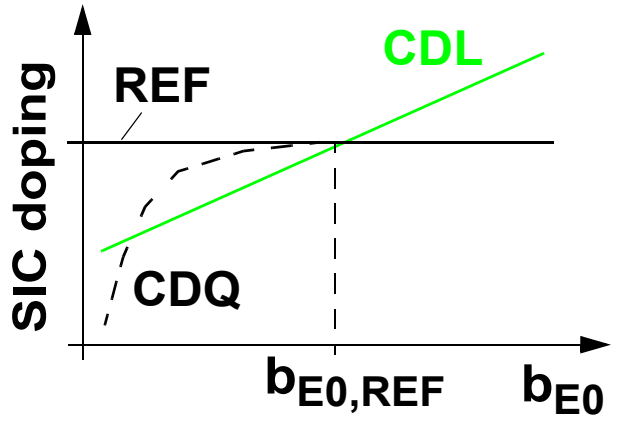
- device simulations are missing parasitics
  => deviation at low J_C
- f_t peak reasonably well approximated
- DEVICE - DESSIS differences caused by mobility differences (mostly Ge dependence description)
- collector voltages:
  meas: V_{BC}=0.5; 0; -1.24V
  DESSIS V_{BC}=0.4; 0; -1.72V
  DEVICE V_{BC}=0.4; 0.5; 0; -1.24; -1.72V

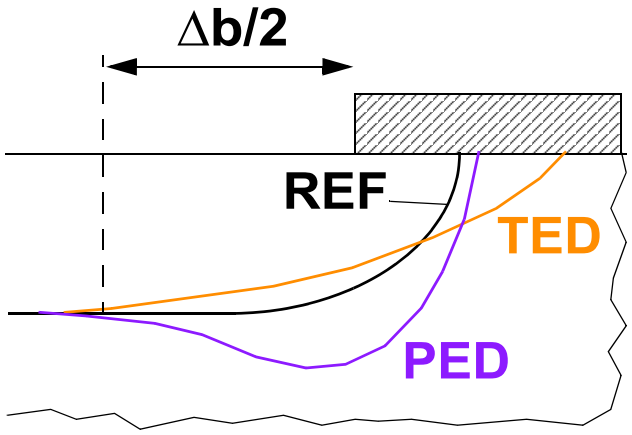
$\Rightarrow$ acceptable agreement with experimental data over large bias range

Scaling effects investigated

reference width $b_{E0,REF}$ = 0.65 μm



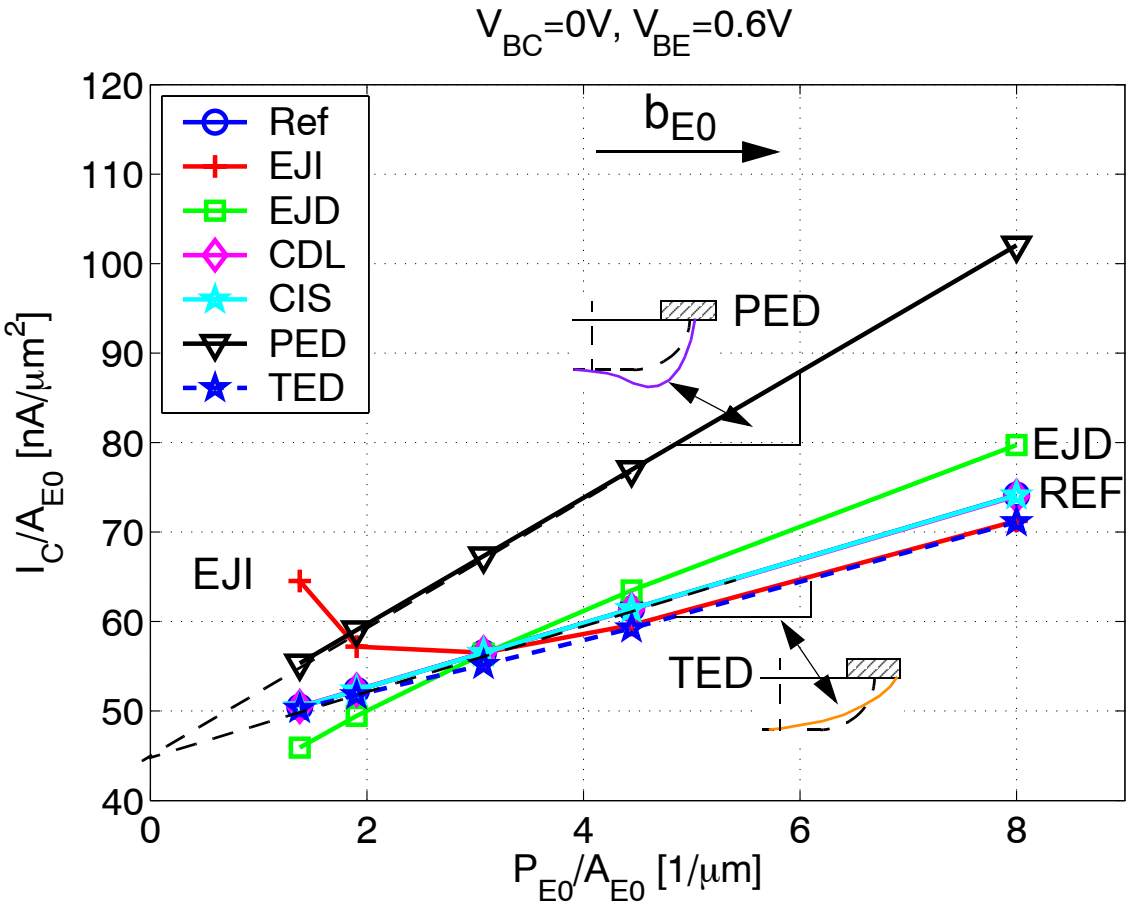




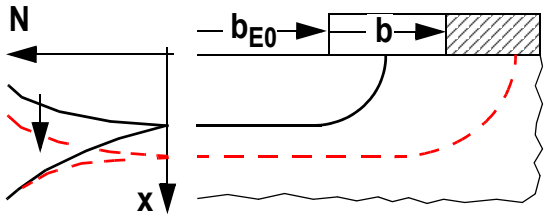
selected parameters for comparison: mostly process control monitors

Simulation Results

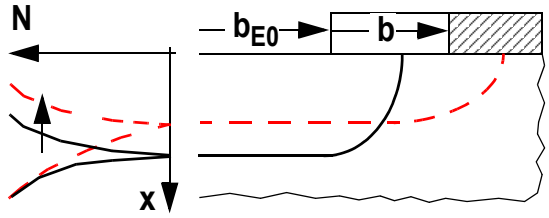
low-injection collector current



- PED, TED: only different slope
- EJI: non-standard sc.



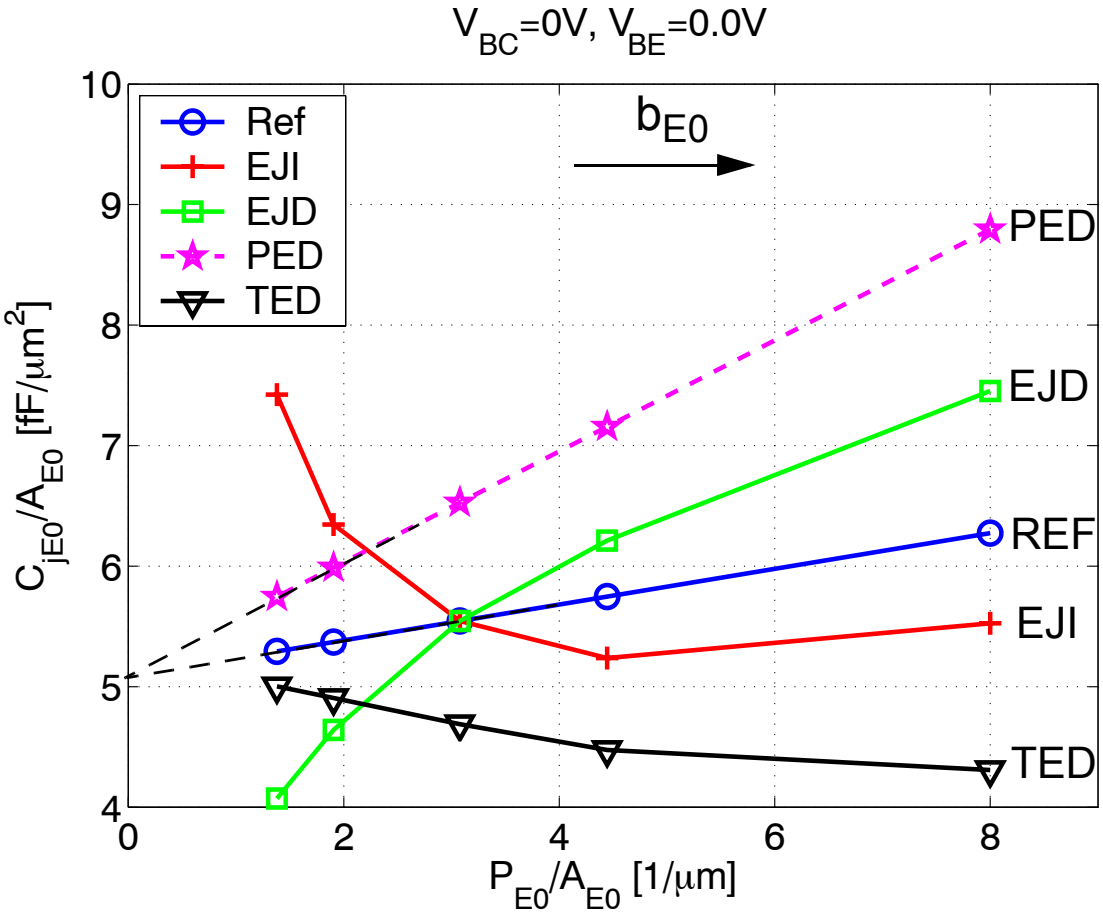
- EJD: non-standard sc.



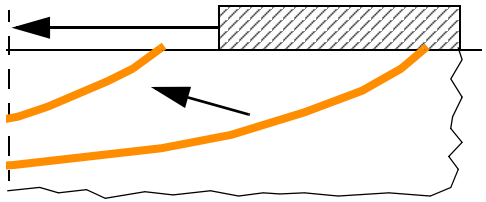
$\Rightarrow$ detection possible for junction depth variation (EJI, EJD)

Geometry effects

zero-bias BE depletion capacitance



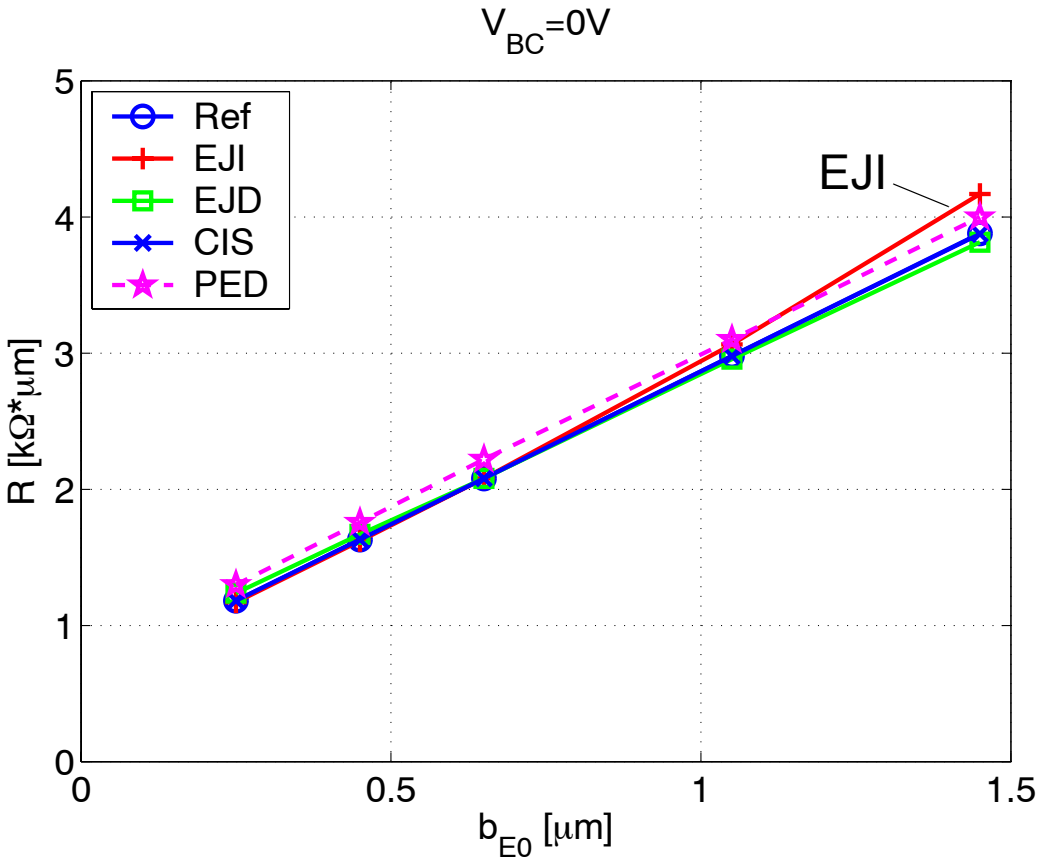
- behavior similar to I_C
- TED: *negative* slope and non-linear scaling



⇒ detection possible for EJI, EJD, and TED

Geometry effects

zero-bias base resistance (from tetrode structures)



- standard scaling:

$$R_{B0} = r_{SBi0} b_{E0} + 2(r_{Ss} b_s + R_x)$$

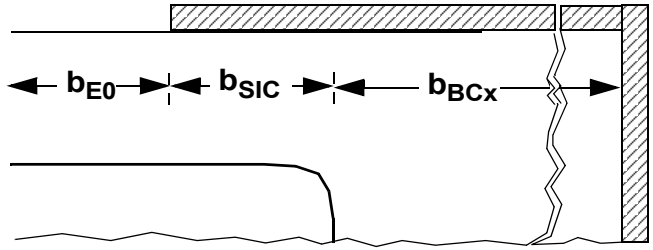
- observed with slightly different
  - slope (rSBi)
  - intercept (rSs)
- non-standard scaling: EJI
- variations within process tolerances

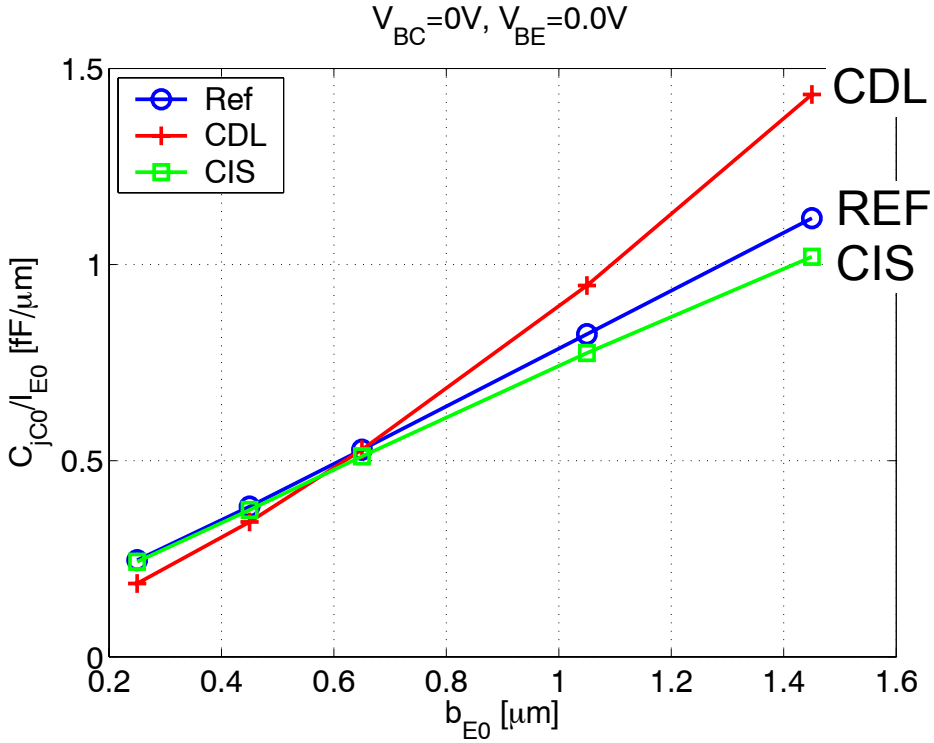
$\Rightarrow$ overall: fairly small variation in HBTs (as opposed to BJTs)

Geometry effects

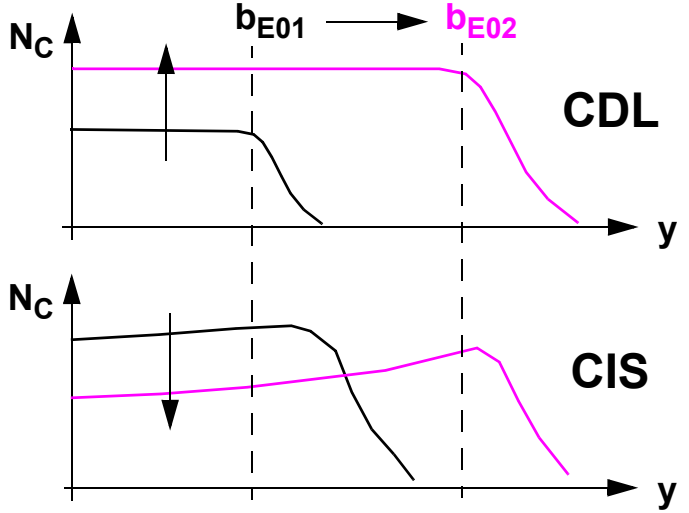
zero-bias BC depletion capacitance

- standard scaling according to: $C_{jC} = C_{jCi,A}(b_{E0} + b_{SIC}) + 2C_{jCx,A}b_{BCx}$
  ((TED, PED, EJI, EJD) = REF)



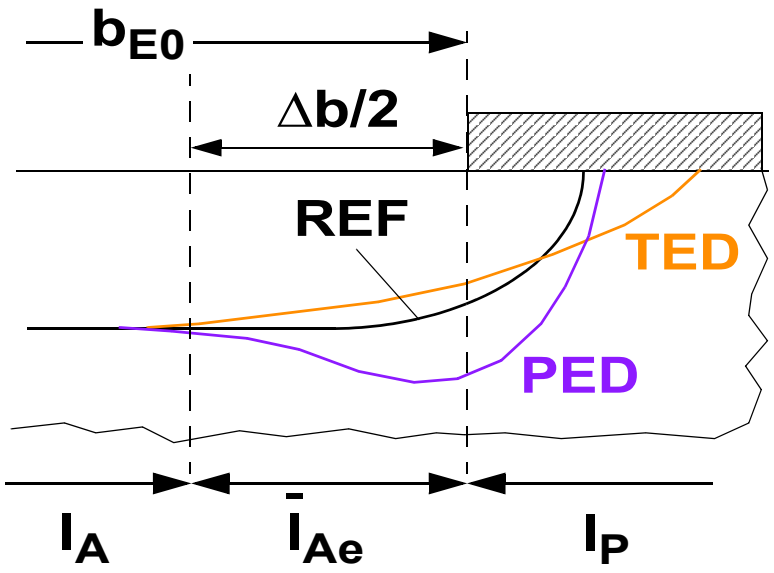


- non-standard scaling



⇒ CIS is hardly detectable from BC depletion capacitance!

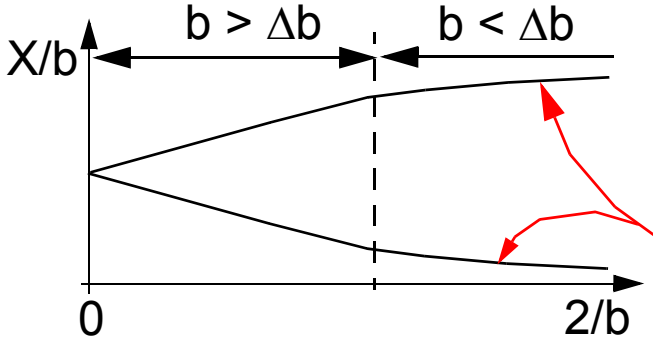
Discussion



- consider 2D case (long transistor)

$$I = I_A(b_{E0} - \Delta b) + \overline{I_{Ae}}\Delta b + 2I_P$$

- for $b_{E0} < \Delta b$: $I = \overline{I_{Ae}}(b_{E0})b_{E0} + 2I_P$



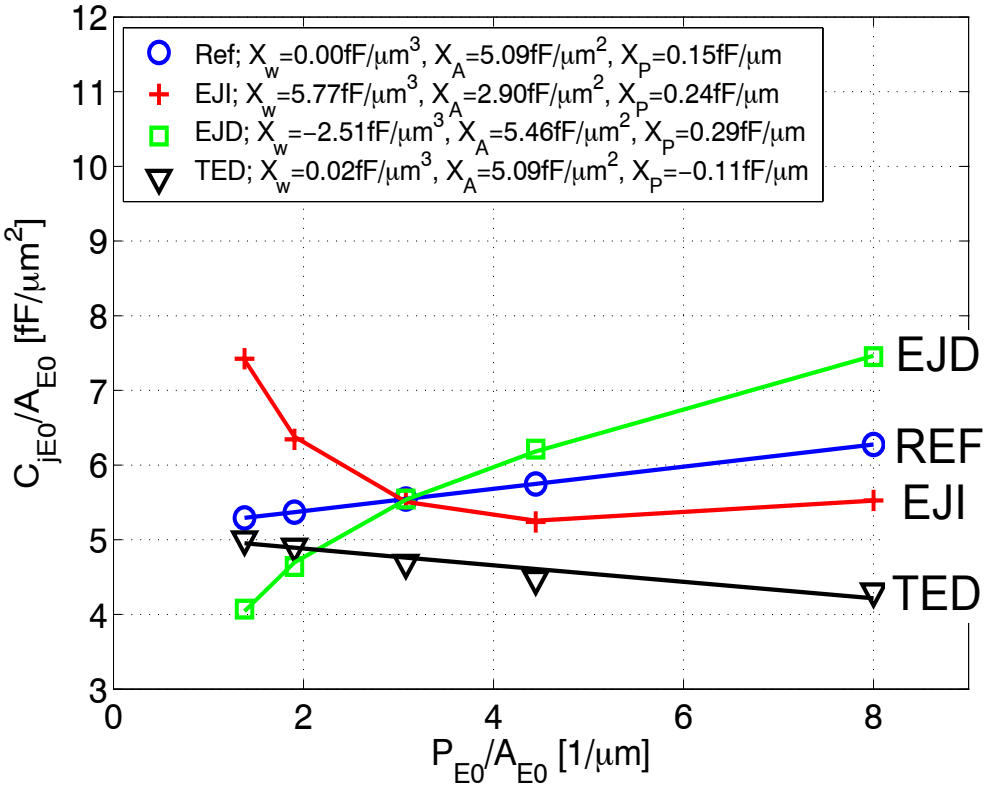
- in general for X (= I, Q, C) and b (= b_{E0},b_{BC},...):

$$\frac{X}{b} = \begin{cases} X_A + \left[(\bar{X}_{Ae} - X_A)\dfrac{\Delta b}{2} + X_P\right]\dfrac{2}{b} & , b > \Delta b \\ \bar{X}_{Ae}(b) + X_P\dfrac{2}{b} & , b \le \Delta b \end{cases}$$

$\Rightarrow$ standard scaling (with different slope) for b > Δb

Generic equation for describing non-standard scaling

$$\frac{X}{A} = \frac{X_w}{(P/A)} + X_A + X_P\frac{P}{A} + X_n\left(\frac{P}{A}\right)^2, \quad 1 >> b$$



- standard scaling equation:

$$X_A + X_P\frac{P}{A}$$

- wide emitter effects: X_w
- narrow emitter effects: X_n
- user-defined scaling with TRADICA "poly" function:

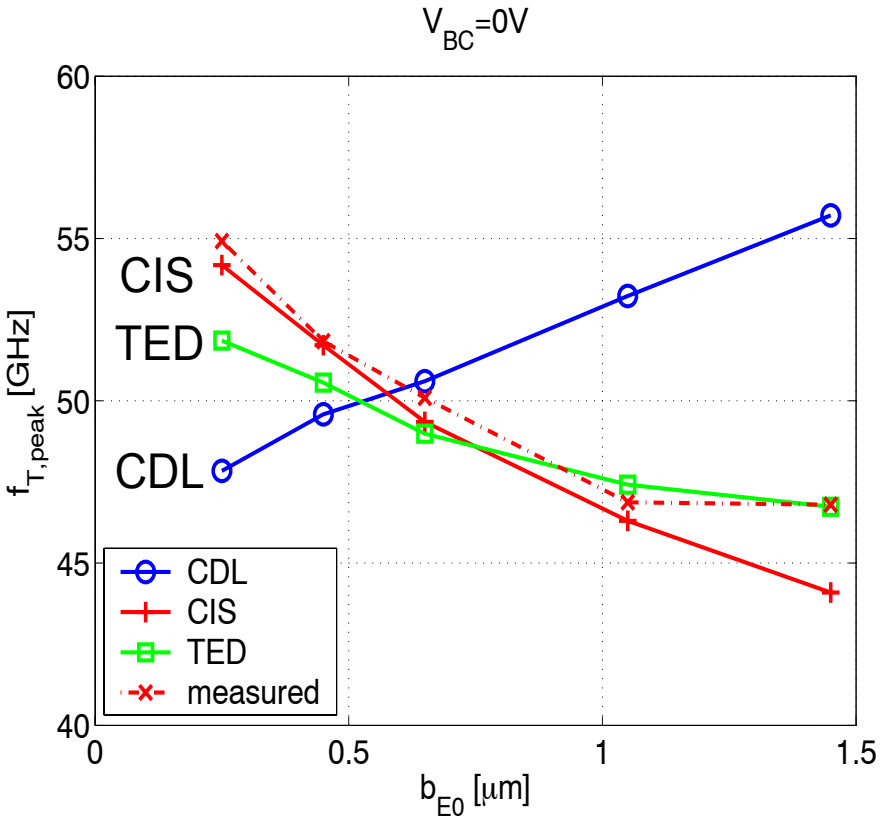
  - set $X_A^{\#} = X_A + \frac{X_w}{P/A}$

  - set $X_P^{\#} = X_P + X_n\frac{P}{A}$

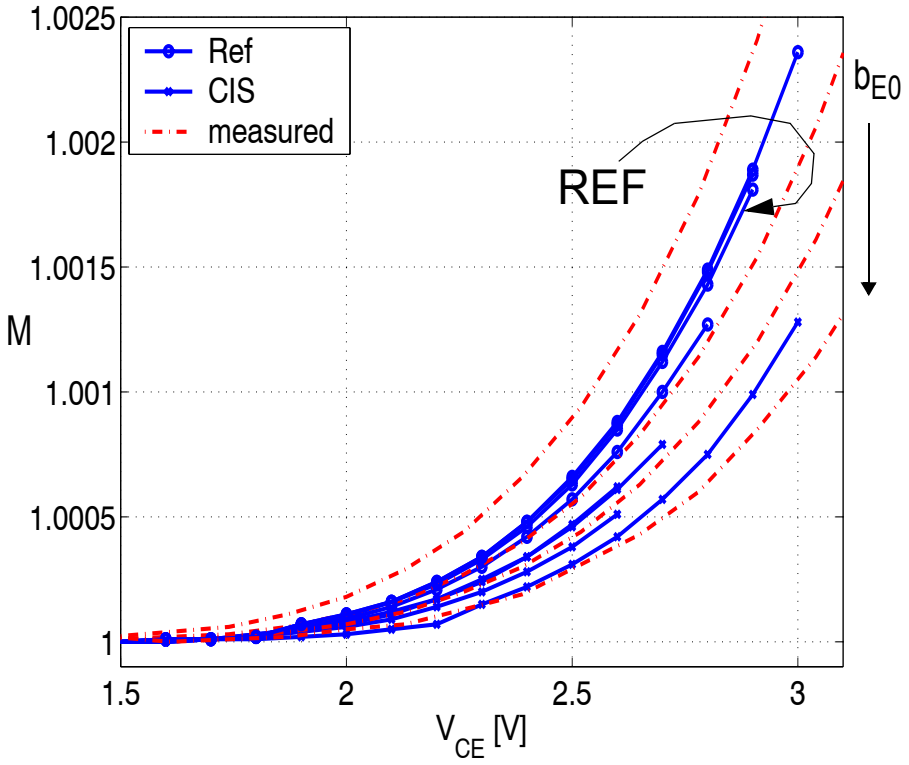
$\Rightarrow$ accurate approximation

Experimental Results

transit frequency



avalanche multiplication factor



$\Rightarrow$ trend follows CIS

$\Rightarrow$ trend follows CIS

$\Rightarrow$ not detectable from BC depletion capacitance

Conclusions

- many effects can lead to deviations from standard geometry scaling behavior
- non-standard scaling cannot be detected from cases with just different slopes
- need to look at sufficiently large set of characteristics to detect profile variations and most likely cause
- non-standard geometry scaling can be modeled analytically
  - directly in "specific electrical" parameter calculation
  - preferable: in technology parameters (e.g. average doping) => to be derived yet

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