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ÉCOLE NATIONALE SUPÉRIEURE D'INGÉNIEURS DE CAEN
& CENTRE DE RECHERCHE

Perraud Jean Claude 18 june 2007 < perraud@ecole.ensicaen.fr >

New Models into SPICE

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Using an *Improved* Advanced Verilog A Model compiler for SPICE 3F5

(2007 : directly from Compiler , does as Built-In C models)

1- New features of the new Verilog A Model compiler :
my proposal of New extensions for Verilog :
Alias, Init, Limit, Csource features

2- Simulations Results : behaviour and simulation
=> simple and complex circuits
=> not saturated and hard saturated
=> Existing Built IN Gummel-Poon Spice model
versus
some Other models compiled using this new Verilog A Compiler
a) Standard Gummel-Poon no Init && limit Functions
b) Gummel-Poon Model with Init && limit Functions
c) Gummel-Poon Model SELF HEATING and Init && limit
c1) when SELF HEATING OFF
c2) when SELF HEATING ON
d) Hicum models
Level 0 (2007)
Level 2V2.1 (2006)
Level 2V2p22 (2007)

3- Remaining Works ...

4- Other Developments

5- CONCLUSIONS

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1- New features of the new Verilog A Model compiler :

my proposal of New extensions for Verilog :

Alias, Init, Limit, Csource features

1-1 ALIAS :

ex: "alias fgeo fge0 " ....

to define an equivalent name for a parameter name

1-2 1 INIT function per model :

ex: " initnode function InitCond ;"

to define the Analysis starting values of model nodes
as it is done in Built IN Spice models

1-3 1 LIMIT function per model :

ex: " limitnode function LimitCond ;"

to limit the values of model nodes when iterate , exactly
as it is done in Built IN Spice models

1-4 C source Functions :

ex: " csource function real devpnjlim ;"

can only be used in Init function && Limit function
to simplify the code of Init function && Limit function,

Does exactly as it is done in Built IN Spice models

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2- Simulations Results : (behaviour and simulation times)

=> simple and complex circuits

=> not saturated and hard saturated

=> comparison between :

Existing Built IN Gummel-Poon Spice models

versus

some models compiled using this new Verilog A Compiler

a) Standard Gummel-Poon no Init && limit Functions

b) Gummel-Poon Model with Init && limit Functions

c) Gummel-Poon Model && SELF HEATING && Init && limit

c1) when SELF HEATING OFF

c2) when SELF HEATING ON

1. **Hicum models**
   - **Level 0 (2007)**
   - **Level 2V2.1 (2006)**
   - **Level 2V2p22 (2007)**

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2.1- GUMMEL-POON :

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Goal for these simulation results :

It is to compare the simulation results (behaviour & time) ,
using the same circuits , (increased time when adding self heating features ...)
the same model , the same model parameters ...same circuits ...
(same equations, derivatives slightly different ...),

ie : Philips - SUBILO 6 GHz NPN, CBEB, EMIT SIZE = 2.0X9.0 UM**2

NO Manual OPTIMISATIONS ..... (but with Init Limit function in Verilog A)

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for the following models :

GUMSTD Model GummelPoon Standard Binary Build IN Into Spice - With Init Limit function
GUM1 Model GummelPoon from Verilog A - NO self heating - NO Init Limit function
GUM2 Model GummelPoon from Verilog A - NO self heating - With Init Limit function
GUM3 Model GummelPoon from Verilog A - self heating OFF - With Init Limit function-5nodes
GUM4 Model GummelPoon from Verilog A - self heating ON - With Init Limit function-5nodes

using the following circuits : ECL Ring Oscilator -21 stages - D. Celi (ST) -

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ring1 : NO SAT ECL Ring Osc - Valim = 2.7 V (R1:4000, R2:4000, R3:8000)
ring2 : NO SAT ECL Ring Osc - Valim = 5.2 V (R1:4000, R2:4000, R3:8000)

ringS1 : SAT ECL Ring Osc - Valim = 2.7 V (R1:4000, R2:4000, R3:4000)
ringS2 : SAT ECL Ring Osc - Valim = 5.2 V (R1:4000, R2:4000, R3:4000)

ringHS1 : HARD SAT ECL Ring Osc - Valim = 2.7 V (R1:4000, R2:4000, R3:2000)
ringHS2 : HARD SAT ECL Ring Osc - Valim = 5.2 V (R1:4000, R2:4000, R3:2000)

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2.2- HICUM :

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Goal for these simulation results :

It is to compare the simulation results (behaviour & time) , using the same circuits , using the HICUM model 2 22 :

"Version mars 2006" versus "Version october 2006" ,

using the same model parameters (previous ST Model parameters) ...

NO Manual OPTIMISATIONS ... (but with Init Limit function in Verilog A)

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Model HICUM Level_2 Version 2.21:

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simulations done in Nov 2006 from Verilog A - With Init Limit function in Verilog A

hic2221.va : version March 2006 : updated November 2006 (Init && Limit)

with Init and Limit function into the Verilog A , with SELF HEATING (5 ext nodes)

- **When self heating OFF**
- **When self heating ON**

Model HICUM Level_2 Version 2.22:

****

simulations done in Nov 2006 from Verilog A - With Init Limit function in Verilog A

hic2222.va : October 2006 :

with Init and Limit function into the Verilog A , with SELF HEATING (5 ext nodes)

- **When self heating OFF**
- **When self heating ON**

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1rst SIMULATIONS RESULTS

Units : OP : (iter) ImpOP: (iter) TRAN: (iter) AnalTime : (sec) loadTime: (sec)

	GUMSTD Std Build-In With LimInit NO SHT	GUM1 From VA NO LimInit NO SHT	GUM2 From VA With LimInit NO SHT	GUM3 From VA With LimInit SHT OFF	GUM4 From VA With LimInit SHT ON	HICUM2221 From VA With LimInit SHT OFF	HICUM2221 From VA With LimInit SHT ON	HICUM2222 From VA With LimInit SHT OFF	HICUM2222 From VA With LimInit SHT ON
NO SAT (ring1)									
ECL Ring Osc									
Valim = 2.7 V									
OP	6	*	6	6	9	7	8	7	8
ImpOP	(G40)323	(G40)325	16	16	16	11	11	10	10
TRAN	5122	5591	6089	6089	9751	3359	3620	3278	3639
AnalTime	6.865	12.90	12.15	15.44	23.90	28.53	30.97	17.85	24.91
loadTime	1.97	7.63	7.90	10.18	17.49	26.04	28.32	15.40	22.22
NO SAT (ring2)									
ECL Ring Osc									
Valim = 5.2 V									
OP	9	*	6	6	10	7	9	9	10
ImpOP	(G40)328	*	15	15	15	9	10	9	9
TRAN	5208	*	6110	6108	10181	3365	3992	3349	3830
AnalTime	6.65	*	11.89	15.13	24.29	27.71	34.15	16.52	27.24
loadTime	1.89	*	7.53	9.96	17.86	25.16	31.15	14.11	24.40
SAT (ringS1)									
ECL Ring Osc									
Valim = 2.7 V									
OP	7	*	7	7	10	16	118	16	118
ImpOP	(G40)324	G40)306	14	14	14	9	9	8	8
TRAN	11300	12187	12488	12334	25818	9705	13586	10105	13258
AnalTime	12.47	21.60	20.72	26.20	55.51	84.40	115.55	52.27	93.90
loadTime	4.04	14.65	14.98	19.29	43.75	77.40	105.43	45.07	84.48
SAT (ringS2)									
ECL Ring Osc									
Valim = 5.2V									
OP	8	*	7	7	10	7	114	7	114
ImpOP	(G40)328	*	14	14	14	8	8	7	8
TRAN	7761	*	9330	9342	16749	10549	11580	10450	12205
AnalTime	9.58	*	15.64	20.45	35.83	83.39	97.58	52.15	86.88
loadTime	2.67	*	10.71	14.18	27.41	75.88	89.07	44.74	77.38

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GUMSTD	GUM1	GUM2	GUM3	GUM4	HICUM2221	HICUM2221	HICUM2222	HICUM2222
Std Build-In	From VA	From VA	From VA	From VA	From VA	From VA	From VA	From VA
With LimInit	NO LimInit	With LimInit	With LimInit	With LimInit	With LimInit	With LimInit	With LimInit	With LimInit
NO SHT	NO SHT	NO SHT	SHT OFF	SHT ON	SHT OFF	SHT ON	SHT OFF	SHT ON

Units : OP : (iter) ImpOP: (iter) TRAN: (iter) AnalTime : (sec) loadTime: (sec)

HARD SAT (ringHS1)
ECL Ring Osc
Valim = 2.7 V

OP	15	*	28	28	34	89	121	57	121
ImpOP	(G40)323	(G40)265	12	12	12	9	9	8	8
TRAN	10598	14477	16872	16243	29152	14924	16713	14775	16355
AnalTime	11.52	27.93	25.09	36.07	58.68	118.4	149.60	74.77	113.32
loadTime)	3.50	16.37	18.26	24.01	45.90	107.34	137.74	64.56	101.78

HARD SAT (ringHS2)
ECL Ring Osc
Valim = 5.2V

OP	7	*	8	8	12	9	115	8	115
ImpOP	(G40)328	(G40)308	11	11	11	8	8	7	8
TRAN	10662	15731	14651	14614	26123	11476	14454	11895	14900
AnalTime	12.08	26.93	22.38	38.52	53.84	94.31	126.69	61.98	103.43
loadTime	3.53	17.64	16.25	22.52	41.93	86.13	116.11	53.91	92.88

note :

(iter) : means Number of Iterations
(sec) : means Number of Seconds
(G40) : means Gmin stepping completed , nb of step=40 .
*** : means no results**
Std Build-In : means Standard Built In SPICE Model
From VA : means Model compiled from a Verilog A Source File
With LimInit : means Model with Init and Limit function into the compiled model
NO LimInit : means Model with NO Init and Limit function into the compiled model
NO SHT : means Model with NO SELF HEATING Feature
SHT OFF : means Model with SELF HEATING Feature OFF
SHT ON : means Model with SELF HEATING Feature ON

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note :

Gummel-Poon reference Verilog A code :

Verilog-A/AMS definition of BJT (GP model) 2003
Based on Berkeley Spice3f5 implementation
This implementation does not account
for excess-phase, and includes substrate
UPDATED March 8, 19 2004
Contributed By:
Geoffrey Coram, Ph.D Senior CAD Engineer Analog Devices, Inc.
UPDATED 9 oct 2006 J.C.PERRAUD : add INIT + LIMIT functions

we can express the Total Simulation time (AnalTime) with the following equation :

Total of Simulation time = Total of load Model Time + Total of Matrix Solving Time ;
or
Total of Simulation time = Nb of Iterations * (load Model Time(for 1 Iteration) + Matrix Solving Time(for 1 Iteration))

So obviously to decrease the Total of Simulation time :
=> we should decrease the load Model Time(for 1 Iteration)
=> we should decrease the Matrix Solving Time (for 1 Iteration)

the load Model Time(for 1 Iteration) depends of the Models Equations :
=> Number of lines in Evaluate Model Function
=> complexity of each lines of Evaluate Model Function

the Matrix Solving Time is said to vary as Matrix Size at a power of 3 : NbNodes ** 3

(automatic loading of a Hicum model into SPICE needs around 6 seconds ,
1 second to generate the C files and 5 seconds to compile and generate
the xxx.so library and to load && link the xxx.so library to SPICE)

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comments :

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and so , now , I can have exactly the same kind of behaviour and convergency

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as it is available when using existing Standard build-in SPICE Model

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I can now directly test and demonstrate the Verilog A Model with their Strategy

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of initialisation and limitations (as it is defined in theVerilog A code) ...

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1rst SIMULATIONS RESULTS :

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a- I have done some Slight modification in the VERILOG A code of new HICUM 2.22 model (NPN/PNP + Init Limit Functions)

b- New 2.22 HICUM model gives close numerical results (DC && TRAN) from the previous VERILOG A codes

c- New 2.22 HICUM model gives slight better time simulations results (DC + TRAN) from the previous VERILOG A codes (when SHT ON)

d- New 2.22 HICUM model gives better time simulations results (~*0.6) (DC + TRAN) from the previous VERILOG A codes (when SHT OFF)

note :

with close number of iterations , so differences in loadTime comes probably because as it is in the new Verilog A Source , the derivatives from "tnode" are not calculated when Self Heating is OFF... because the C Line optimisation algorithms into my VERILOG A model SPICE compiler

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e- GUMMEL-POON versions :

e-1 GUMMEL-POON Standard Build-In Binary SPICE 3F5 version is the more fast:

e-2 GUMMEL-POON from Veriloga without Init && Limit Functions do not converge into complex circuits ... (identical results from the previous results ...)

e-3 GUMMEL-POON from Veriloga with Init && Limit Functions converge into complex circuits ...
It has the same behaviour as the GUMMEL-POON Standard Build-In Binary SPICE 3F5 version ...(&& same iteration number ...)
But a relatively High loadTime = ~ 4 * loadTime of the GUMMEL-POON Standard Build-In Binary SPICE 3F5 (probably because my C Line optimizer into my VERILOG A model SPICE compiler is not enough clever ... Today I do not How to do better ...)

note :
for GUMMEL-POON , without C Line optimizer , a VERILOG A model SPICE compiler should generate 7 derivatives lines for each VERILOG A model code line ...
So in theory , 16 = 8*2 C lines codes for each VERILOG A model code line ...
Obviously people who introduce this model by hand try to generate C lines code for derivative only when he knows that the derivatives are not NULL ... Resulting in simpler C code ...
And more , GUMMEL-POON is an Old model with a C code a lot improved ...

e-4 GUMMEL-POON from Veriloga with Init && Limit Functions && With SELF HEATING code , but when SHT OFF :
loadTime (With SELF HEATING code && SHT OFF) = ~ 1.3 * loadTime (NO SELF HEATING code)

e-5 GUMMEL-POON from Veriloga with Init && Limit Functions && With SELF HEATING code , but when SHT ON :
loadTime (With SELF HEATING code && SHT ON) = ~ 1.9 * loadTime (With SELF HEATING code && SHT OFF)

(in this case , the number of iterations change a lot , from "SHT=OFF" to "SHT=ON" ...)

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2nd SIMULATION RESULTS:

	HICUM2072 level 0 2007 From VA With LimInit SHT OFF	HICUM2072 level 0 2007 From VA With LimInit SHT ON	HICUM2222 level 2V2p22 From VA With LimInit SHT OFF	HICUM2222 level 2V2p22 From VA With LimInit SHT ON
NO SAT (ring1)				
ECL Ring Osc				
Valim = 2.7 V				
OP	6	8	6	8
ImpOP	10	10	10	10
TRAN	4576	5153	4595	5184
AnalTime	20.71	24.00	26.04	39.70
loadTime	18.08	22.03	22.48	34.54
NO SAT (ring2)				
ECL Ring Osc				
Valim = 5.2 V				
OP	6	10	6	10
ImpOP	10	10	9	9
TRAN	4674	5290	4701	5311
AnalTime	21.74	25.99	27.38	44.89
loadTime	19.077	22.97	22.71	39.36
SAT (ringS1)				
ECL Ring Osc				
Valim = 2.7 V				
OP	16	17	16	17
ImpOP	9	9	9	9
TRAN	9255	10359	8554	9938
AnalTime	40.31	49.23	52.16	83.50
loadTime	35.57	43.95	45.36	74.28
SAT (ringS2)				
ECL Ring Osc				
Valim = 5.2V				
OP	6	13	6	13
ImpOP	8	8	8	8
TRAN	9018	11142	9482	10542
AnalTime	40.85	54.14	55.91	85.45
loadTime	36.06	49.51	47.30	75.94

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	HICUM2072 level 0 2007 From VA With LimInit SHT OFF	HICUM2072 level 0 2007 From VA With LimInit SHT ON	HICUM2222 level 2V2p22 From VA With LimInit SHT OFF	HICUM2222 level 2V2p22 From VA With LimInit SHT ON
HARD SAT (ringHS1)				
ECL Ring Osc				
Valim = 2.7 V				
OP	**18**	**20**	**19**	**20**
ImpOP	**8**	**8**	**8**	**8**
TRAN	**15124**	**17371**	**15710**	**18338**
AnalTime	**65.64**	**80.07**	**94.53**	**149.54**
loadTime	**58.60**	**72.86**	**81.18**	**133.83**
HARD SAT (ringHS2)				
ECL Ring Osc				
Valim = 5.2V				
OP	**7**	**15**	**7**	**15**
ImpOP	**8**	**8**	**7**	**15**
TRAN	**12395**	**14741**	**12694**	**15571**
AnalTime	**58.75**	**71.09**	**73.53**	**119.69**
loadTime	**50.48**	**64.99**	**62.59**	**106.18**

2nd SIMULATION RESULTS :

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these results of the HICUM model level 0 (2007) and the HICUM model level 2V2p22 (2007) was done using 2 new set parameters of the same ST BJT device

(ie : we have very close OP/DC and AC results)

(many Thancks to them for their friendly help & collaboration)

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a- Both , HICUM model level 0 (2007) and HICUM model level 2.22 (2007) , gives, as implemented in my SPICE , very low Iterations number in OP(6 to 20) / DC

b- Both , HICUM model level 0 (2007) and HICUM model level 2.22 (2007) , gives, as implemented in my SPICE , very good behaviour, for all analysis, (OP , DC , AC , TRAN , and in other related analysis ...)

Iterations number && Simulation time increase only slightly with the circuits (because mainly of Saturate and Hard Saturate BJT ...)

c- HICUM model level 0 (2007) is faster than HICUM model level 2.22 (2007) :

S.H.T OFF :

not saturated BJT : + 30%
saturated BJT : + 45%

S.H.T ON :

not saturated BJT : + 70%
saturated BJT : + 86%

d- Obviously , Simulation time , for a circuit depends also of the parameters sets ...

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5- Remaining Works ... to be done ...

=> Noise Analysis ...

=> remaining features : "idt ()"
(not really needed for a True Verilog A Model Compiler ...)

=> Spice Verilog A Compiler for HP workstation under HPUX

6- Other Developments :

Transient Simulation of S PARAMETERS Macro-Models

(in t domain , Beta version available)
that includes the following steps :

6-1 generate S PARAMETERS equivalent from a Macro-Model Sub-Circuit
(New Analysis into SPICE 3F5 ...)

6-2 Automatic Rational approximations of S PARAMETERS
(complex vector over Frequency) by vector fitting :
using Multiple Poles relocation method and
Rational least squares approximation...
(by default : 20 real poles or 10 Complex poles ...)

see : rational_poles_vector_fitting_BjornGustavsen_1999.pdf

6-3 Recursive convolution simulation , in t domain :
the Macro-Model is now used from its equivalent poles fitted functions ...
(see : Laplace Transform function table of poles to the t domain ...)

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7- CONCLUSIONS :

7-1 Simulation Results && Comparisons for :

=> New Improved Advanced Verilog A Model compiler for SPICE 3F5

=> GUMMEL-POON (experimental versions) from Veriloga :

=> with Init & Limit Functions add-on

=> With/Without SELF HEATING add-on

=> New HICUM models from Veriloga with Init & Limit Functions

Have been presented and demonstrated ...
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(Results are freely available , on request , to validate your own simulators)

7-4 All Technologies developed into this SPICE can be transferred to other simulators ...

To negotiate Licences , please contact :

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