HICUM - Workshop 2007

New TRADICA Features

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Introduction

- highly competitive semiconductor industry
  - need to reduce time-to-market and increase yield

- cycle time reduction can be achieved by
  - device optimization during process development guided by circuit design feedback
  - circuit optimization based on accurate (physics-based) modeling, incl. device design freedom

=> concurrent engineering: simultaneous process development and circuit design

- link compact device modeling to circuit design and process optimization
  - use predictive modeling capability
  - add generic device sizing method based on lateral *and* vertical technology parameters
  - establish figures of merit (FoMs) related to device and circuit performance

=> optimizer

Optimization Methods

- available optimization algorithms:
  - Nelder-Mead simplex method (can converge at local extremum)
  - combined with simulated annealing (search for global extremum)

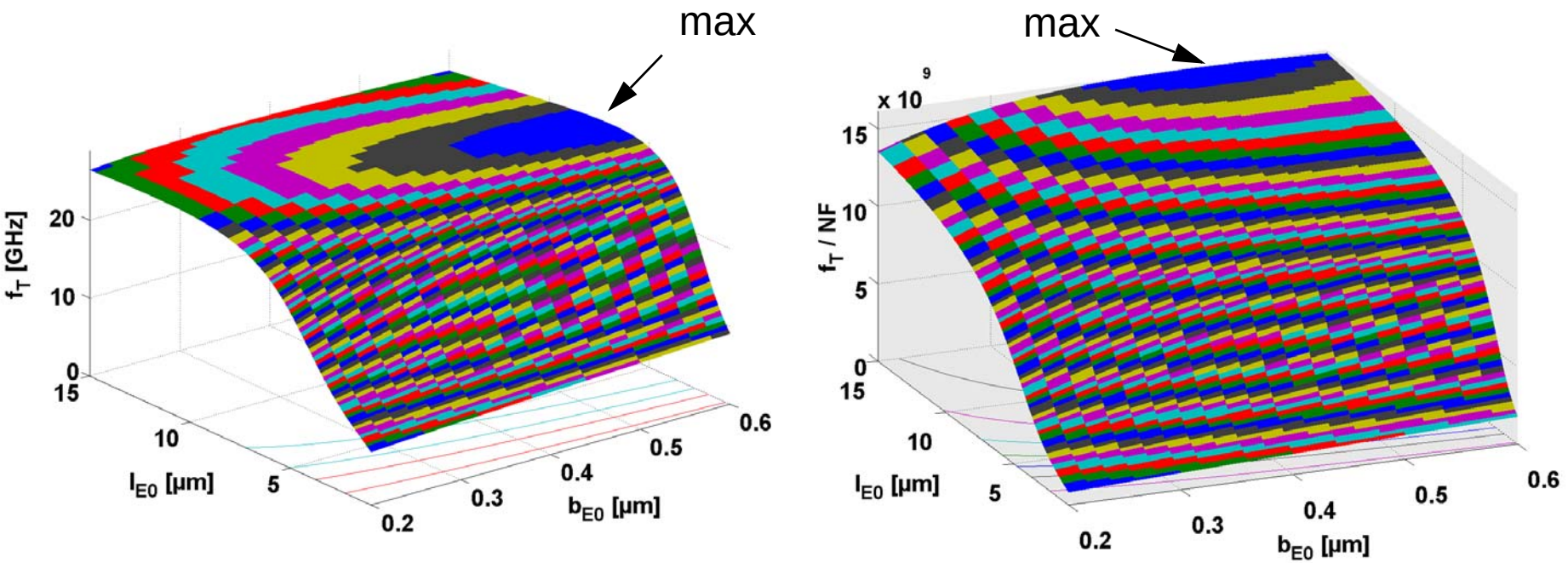
- FoMs are directly calculated by TRADICA to ensure low simulation time
  - newly integrated HICUM/L2 small signal solution used (with/without R_G)
  - additional device FoMs: f_T, f_{3dB}, Y parameters (calculated numerically), small signal equivalent circuit parameters for hand calculations
  - circuit FoMs: delay time for CML, ECL and EF gates, f_{3dB},gain, GBW of a cascode LNA

- FoMs are used as optimization targets (*single* or *joint* FoM or *target*)
  - *joint* FoM: properly arranged weighted product of single FoMs
  - *target*: search for specific FoM value

- 2 optimization types:
  - process optimization (max. 14-dimensional)
  - device optimization (max. 2-dimensional)

Device Optimization

- optimization of the emitter window dimensions for a certain FoM @ given bias



- maximum f_T: 28.94 GHz @ b_{E0}=0.60µm and l_{E0}=6.84µm
- taking the noise figure NF into consideration, the optimum is clearly shifted maximum f_T *and* minimum NF @ b_{E0}=0.48µm and l_{E0}=15.00µm
- no limitation in number of FoMs or dimensions for optimization

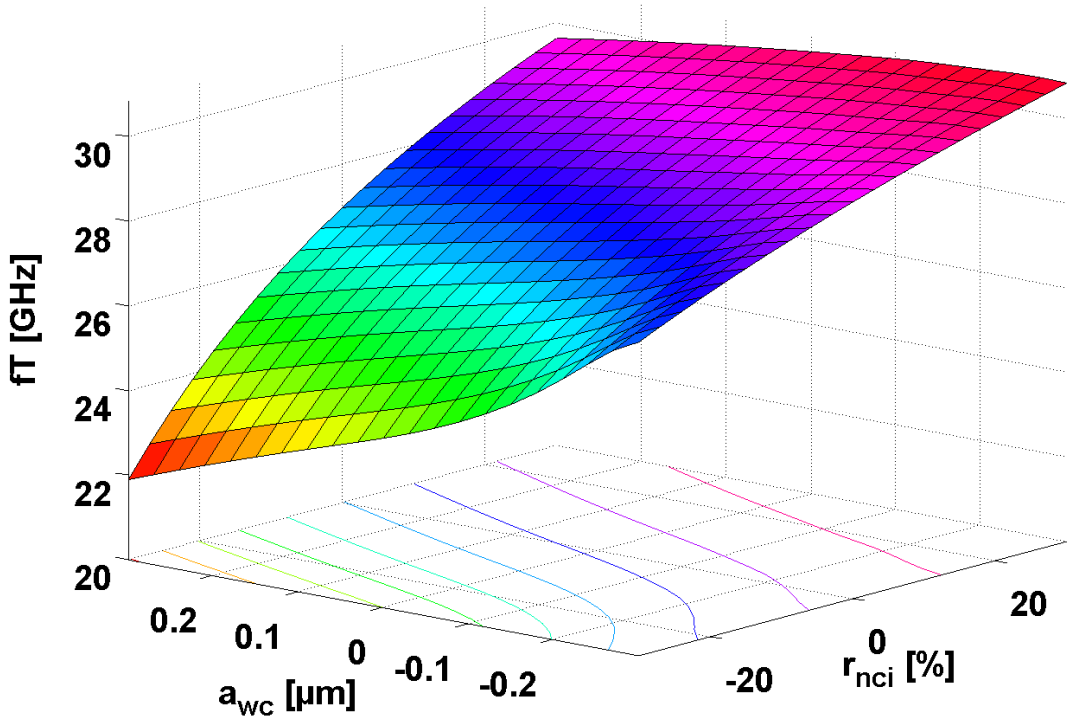
Process Optimization

- optimization of the process technology (represented by TPs) for a certain FoM @ given bias and transistor configuration

- significant speed improvement for N-dimensional optimization

Example

- consider a 4 dimensional optimization
- nci δ=0.14 => 29 points
- nbei δ=0.05 => 11 points
- wc δ=0.08 => 17 points
- wb δ=0.08 => 17 points
- resulting grid consists of 92191 points, calculation time 24h
- in TRADICA 4min



MOS in TRADICA

- work on MOS model integration in TRADICA started
- EKV 2.62 and 2.63 integrated
  - numerical derivatives used
  - transcapacitances and transconductances available
  - verified vs. Spectre and golden C-Code
- plans to enable all TRADICA features for MOS models
- for further information please see
  => poster session
  => demo session