

Design Technologie für präzise analoge IP-basierte Front-End Lösungen in höchstintegrierten Hochgeschwindigkeits-Datenübertragungssystemen

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Förderkennzeichen: 01M3071

Statistical Simulation

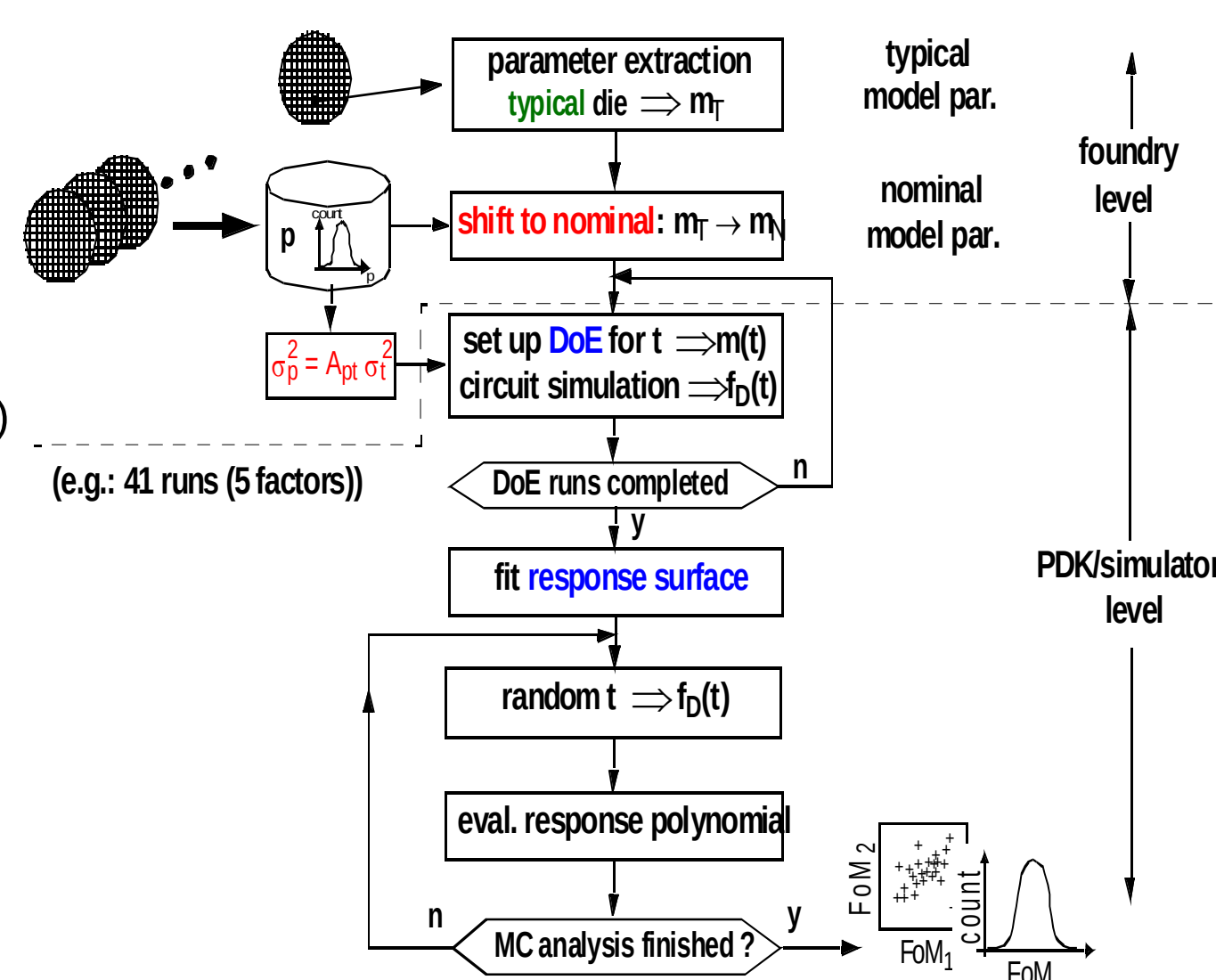
Use of a TRADICA based Statistical Design Kit in the Cadence Environment

The Tradica Principle

- Initially a TRANSistor Dimensioning and CALculation program used for an analog simulator
- Since mid nineties it has become an expert system, being expanded to handle all devices of a technology
 - for the statistical part FAB process parameters as well as technology parameters (e.g.: base width, base doping) are used as independent variables (technology scaling ability)
 - advanced scaling equations support a large variety of layout sizes
 - devices using the same process step are automatically coupled
 - matching information can be included
 - for bipolar the advanced HICUM and the classic SGPM are supported in various complexity levels

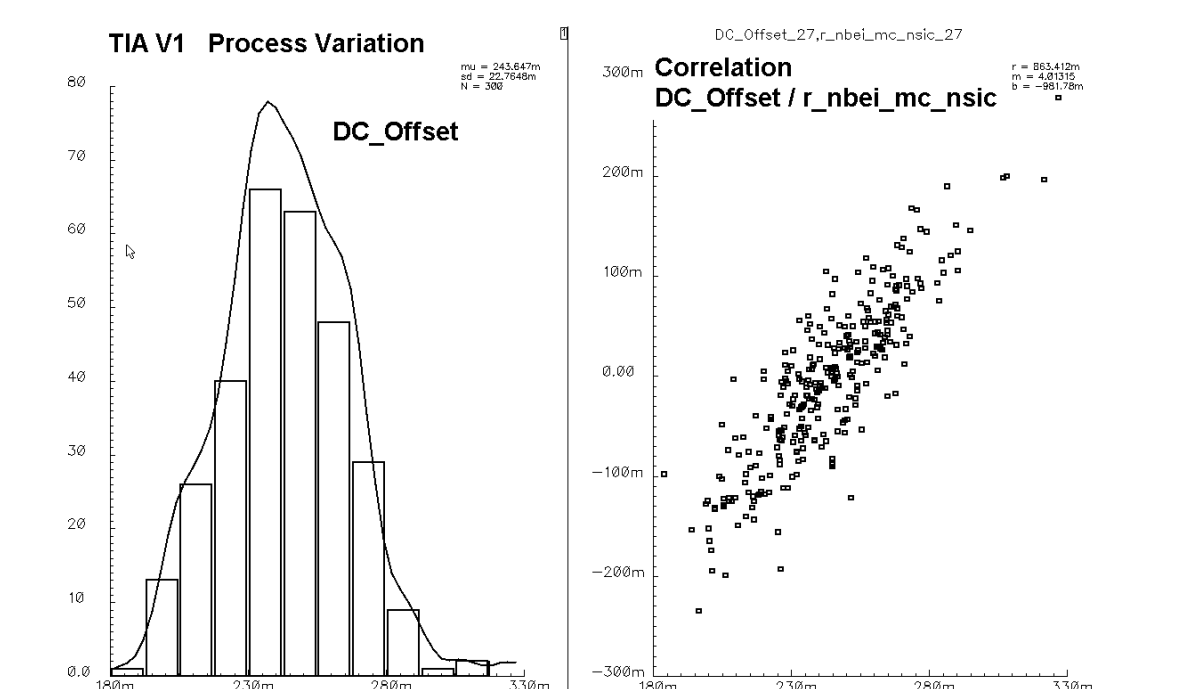
Statistical simulations

- So far corner simulations are widely used not only for CMOS but also for bipolar designs. But this is inadvisable due to the fact that a part of the design space is non-physical
- Several methods can be used to enable statistical simulations
 - using standard models (poor scaling)
 - taking the electrical parameters of the model as statistical variables (no statistical coupling, non-physical solutions)
 - extracting statistically independent parameters (time consuming)
- So there is only one solution:
 - implementation of the TRADICA principle into the design flow

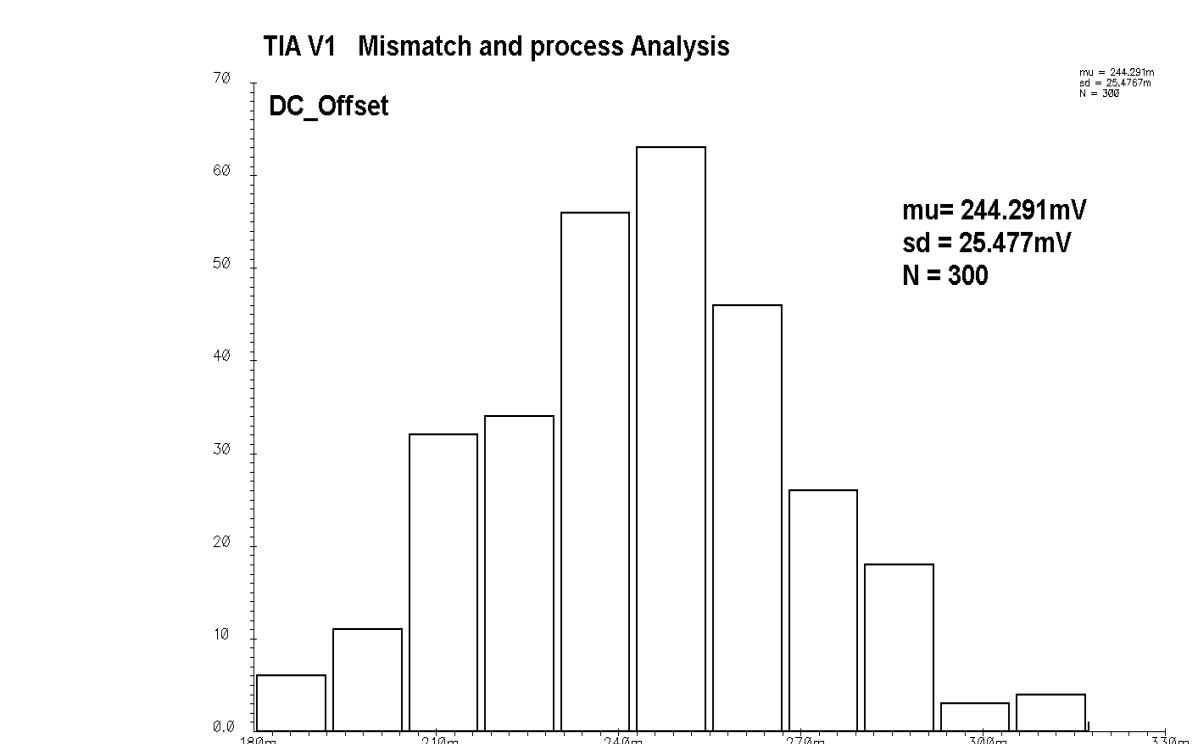


Identification of 1st order Effects

- 300 Monte Carlo runs were used to identify the process parameters which have the largest impact on the DC offset of the output signal
- In the example the doping of the inner base is most sensitive
 - Rerun the simulator and perform Monte Carlo only on the sensitive process parameter



- An additional simulation shows the effect of mismatch and process variation. It is now possible for the designer to identify the additional influence of mismatch to the design. This is also the data which is necessary to compare the simulation results with the manufactured IC's

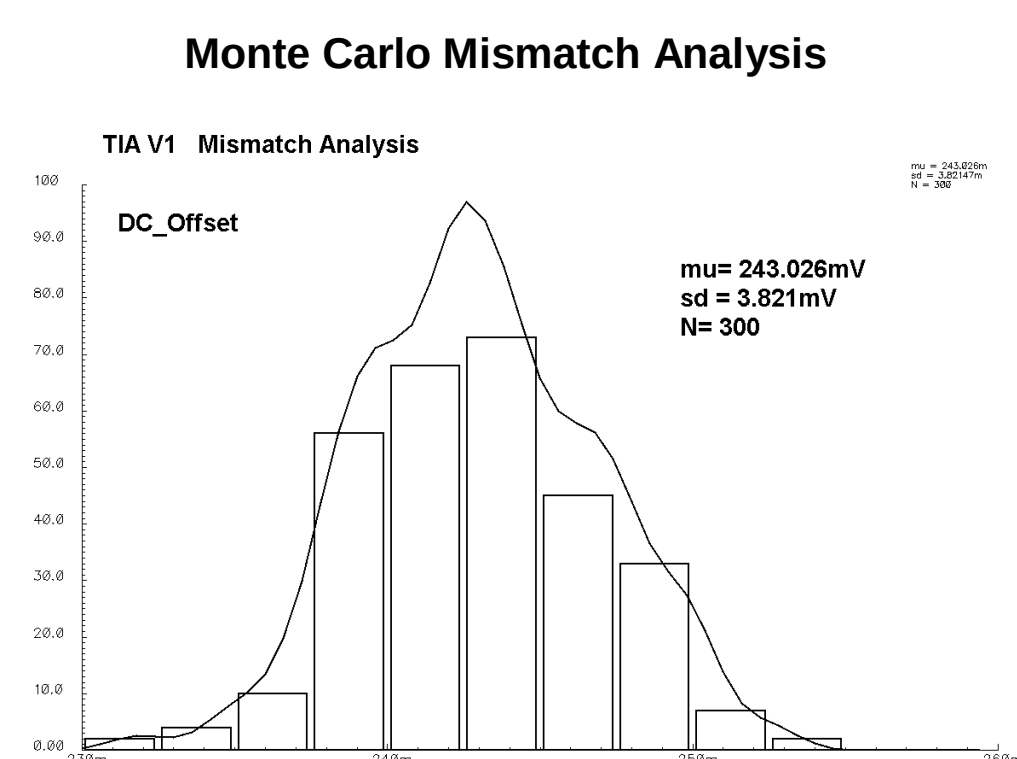
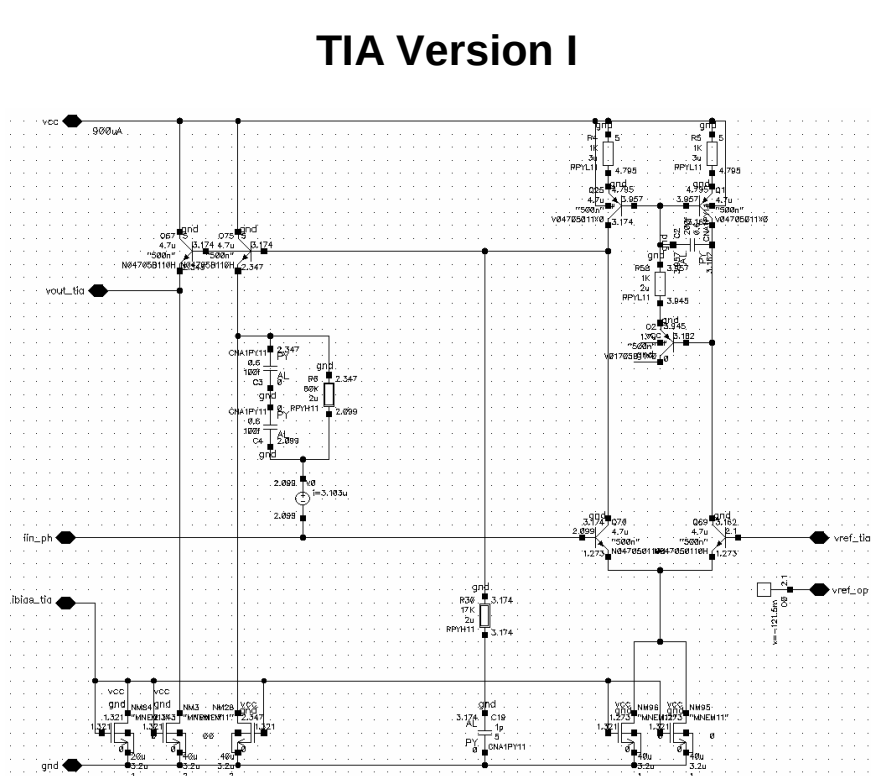


Closing the loop

- Formerly there was a gap between
 - the input for the statistic, i.e. the technology parameter variation
 - the output of a wafer FAB, i.e. the results of electrical measurements on PCM (process control monitor) structures
- To close this gap and to verify the statistical approach it is necessary to
 - Implement the statistical simulation capabilities into a design kit
 - collect sufficient PCM data
 - perform statistical simulations of the PCM test structures with the same testbench as the measurement to estimate the technology parameter variation
 - verification of technology parameter variation by comparison of measured and simulated PCM data

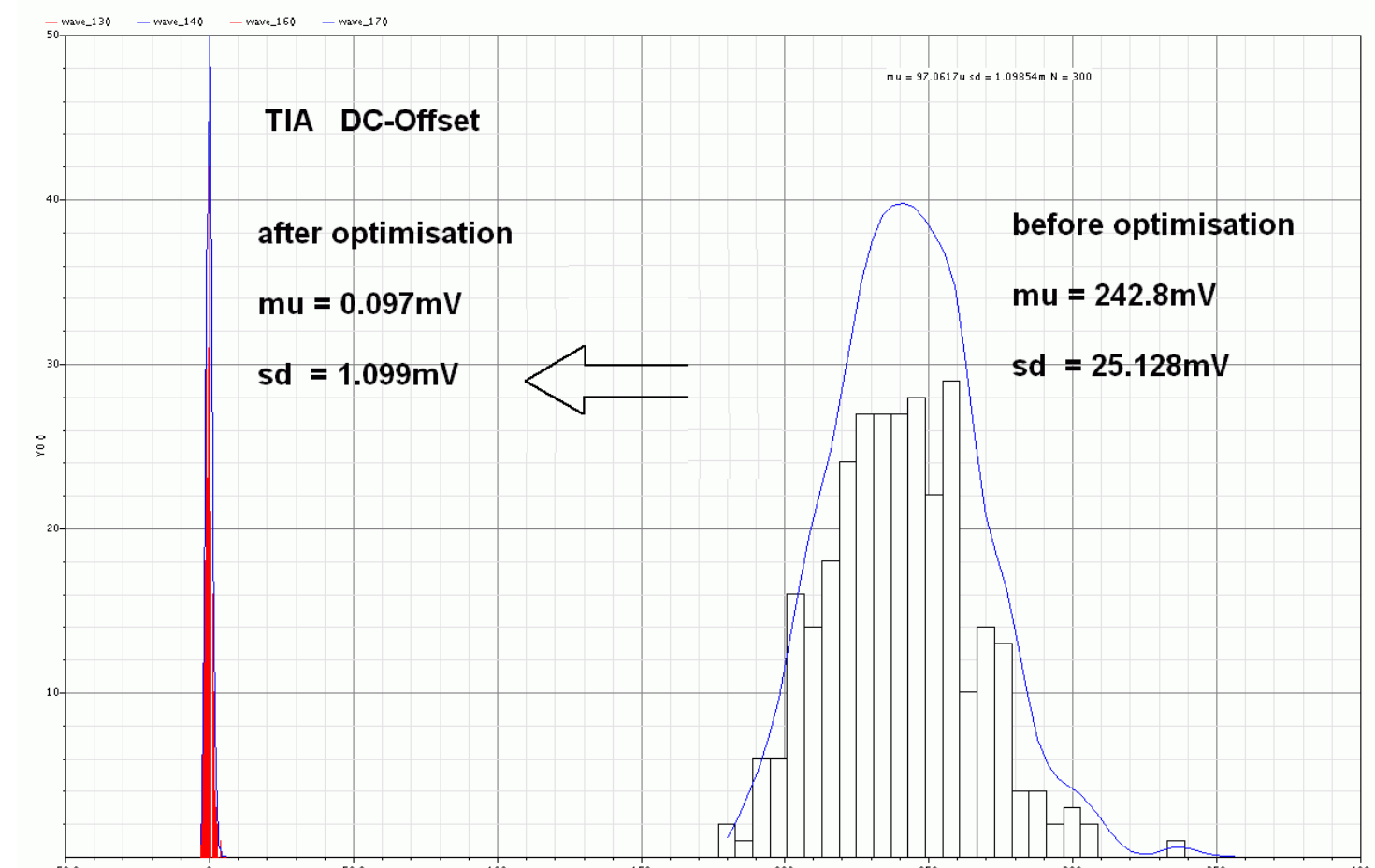
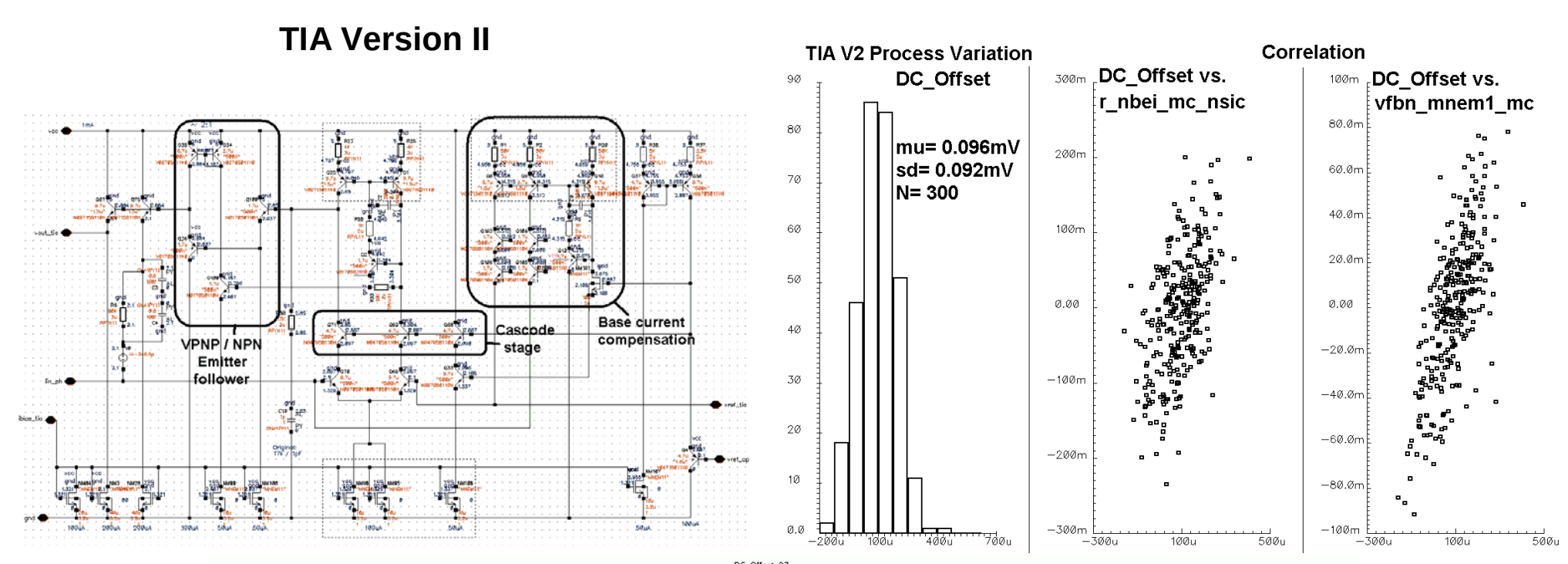
Using the Statistical Design Kit

Example: DC offset of a Transimpedance Amplifier (TIA)

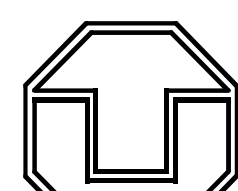


Results for the redesigned circuit

- Several additional blocks have to be added to reduce the offset and spread



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