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A Method for Bipolar Transistor Optimization in Process and Circuit Development

Abstract - This poster represents a summary of the *diploma thesis* of K.E. Moebus in 2006 at the Chair for Electron Devices and Integrated Circuits.

Today's semiconductor industry is characterized by fierce market competition, caused by quickly evolving technology and declining product life cycles. These circumstances force the semiconductor industry to reduce time-to-market and increase yield in order to lower the cost. Thus, it was the objective of this work to integrate an automatic optimization procedure into TRADICA (TRAnsistor DImensioning and CAlculation) to increase the competitiveness of semiconductor companies.

As one can see in Fig. 1, the optimization method integrated (only for bipolar transistors right now) consists of two succeeding optimization steps called Simulated Annealing and Nelder-Mead Simplex Method. Simulated annealing is started several times in a loop until convergence is reached. Simulated annealing itself is an extended version of the Nelder Mead simplex method combined with an random variation. Thus, the optimization algorithm can find a global extremum (with some minor deviations) in the presence of several local extrema. Afterward, a pure Nelder Mead optimization is performed. The Nelder Mead Simplex Method is used to fine tune the results of the first optimization pass which is necessary due to the random character of simulated annealing.

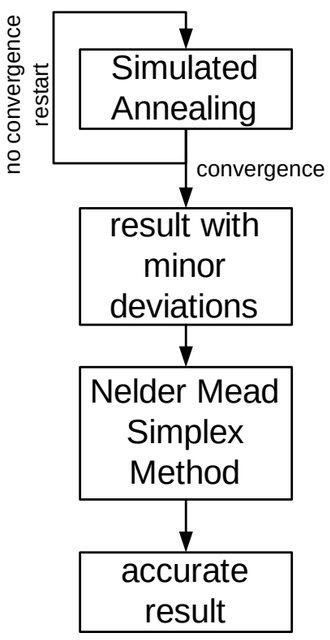

Fig. 1: Optimization procedure integrated in TRADICA.

The performance of a device or process is measured via figures of merit (FoM) such as transit frequency (f_T) and noise figure (NF). The optimizer is used to find the extremum of an FoM within a specified search range. Hence, there are two options to increase productivity by utilizing the optimizer in TRADICA.

The first one is called device sizing, meaning the emitter window dimension at the extremum of an FoM is calculated while the process technology is kept constant. Fig. 2 shows that TRADICA finds the transistor configuration to ensure maximum f_T. The calculation takes only a few seconds. Thus, the designer saves a significant amount of time considering the complexity and number of transistors ICs consist of.

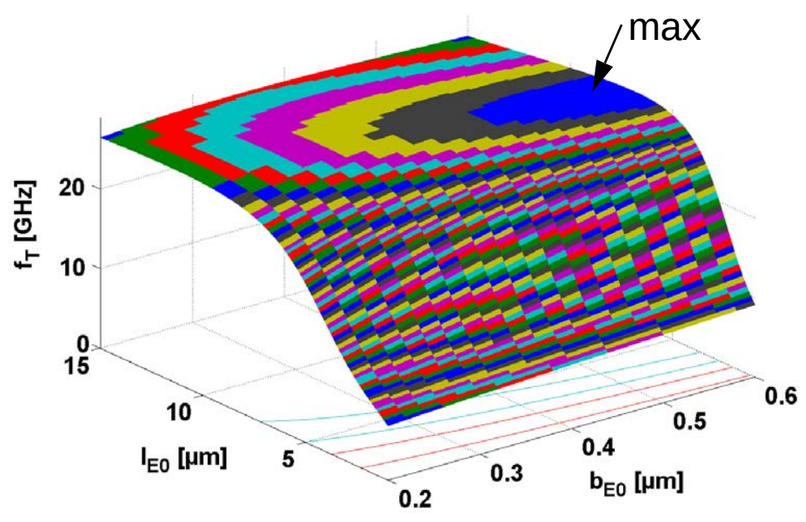

Fig. 2: Reference surface of f_T vs. emitter window dimensions and TRADICA calculated maximum (indicated by an arrow).

The second one is called process optimization. Here, the transistor configuration is held constant while the optimal device design is calculated w.r.t. a suitable FoM. Process optimization is necessary to meet the various and diverging requirements of, e.g. mobile applications. Hence, products will achieve optimal performance if fabricated with an optimized production technology (see Fig. 3).

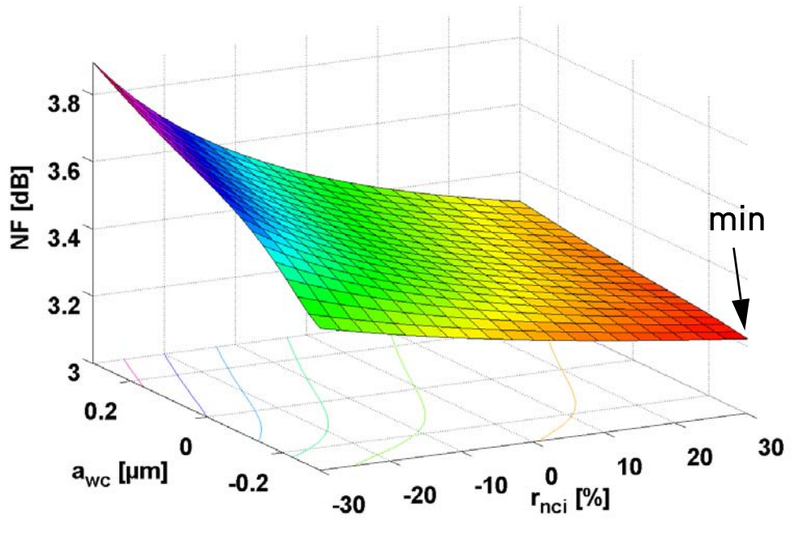

Fig. 3: Reference surface of NF vs. collector width and internal collector doping concentration variation (TRADICA calculated minimum is indicated by an arrow).

Based on the newly integrated optimization algorithm process and device development for bipolar transistors can be enhanced. It is possible to optimize the transistor configuration w.r.t. circuit FoMs. Multidimensional optimizations can be performed quickly (minutes compared to hours for traditional optimizations) with significantly lower cost.

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