

Modeling of non-isothermal effects in DEVICE

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Introduction

With the continuous decrease of semiconductor device dimensions non-isothermal device simulations become an more important issue. The minimization of devices leads to an increase of the dissipated power per volume ratio, which causes a local rise of heat. The emerging temperature distribution influences the electrical behavior (electro-thermal effects). So, non-isothermal simulations are of major interests for circuit designers, because of the determination of thermally stable operating points. Non-isothermal simulations also allow an adjustment of compact-model parameters with respect to electro-thermal effects. Non-isothermal device simulations also assist in technology development. The results of these simulations can be used to predict hot spots within a device. This poster gives a short overview of non-isothermal simulations with DEVICE.

Implementation in DEVICE

Based on the standard drift-diffusion model, consisting of the Poisson and the continuity equations, a formulation for the heat generation rate H within a device has to be defined. There are several formulations existing in the literature. In DEVICE the expression of *Chryssafis and Love* [3, 4, 6]

$$H = -J_n \cdot \operatorname{grad}(\varphi_n) - J_p \cdot \operatorname{grad}(\varphi_p) + qR(\varphi_p - \varphi_n) , (1)$$

has been implemented. For the evaluation of the temperature distribution within a device, the heat flow equation has to be solved. In the steady-state case, the heat flow equation is given by the following expression:

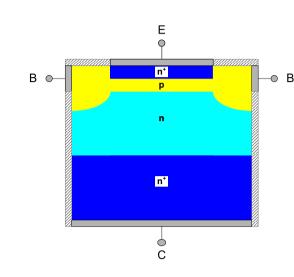
$$\operatorname{div}\operatorname{grad}(T_L) = -\frac{H}{\kappa} , \qquad (2)$$

where κ is the spatially constant thermal conductivity and T_L is the lattice temperature. In DEVICE, equation (2) is solved via the *Green's* function approach [5]. The drift-diffusion model and the non-isothermal model (equ. (1) and (2)) are successively solved in an iterative solution block. In order to improve the convergence, it is recommended to solve the drift-diffusion model simultaneously. Notice, after every iteration cycle all temperature dependent physical and electrical parameters, e.g. band-gap voltage, intrinsic carrier density or carrier mobilities, have to be adjusted to the previous calculated lattice temperature. A more detailed description about the extension of electrical and physical quantities due to spatially dependent temperature distributions can be found in [1].

Simulation results

Three common device structures are chosen to show the necessity of non-isothermal simulations. Fig. 1 shows a typical

bipolar transistor structure. The used doping profile is illustrated in Fig. 2.



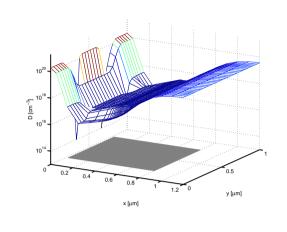
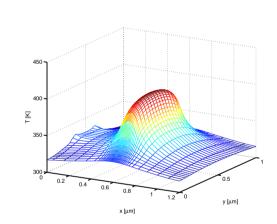


Figure 1: Schematic structure of the simulated bipolar transistor

Figure 2: Doping profile of the simulated bipolar transistor

To reduce the CPU time, equation (1) is restricted to regions where significant power dissipation is expected (gray marked area in Fig. 2 underneath the doping profile). Fig. 3 shows the shape of a calculated temperature distribution for $V_{BE} = 1.1 \text{ V}$ and $V_{CE} = 3.0 \text{ V}$. The resulting I_C vs. V_{CE} characteristic is shown in Fig. 4. The solid line represents the output characteristic of a non-isothermal simulation and the dashed line the one of an isothermal simulation, respectively.



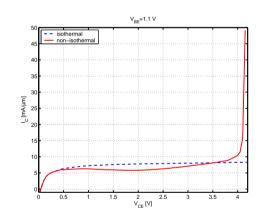
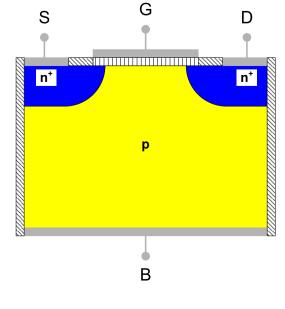


Figure 3: Temperature distribution $@V_{BE} = 1.1 \text{ V}$ and $V_{CE} = 3.0 \text{ V}$

Figure 4: I_C vs. V_{CE} (isothermal and non-isothermal simulation)

For low collector-emitter voltages, the simulation results of both models are the same, because the dissipated power is too small to cause a significant temperature rise. For sufficiently high collector-emitter voltages however, the bipolar transistor is thermally unstable due to the exponential rise of the collector current. Hence, thermal instability must be considered in circuit design. Note, that the peak of the temperature distribution is located in the internal collector region of the bipolar transistor [2]. Fig. 5 and 6 shows the structure of a bulk MOS transistor and the doping profile, respectively.



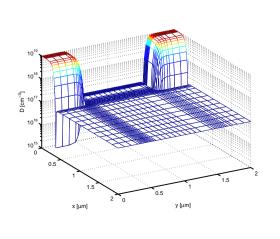
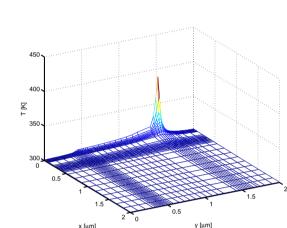


Figure 5: Schematic MOS-structure

Figure 6: Doping profile of the simulated MOS transistor

The output characteristic is illustrated in Fig. 8, where the solid line is the result of the non-isothermal simulation and the dashed line of the isothermal simulation, respectively. In contrast to the bipolar transistor, the MOS transistor behaves thermally stable. The temperature distribution is shown in Fig. 7 for an operating point in pinch off region. It is obvious, that the temperature peak is located at the channel - drain transition underneath the gate. This is a quite good example, where hot spots might occur within a device.



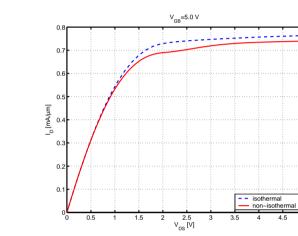
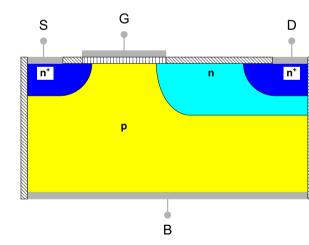


Figure 7: Temperature distribution $@V_{GB} = 5.0 \text{ V}$ and $V_{DS} = 3.0 \text{ V}$

Figure 8: I_D vs. V_{DS} (isothermal and non-isothermal simulation)

Due to this hot spot, HVMOS transistors are used for high power applications. These devices combine the advantages of a thermally stable behavior and the absence of hot spots. Fig. 9 shows the structure of a HVMOS and Fig. 10 the doping profile, respectively.



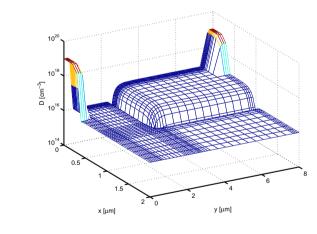
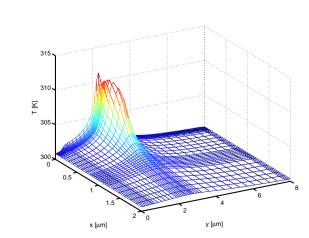


Figure 9: Schematic HVMOS-structure

Figure 10: Doping profile of the simulated HVMOS transistor

Unlike the doping profile of MOS transistor (see Fig. 6), the HVMOS transistor has an additional n⁻ drift region between the channel-drain transition (see Fig. 10), to reduce the local high electric field [2]. Fig. 11 shows the temperature distribution of the HVMOS transistor in pinch off region. The results of a non-isothermal and of an isothermal simulation are compared in Fig. 12.



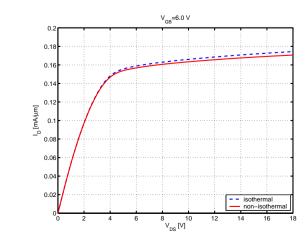


Figure 11: Temperature distribution $@V_{GB} = 6.0 \text{ V}$ and $V_{DS} = 18.0 \text{ V}$

Figure 12: I_D vs. V_{DS} (isothermal and non-isothermal simulation)

The differences between the output characteristics are marginal, since the local temperature rise is small compared with those of the bipolar or MOS transistor. Another benefit is the prevention of hot spots.

Conclusion

Non-isothermal device simulations are necessary in developing compact-models, devices itself and circuits. The thermal behavior of circuits essentially depends on the used devices and their thermal stability. To ensure the functionality of devices in early stage, they have to be simulated non-isothermally in order to rule out the possibility of hot spots or thermally unstable operating points. Note, that the illustrated results above may vary from those of other semiconductor device simulators, since there are used a variety of physical models and thermal boundary conditions. The conclusions drawn from other device simulators should typically resemble those of DEVICE.

References

- [1] G. Wedel, "Modellierung nichtisothermer Effekte mit DEVICE", Studienarbeit, Technische Universität Dresden, November 2006
- [2] G. Wedel, M. Claus and M. Schröter, "The influence of electro-thermal effects on semiconductor devices", Internal report (to be published), Technische Universität Dresden
- [3] G. K. Wachutka, "Rigorous Thermodynamic Treatment of Heat Generation and Conduction in Semiconductor Device Modeling", IEEE Transactions On Computer-Aided Design, Vol. 9, No. 11, November 1990
- [4] S. Selberherr, "Analysis and Simulation of Semiconductor Devices", Springer-Verlag Wien New York, 1984
- [5] Y. Zimmermann, "Modeling of spatially distributed and sizing effects in high-performance bipolar transistors", Master Thesis, Technische Universität Dresden, Juni 2004
- [6] P. B. M. Wolbert, "Modeling and Simulation of Semiconductor Devices in Trendy: "electrical, thermal and hydrodynamic behavior" ", Dissertation, ISBN 90-9004446-9, Universität Twente, 1991

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