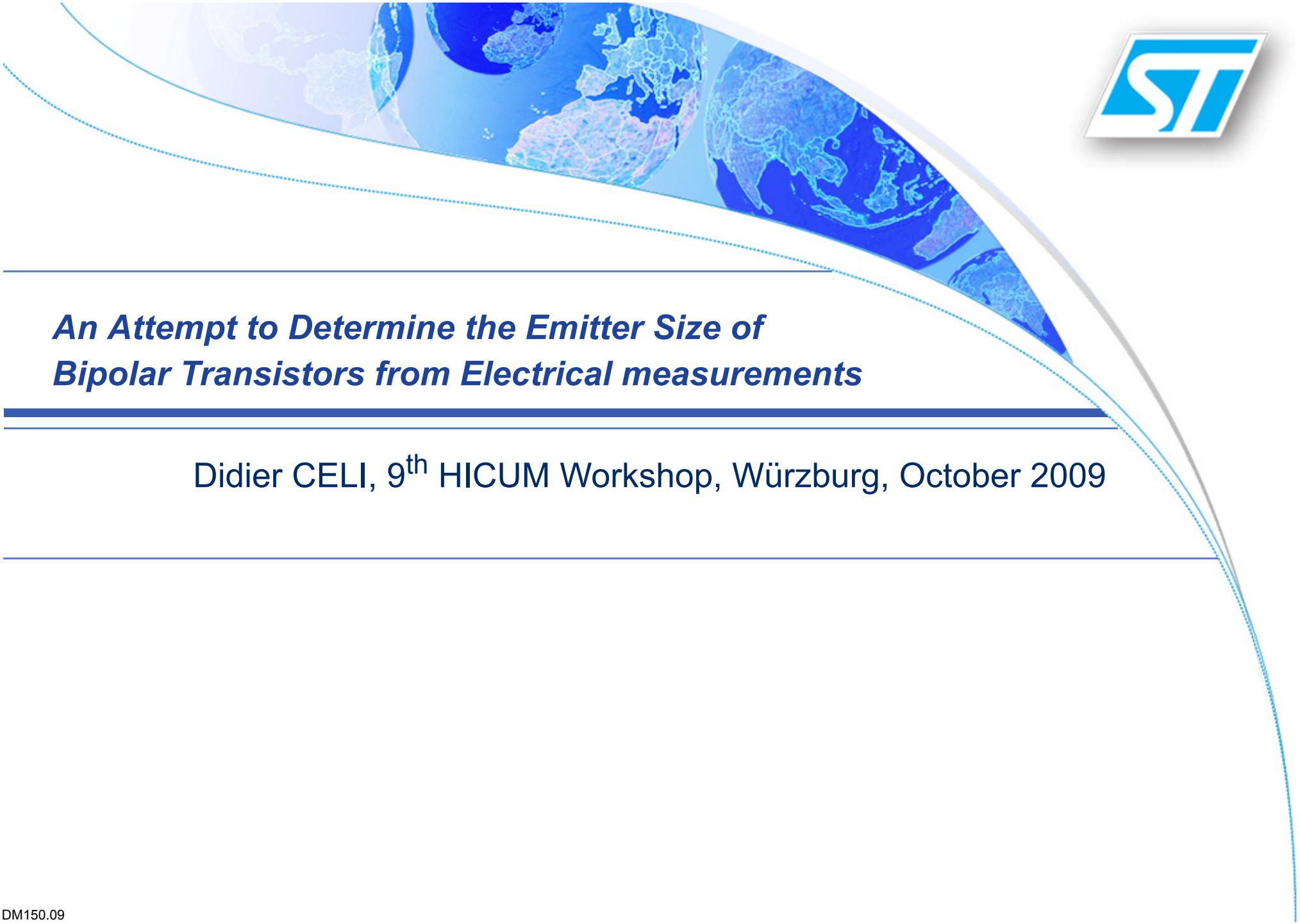


# *An Attempt to Determine the Emitter Size of Bipolar Transistors from Electrical measurements*

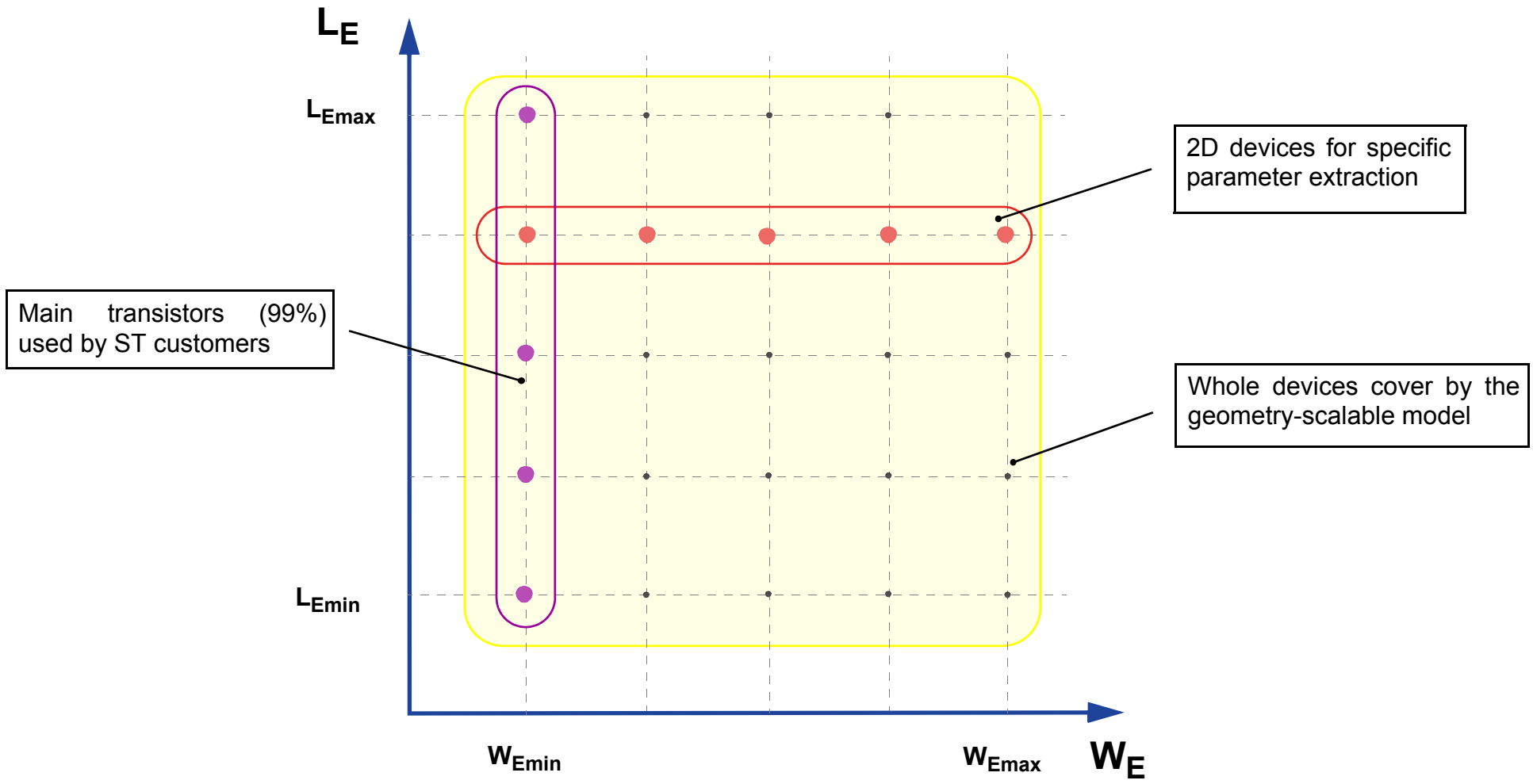
Didier CELI, 9th HICUM Workshop, Würzburg, October 2009

# Outline

- Purpose
- Specific parameter extraction and issues
- Specific parameter extraction from actual sizes of devices (SEM) and results
- Determination of emitter sizes from electrical measurements and specific parameter extraction
- Summary and conclusion

# Purpose

- To determine ***specific*** **model parameters** allowing to predict accurately the electrical behavior of bipolar devices with both variable emitter **length** and **width**



# Specific parameters extraction principle

## 2D devices: geometry-scaling laws

$$X = \mathbf{X_A} \cdot A + \mathbf{X_P} \cdot P \qquad (1)$$

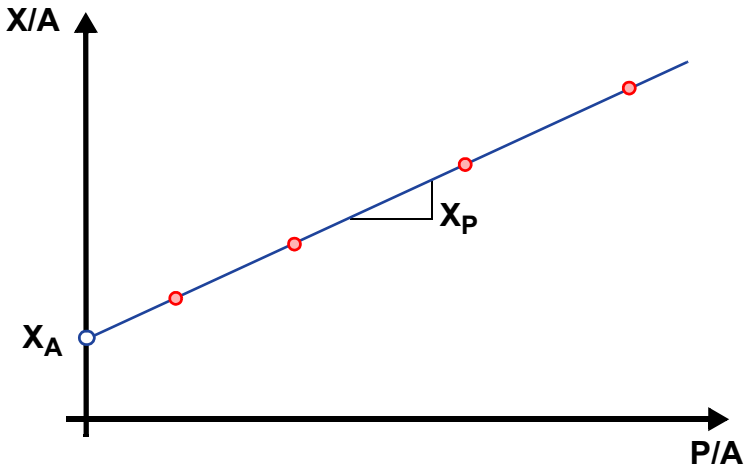
- X is variable which is geometry dependent such as current, charge, capacitance, transit time...
- A and P are respectively the window Area and Perimeter of the considered layer.
- $\mathbf{X_A}$, $\mathbf{X_P}$ are respectively the specific parameter per unit of area and per unit of perimeter.
- 2D device, emitter length greater than the emitter width (corner components can be neglected)

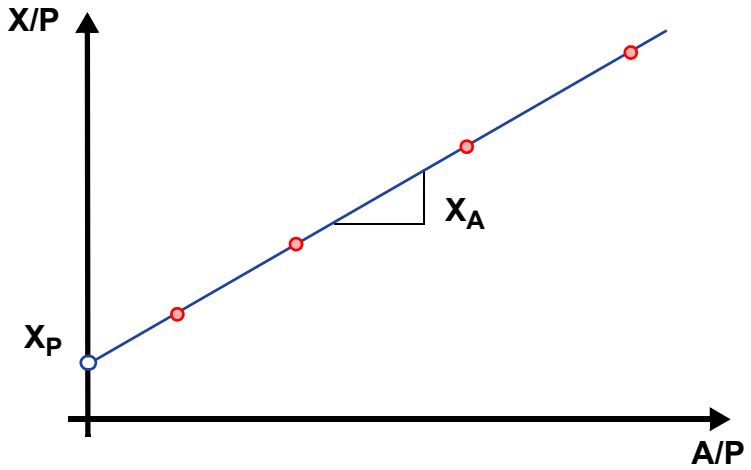
## Extraction methods

- Multivariable linear regression (least squares method)
  Knowing A, P and X, $\mathbf{X_A}$ and $\mathbf{X_P}$ can be directly determined
- Linear regression (linear least squares method)
  From (1) we can write

$$\frac{X}{A} = \mathbf{X_A} + \mathbf{X_P} \cdot \frac{P}{A} \quad \text{or} \quad \frac{X}{P} = \mathbf{X_A} \cdot \frac{A}{P} + \mathbf{X_P}$$

in both case $\mathbf{X_A}$ and $\mathbf{X_P}$ can be determined directly from the *slope* and the *intercept* of following characteristics




- The non-alignment of points allows to easily detect possible geometry-scaling issues.
- For geometry-scalable measurements all the 3 methods give similar results

# Measured devices and code naming

- Devices coming from B3T process ($f_T$=250GHz, $f_{max}$=300GHz) developped in the framework of DOTIFIVE European project [1]
- Drawn dimensions of the Emitter Window.

| | $W_E$ (µm) | | | |
|---|---|---|---|---|
| $L_E$ (µm) | 0.25 | 0.5 | 0.75 | 1 |
| 0.6 | NS122A06 | | | |
| 1 | NS122A10 | NS122B10 | NS122C10 | NS122D10 |
| 3 | NS122A30 | | | |
| 5 | NS122A50 | NS122B50 | NS122C50 | NS122D50 |
| 10 | NS122A100 | NS122B100 | NS122C100 | NS122D100 |
| 20 | NS122A200 | NS122B200 | NS122C200 | NS122D200 |

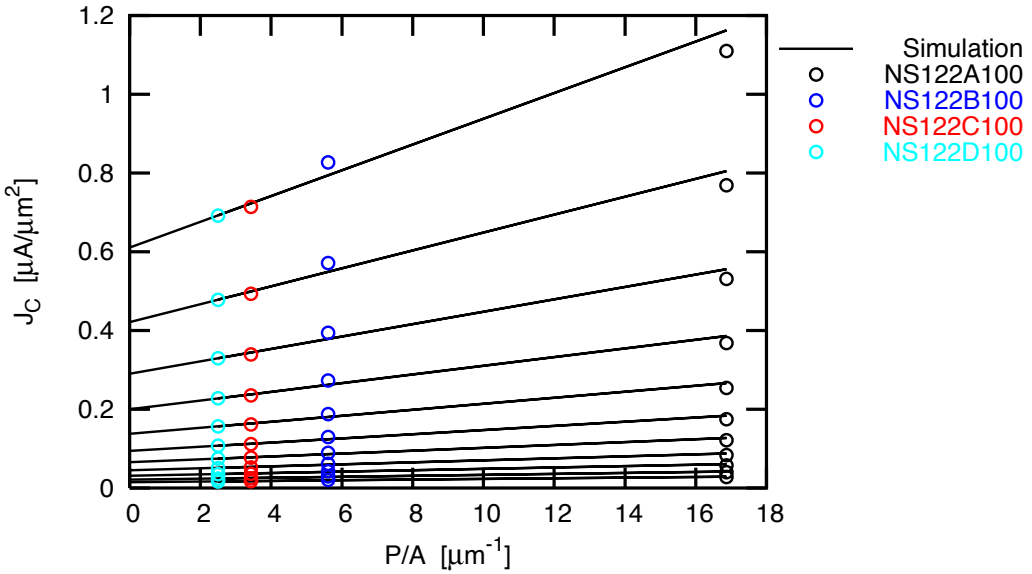
  - In first assumption: the actual emitter sizes are estimated by removing 0.13 µm to the drawn dimensions

- Code naming
  - NS for NPN high Speed, number of emitter, base and collector (122), emitter width (A=0.25, B=0.5, C=0.75, D=1µm), the last number is 10 times the emitter length.

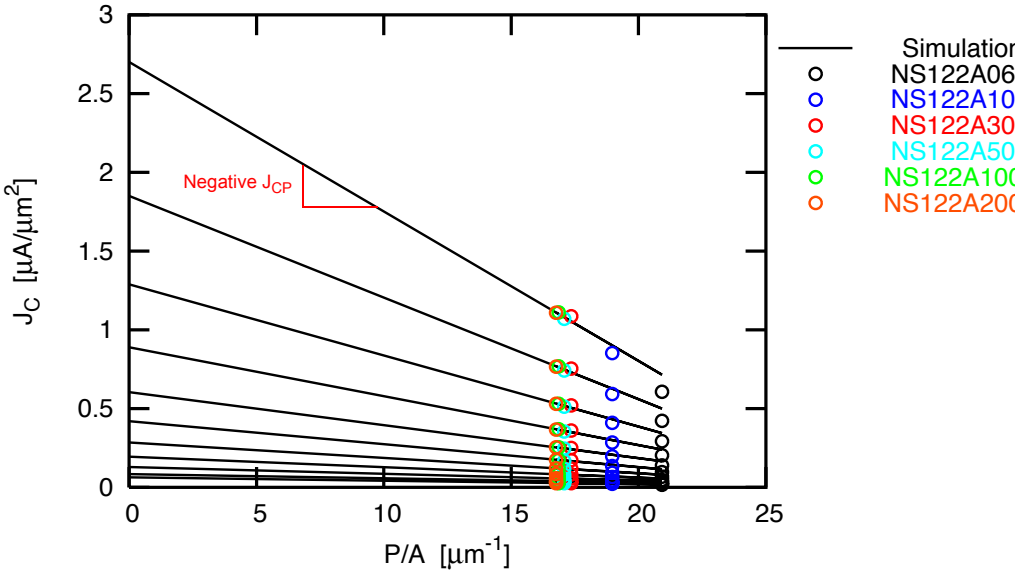
# Results

## Study of the collector current at low $V_{BE}$ and $V_{BC}$=0V

**Variable emitter width and constant length (10µm)**




**Variable emitter length and constant width (0.25µm)**

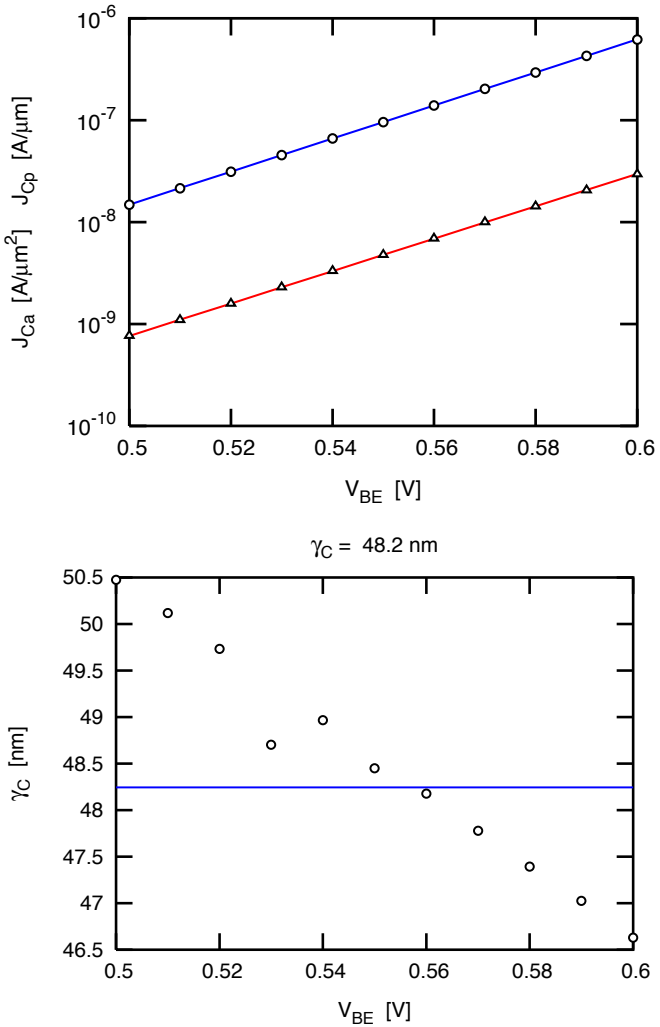


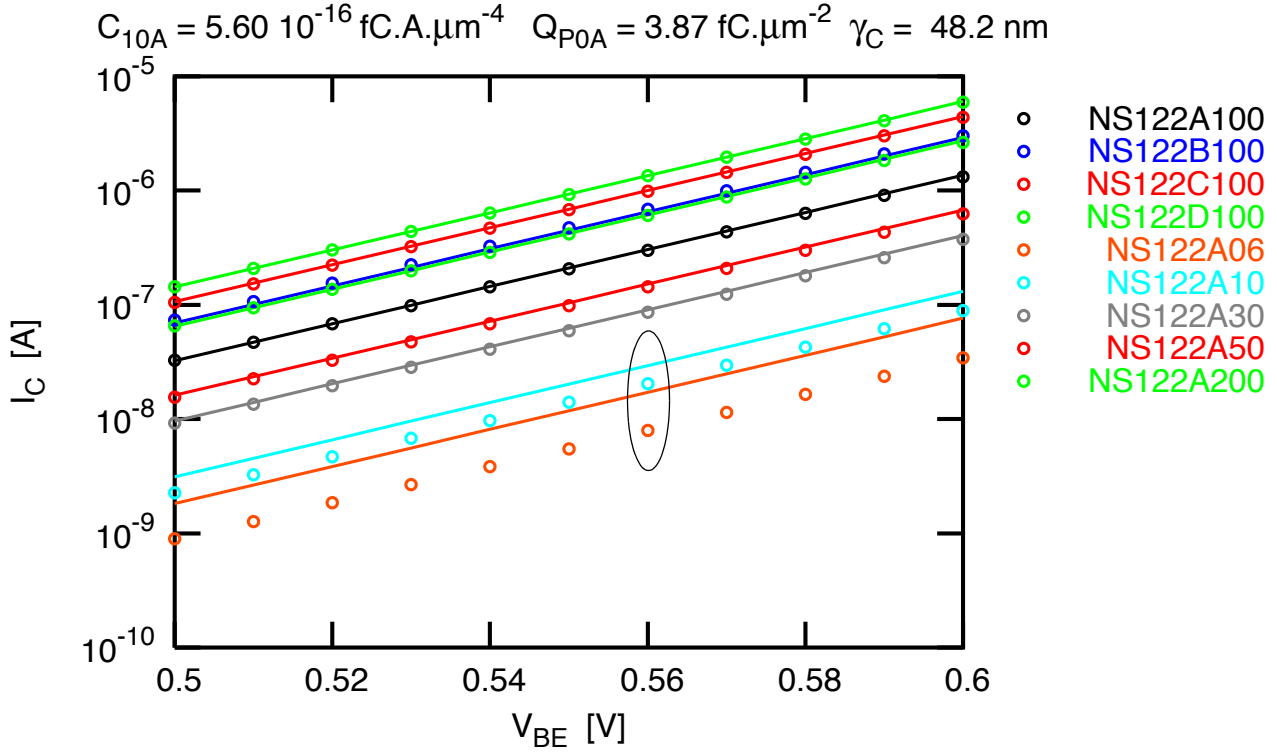

## Comments

- The results obtained from 2D transistors with variable emitter width (and constant emitter length) are not consistent with those obtained from transistors with variable emitter length (and constant emitter width)
- Specific parameters obtained from transistors with variable emitter width cannot reproduce the geometry dependence of transistors with variable length
- Why?

# Results

- Specific parameters obtained from transistors with variable emitter width cannot reproduce the geometry dependence of the transistors with variable length, especially for the smallest devices

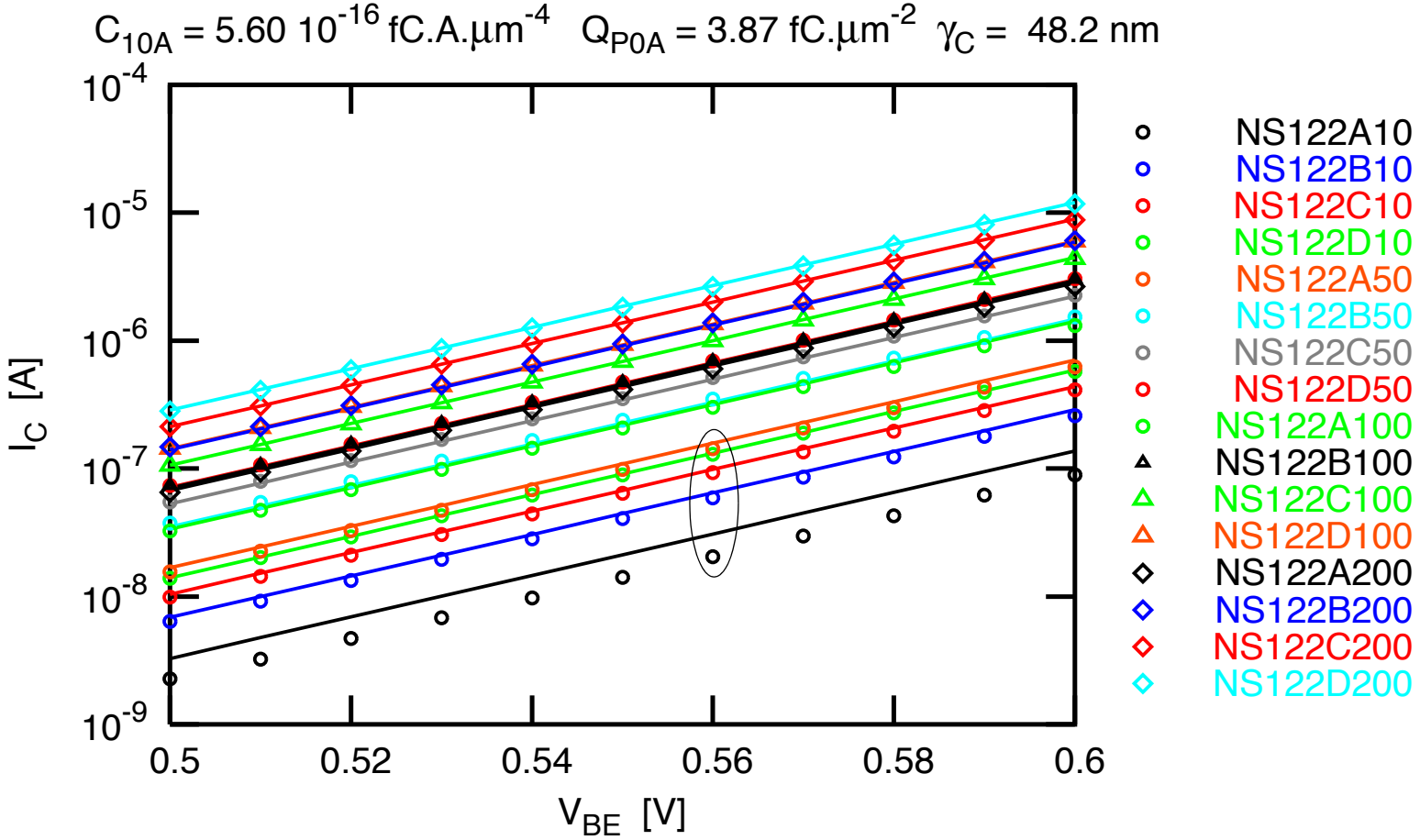



- $\gamma_c = \frac{J_{CP}}{J_{CA}}$
- See Appendix B for interpreting the variation of $\gamma_C$ with $V_{BE}$

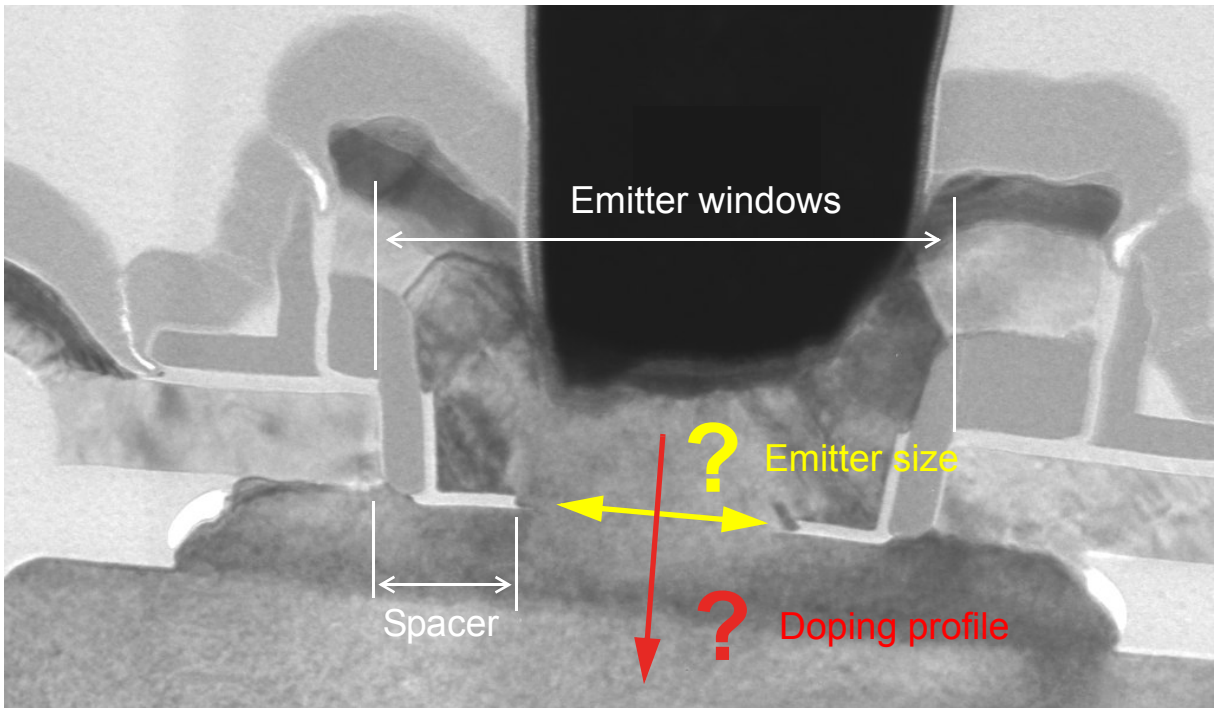
# Results

- On the other hand, the specific model parameters determined from transistors with variable width and L=10µm allows to accurately predict the collector current other variable emitter width and constant length (5, 10 µm).
- It is less true for small emitter length (1µm)



# Questions

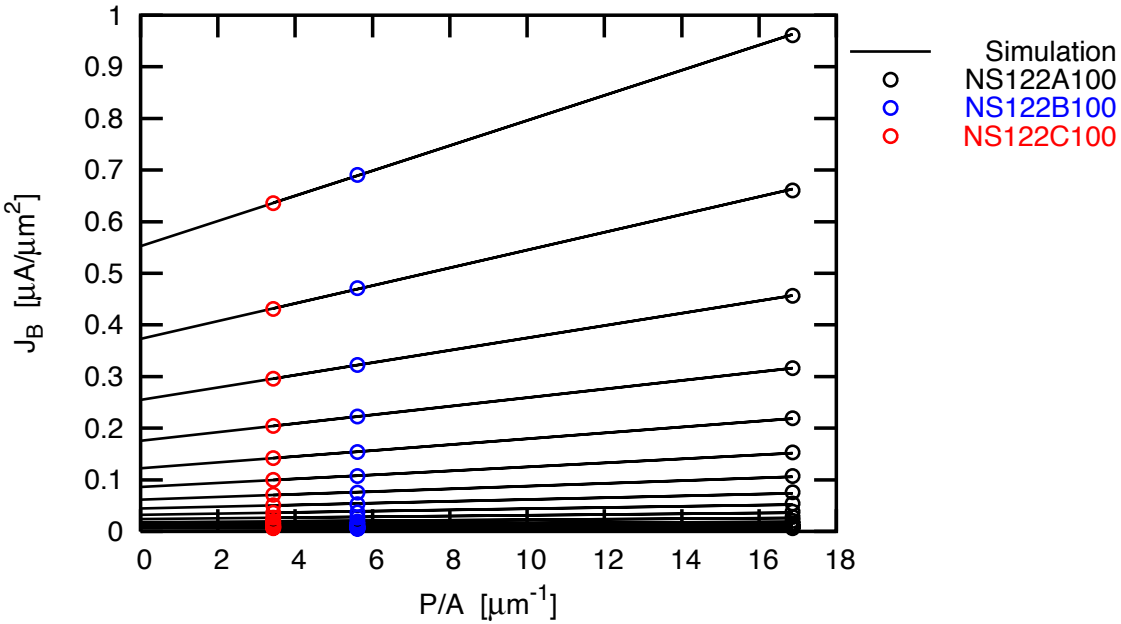
- Is it a problem of non-scalable doping profiles with the size of the emitter (selective SiGe base)?
- Is it a problem of knowledge of the exact actual emitter size on silicon?
- Other non geometry-scalable effects?

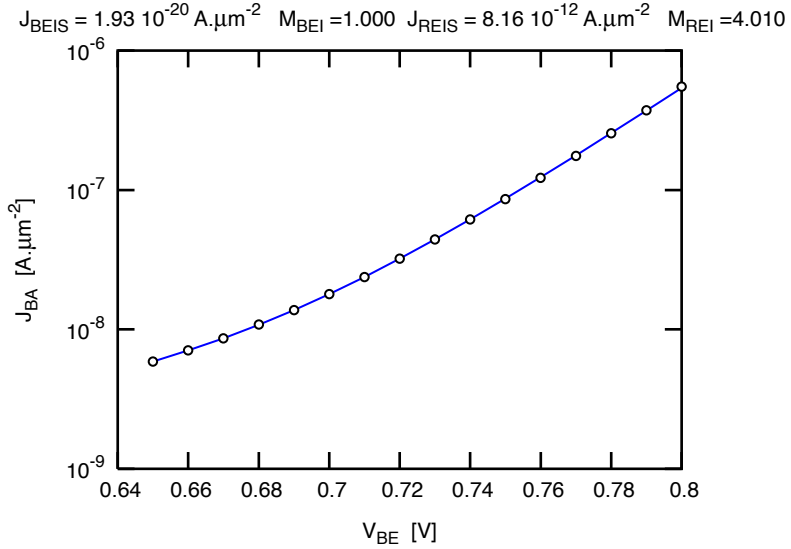


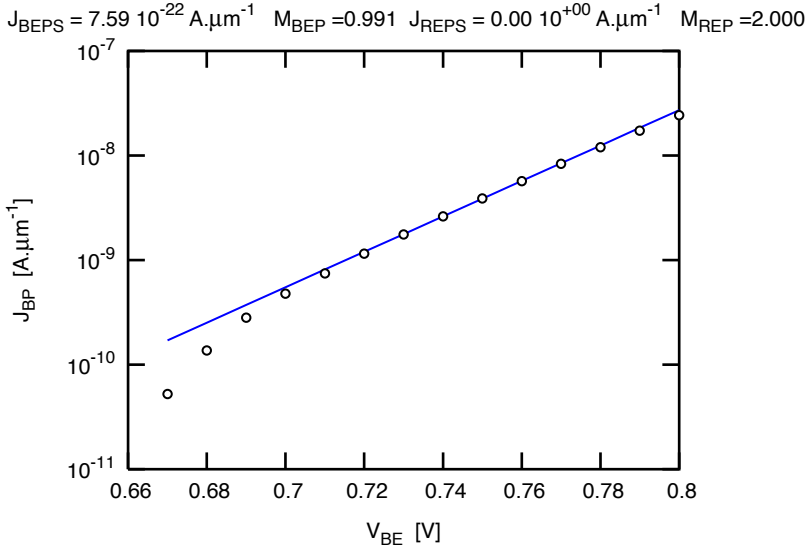

- In order to answer these questions, we looked at the base current which is more sensitive to a variation of the emitter size than to the SiGe profile of the base

# Study of the base current

## Specific parameter extraction [2]

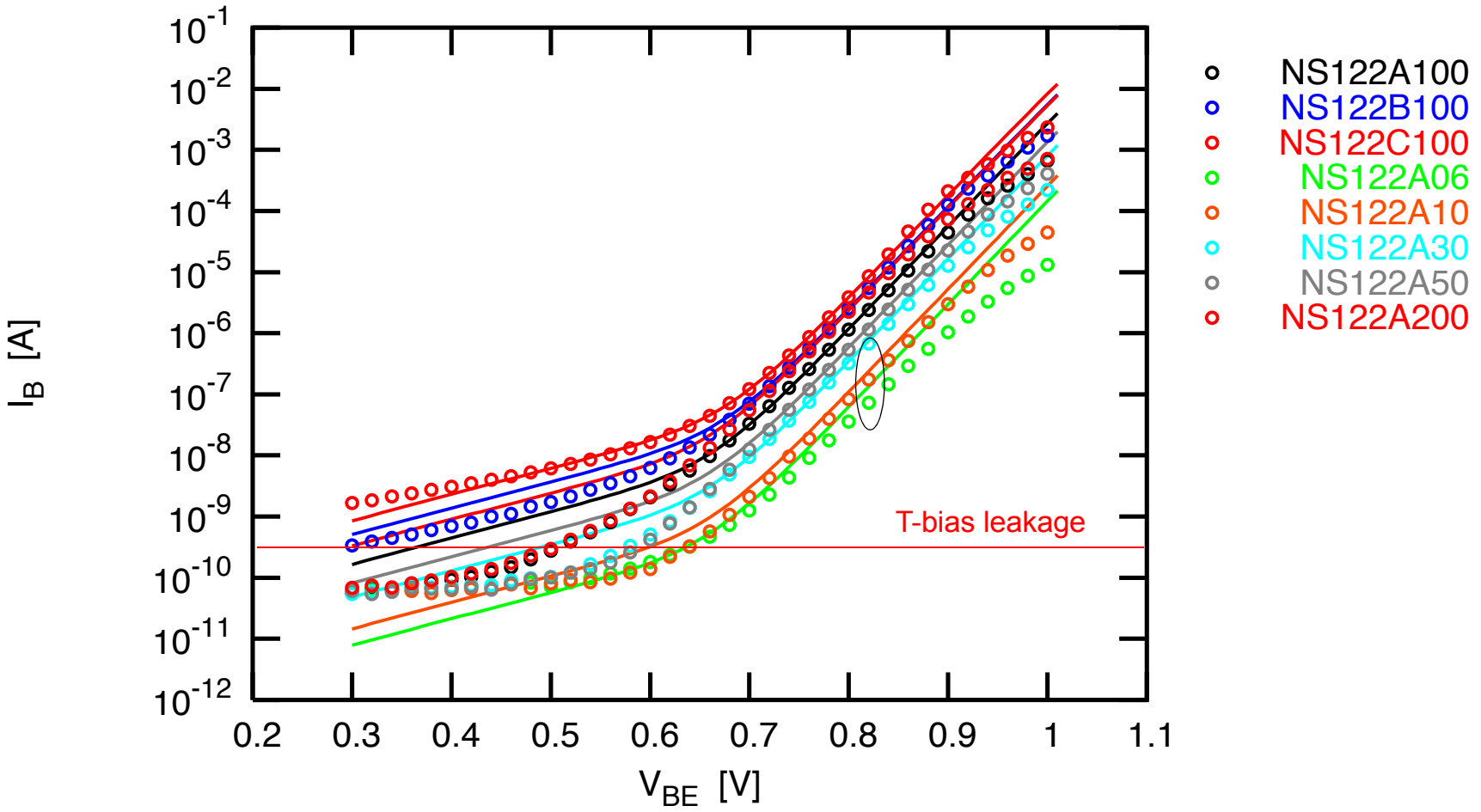


# Study of the base current

- Same issue than for the collector current. Specific parameters obtained from transistors with variable emitter width cannot reproduce the geometry dependence of the transistors with variable length, especially for the smallest devices.



# SEM analysis

- From these results, same issues on the collector and base currents for the smallest devices, we assume that the actual size of small devices are not known with enough accuracy.
- In order to verify this hypothesis, SEM (Scanning Electron Microscopy) pictures of the emitter window (after resist stripping) and of the emitter (after spacer formation) were performed
- Results [3] (2 dies) are summarized in the following table
  - $W_{EW}$ and $L_{EW}$ are respectively the width and the length of the emitter window
  - $W_E$ and $L_E$ are respectively the width and the length of emitter after spacer formation
  - $\delta_{WE}$ and $\delta_{LE}$ are respectively the total spacer width for the width and the length of the transistor

| | Drawn Dimension | | W05 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Center | | | | | | Border | | | | | |
| Transistor | $W_{EW}$ | $L_{EW}$ | $W_{EW}$ | $L_{EW}$ | $W_E$ | $L_E$ | $\delta W_E$ | $\delta L_E$ | $W_{EW}$ | $L_{EW}$ | $W_E$ | $L_E$ | $\delta W_E$ | $\delta L_E$ |
| NN122A6 | 0.25 | 0.6 | 0.204 | 0.434 | 0.082 | 0.269 | 0.122 | 0.165 | 0.219 | 0.414 | 0.063 | 0.235 | 0.156 | 0.179 |
| NN122A10 | 0.25 | 1 | 0.233 | 0.831 | 0.087 | 0.667 | 0.146 | 0.164 | 0.238 | 0.822 | 0.082 | 0.648 | 0.156 | 0.174 |
| NN122A50 | 0.25 | 5 | 0.246 | 4.799 | 0.092 | 4.663 | 0.154 | 0.136 | 0.245 | 4.811 | 0.082 | 4.635 | 0.163 | 0.176 |
| NN122A100 | 0.25 | 10 | 0.244 | 9.849 | 0.095 | 9.658 | 0.149 | 0.191 | 0.240 | 9.818 | 0.087 | 9.611 | 0.153 | 0.207 |
| NN122B50 | 0.5 | 5 | 0.494 | 4.969 | 0.358 | 4.814 | 0.136 | 0.153 | 0.494 | 4.950 | 0.356 | 4.844 | 0.138 | 0.106 |
| NN122C50 | 0.75 | 5 | 0.729 | 4.986 | 0.591 | 4.853 | 0.138 | 0.133 | 0.737 | 4.972 | 0.598 | 4.861 | 0.139 | 0.111 |
| NN122D50 | 1 | 5 | 0.971 | 4.986 | 0.835 | 4.839 | 0.136 | 0.147 | 0.988 | 4.963 | 0.844 | 4.841 | 0.144 | 0.122 |
| NN122D10 | 1 | 1 | 0.983 | 0.982 | 0.840 | 0.837 | 0.143 | 0.145 | 0.983 | 0.988 | 0.840 | 0.847 | 0.143 | 0.141 |

- The differences between estimated actual sizes (page 4) and actual sizes on silicon are not negligible, especially for small width and length

# Analysis of the sizes of the emitter window

- From the analysis of the depedence of the actual emitter length and width versus the drawn length and width of the emitter window [3] we can notice that
  - both the real emitter length vs. the drawn length of the emitter window and the real emitter width vs. the drawn width of the emitter window are linear
  - both the real emitter length vs. the drawn width of the emitter window and the real emitter width vs. the drawn length of the emitter window are non-linear

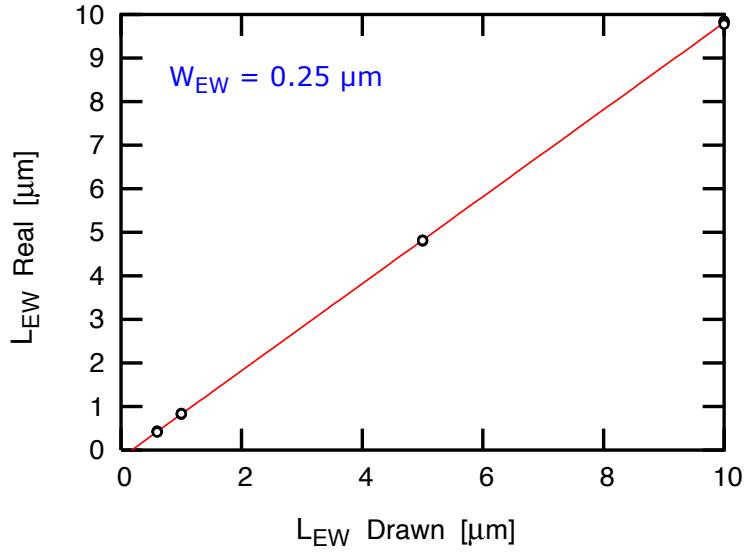
- From these observations, it is possible to determine the real emitter window length $L^*_{EW}$ and width $W^*_{EW}$ from the drawn dimensions ($L_{EW}$ and $W_{EW}$) using a second order model like

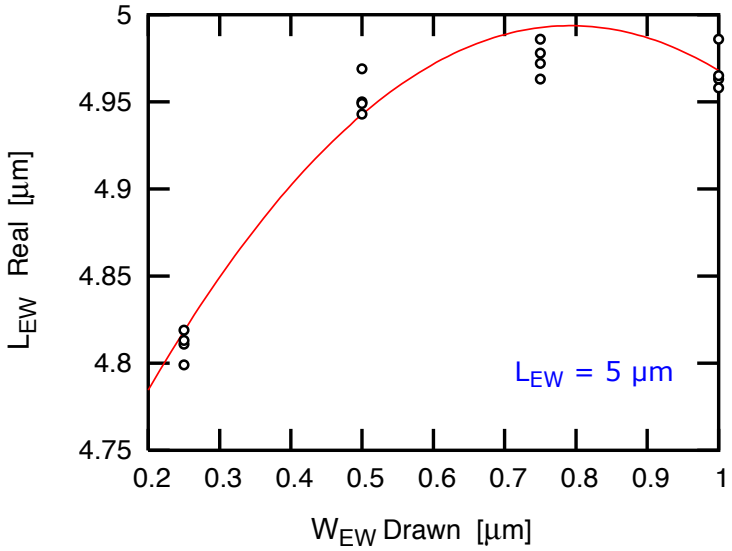
$$\begin{cases} L^*_{EW} = a \cdot W^2_{EW} + b \cdot W_{EW} \cdot L_{EW} + c \cdot W_{EW} + d \cdot L_{EW} + e \\ W^*_{EW} = a' \cdot L^2_{EW} + b' \cdot L_{EW} \cdot W_{EW} + c' \cdot L_{EW} + d' \cdot W_{EW} + e' \end{cases} \quad (2)$$

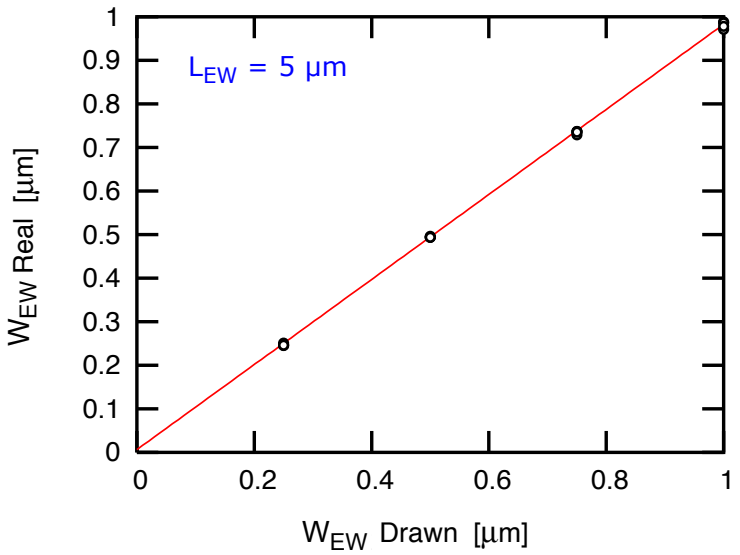
- Coefficients can be found in [3]

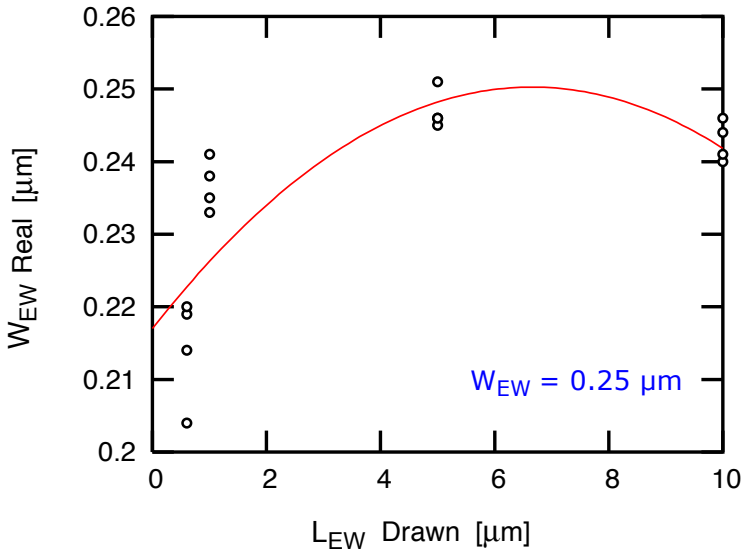
# Analysis of the sizes of the emitter window

- Comparison between measurements and equation (2)



# Analysis of the emitter sizes after spacer formation

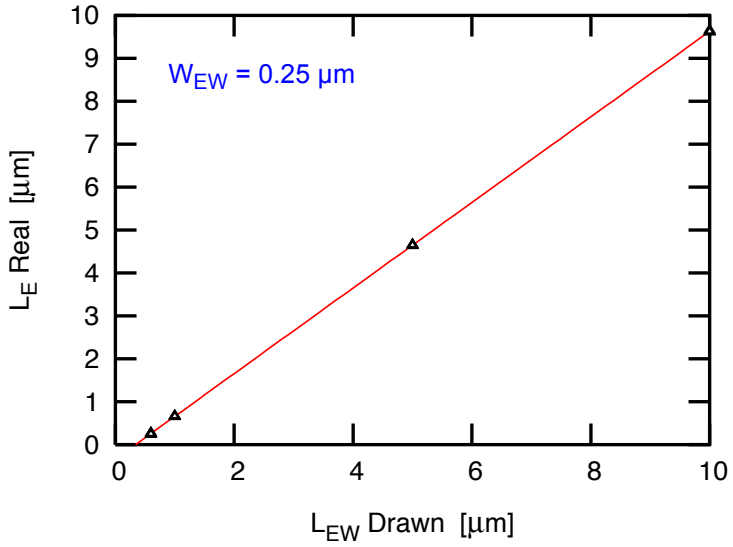
- In the same manner, it is possible to determine the actual dimensions of the emitter ($W_E$, $L_E$) after the spacer formation from the drawn dimensions of the emitter window ($W_{EW}$, $L_{EW}$)

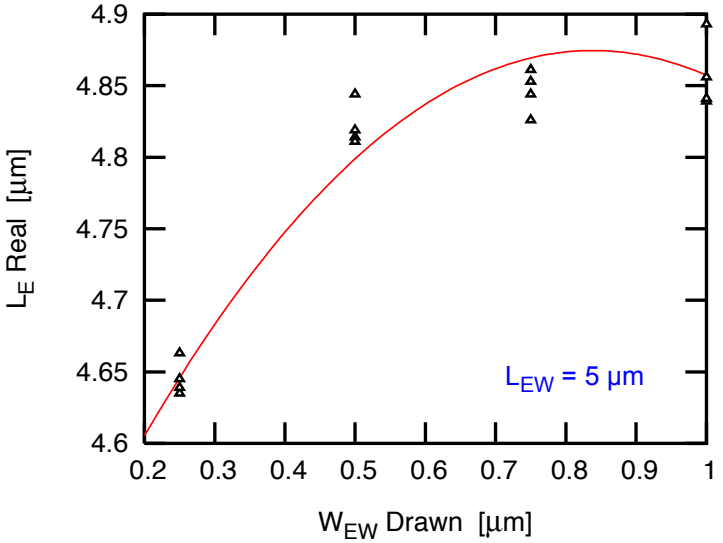
$$\begin{cases} L_E = a \cdot W_{EW}^2 + b \cdot W_{EW} \cdot L_{EW} + c \cdot W_{EW} + d \cdot L_{EW} + e \\ W_E = a' \cdot L_{EW}^2 + b' \cdot L_{EW} \cdot W_{EW} + c' \cdot L_{EW} + d' \cdot W_{EW} + e' \end{cases} \quad (3)$$

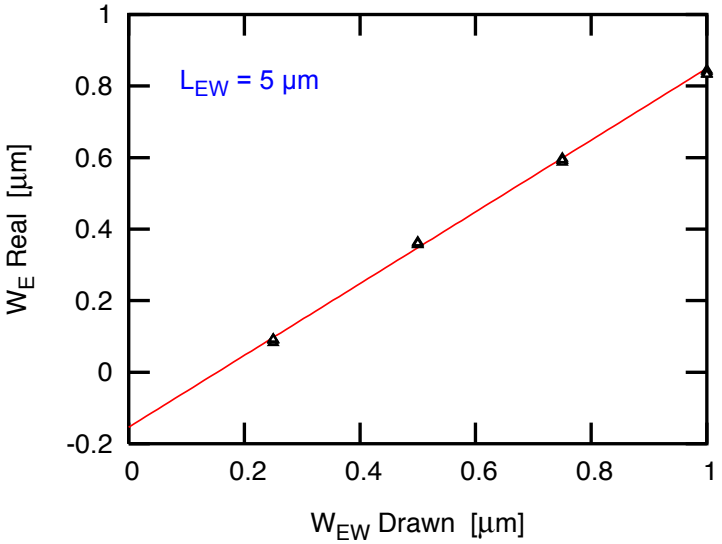
- Coefficients can be found in [3]

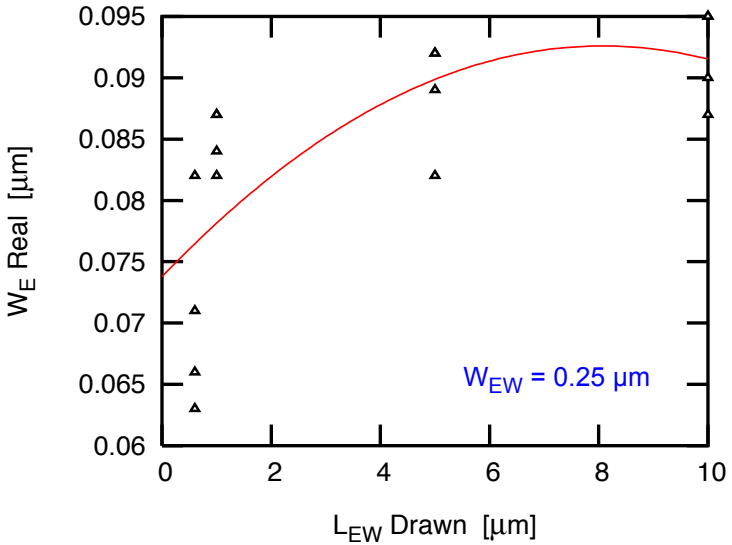
# Analysis of the emitter size after spacer formation

- Comparison between measurements and equation (3)



# Deduction of the total spacer width

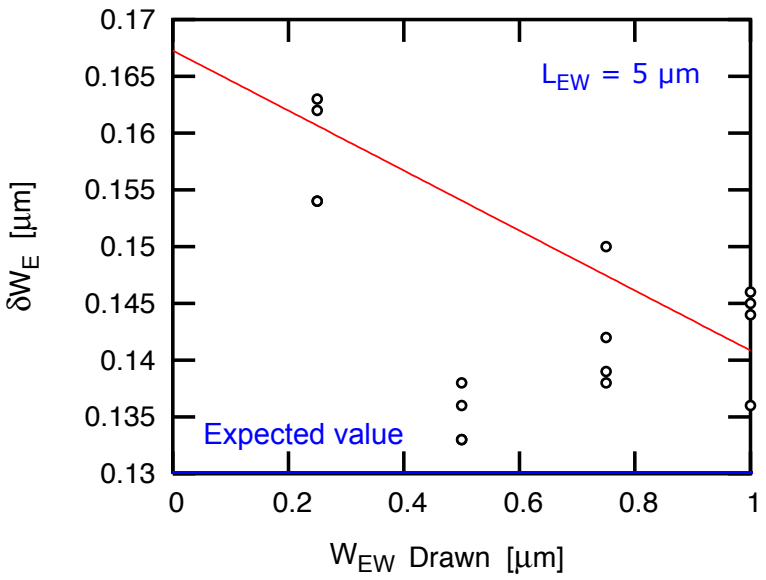
- Subtracting equation (3) from equation (2) allows to calculate the total width of the spacer

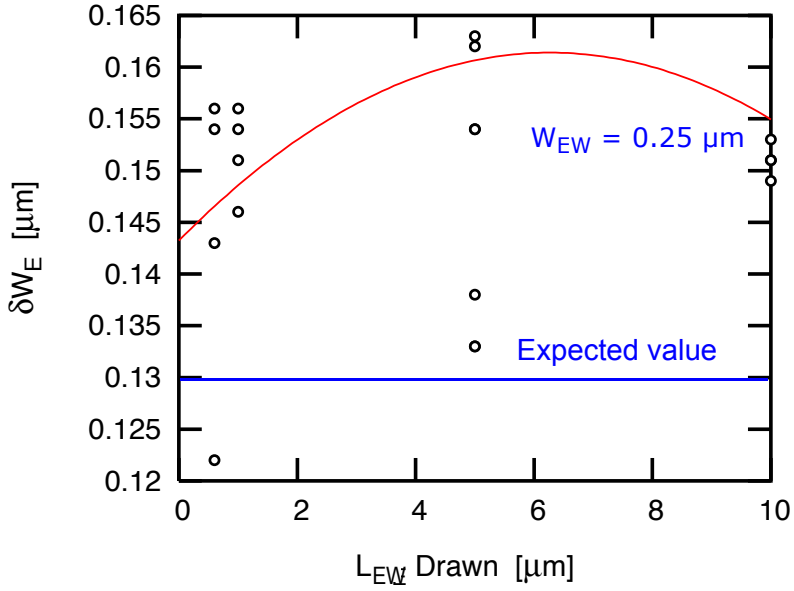
$$\begin{cases} \delta L_E = L^{*}_{EW} - L_E = a \cdot W^2_{EW} + b \cdot W_{EW} \cdot L_{EW} + c \cdot W_{EW} + d \cdot L_{EW} + e \\ \delta W_E = W^{*}_{EW} - W_E = a' \cdot L^2_{EW} + b' \cdot L_{EW} \cdot W_{EW} + c' \cdot L_{EW} + d' \cdot W_{EW} + e' \end{cases} \quad (4)$$

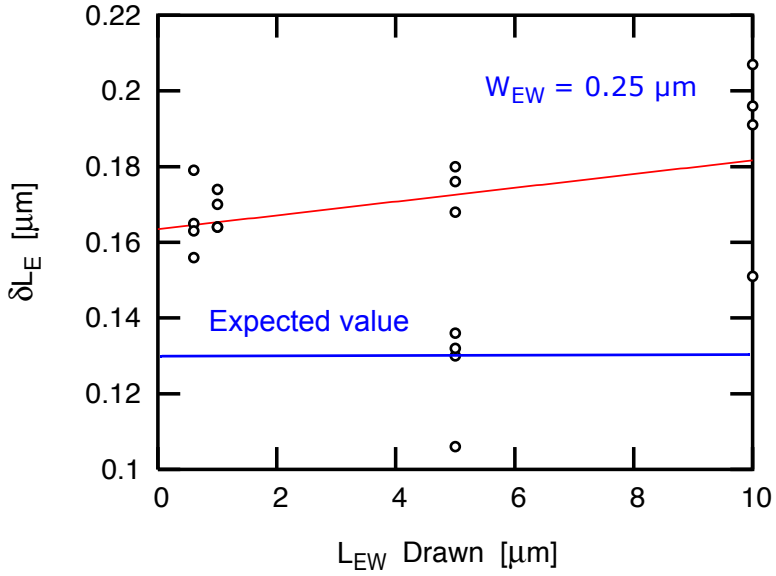
- Coefficients can be found in [3]

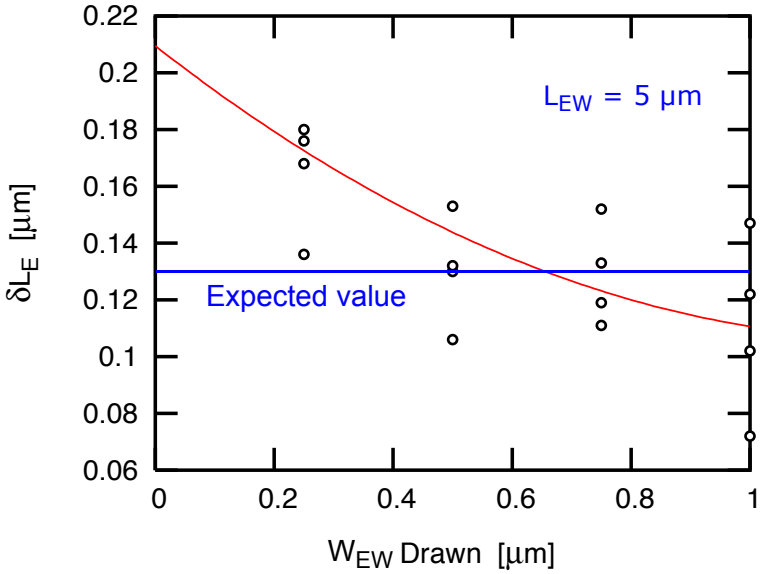
# Total spacer width

- Comparison between measurements and equation (4)



# Silicon sizes versus drawn sizes

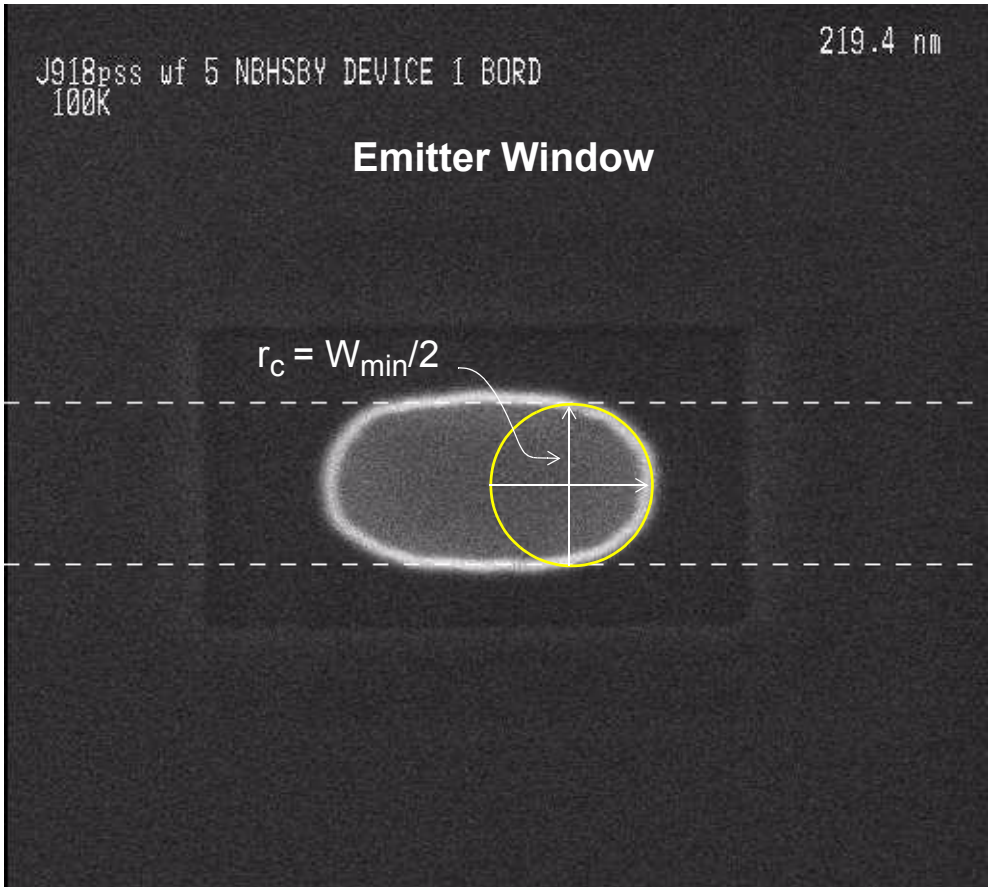
- From the previous equations (2), (3), (4) this table gives the actual emitter sizes ($W_E$, $L_E$), the difference between drawn and silicon dimensions ($\Delta i$), and the total spacer width ($\delta i$) for some of the transistors used for the determination of the geometry-scalable model parameters
- To be compared with the measured data (SEM pictures) given page 11

| | Drawn | | Actual | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Transistor name | $W_{EW}$ | $L_{EW}$ | $W_{EW}$ | $L_{EW}$ | $\Delta W_E$ | $\Delta L_E$ | $W_E$ | $L_E$ | $\delta W_E$ spacer | $\delta L_E$ spacer |
| NN122A6 | 0.25 | 0.6 | 0.223 | 0.425 | 0.027 | 0.175 | 0.078 | 0.435 | 0.145 | 0.165 |
| NN122A10 | 0.25 | 1 | 0.227 | 0.824 | 0.023 | 0.176 | 0.078 | 0.659 | 0.149 | 0.165 |
| NN122A50 | 0.25 | 5 | 0.250 | 4.82 | 0 | 0.18 | 0.089 | 4.65 | 0.161 | 0.173 |
| NN122A100 | 0.25 | 10 | 0.246 | 9.81 | 0.004 | 0.19 | 0.091 | 9.63 | 0.155 | 0.182 |
| NN122B50 | 0.5 | 5 | 0.495 | 4.94 | 0.005 | 0.06 | 0.341 | 4.80 | 0.154 | 0.144 |
| NN122C50 | 0.75 | 5 | 0.739 | 4.99 | 0.011 | 0.01 | 0.592 | 4.87 | 0.147 | 0.124 |
| NN122D50 | 1 | 5 | 0.982 | 4.97 | 0.018 | 0.03 | 0.841 | 4.86 | 0.141 | 0.111 |
| NN122B100 | 0.5 | 10 | 0.485 | 9.93 | 0.015 | 0.07 | 0.342 | 9.79 | 0.143 | 0.137 |
| NN122C100 | 0.75 | 10 | 0.723 | 9.98 | 0.027 | 0.02 | 0.592 | 9.98 | 0.131 | 0.100 |
| NN122D100 | 1 | 10 | 0.961 | 9.95 | 0.039 | 0.05 | 0.842 | 9.88 | 0.119 | 0.071 |
| NN122D10 | 1 | 1 | 0.973 | 0.984 | 0.027 | 0.016 | 0.832 | 0.842 | 0.141 | 0.142 |

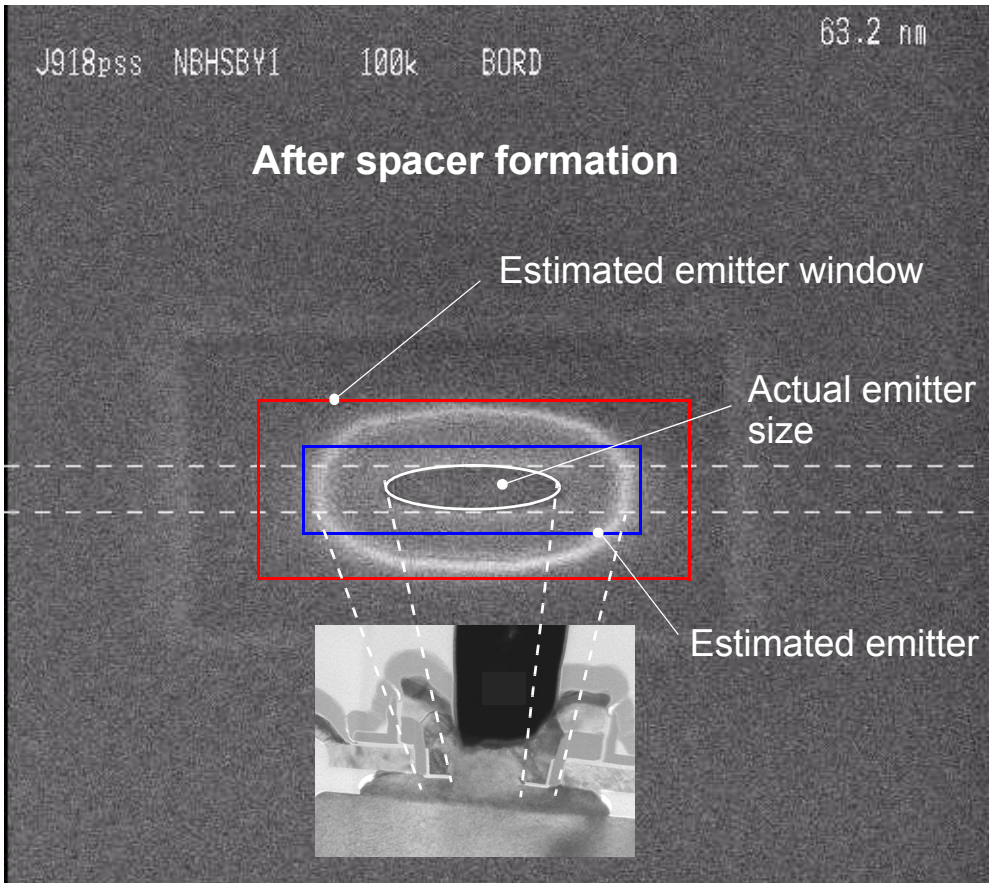
# Actual silicon sizes versus estimated sizes

- Estimated sizes versus actual emitteur dimensions for the smallest device

**Drawn emitter window 0.25 x 0.6 µm²**



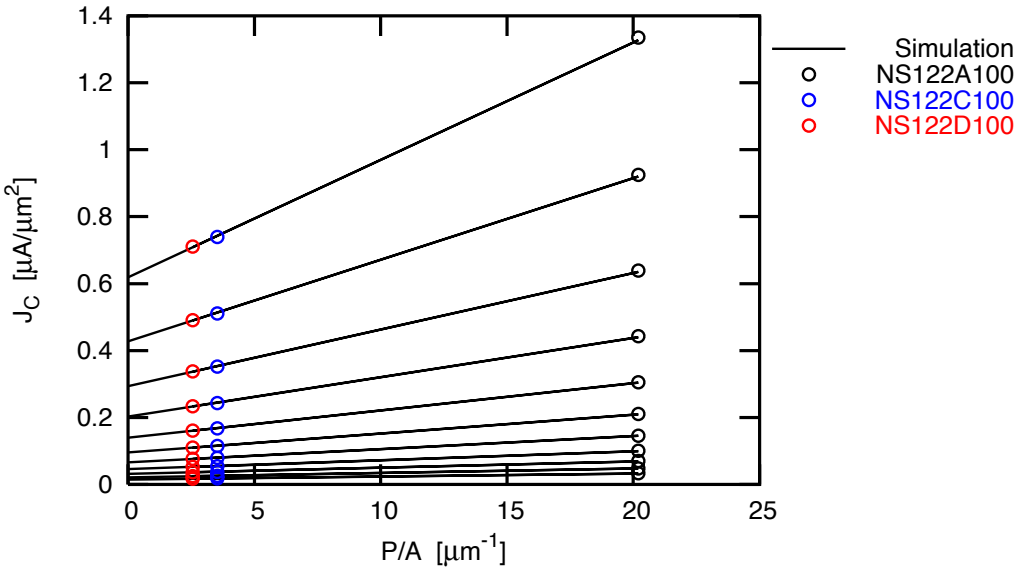

**Drawn emitter window 0.25 x 0.6 µm²**



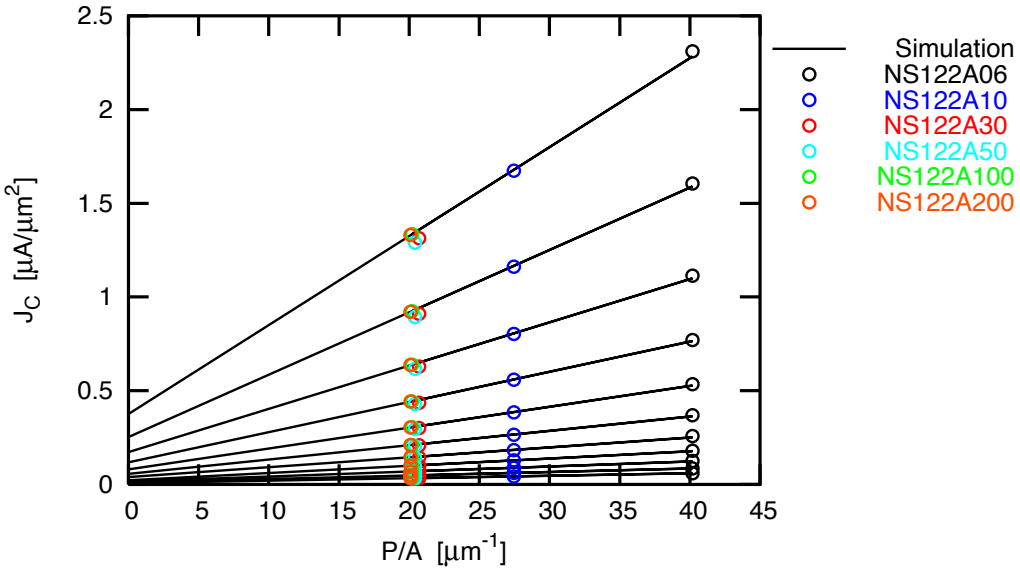
# Collector Current

- Extraction of *specific* parameters from actual emitter dimensions deduced from SEM pictures

**Variable emitter width and constant length (10µm)**



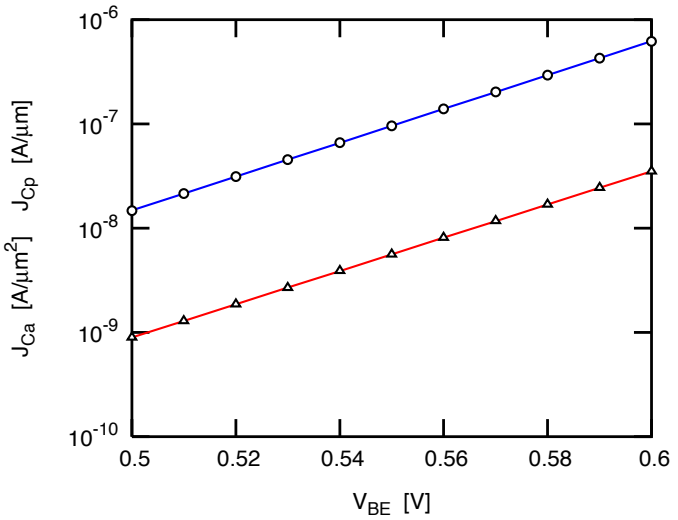

**Variable emitter length and constant width (0.25µm)**



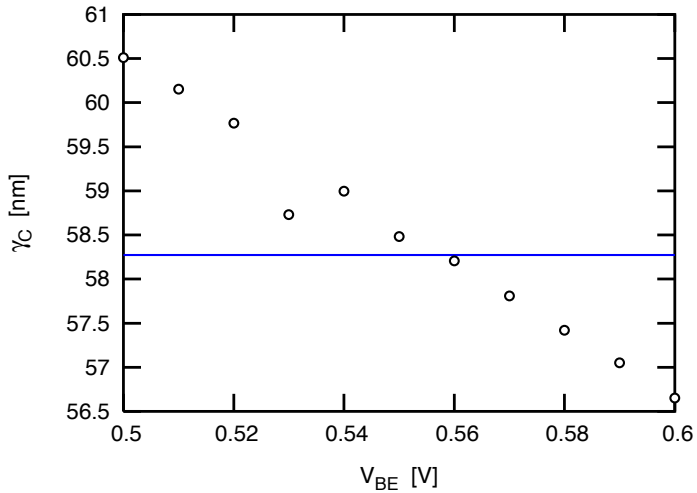

- Comments
  - Contrary to the previous analysis (page 5), now the geometry-dependence of the collector current for transistors with variable width and length is perfect.

# Collector Current

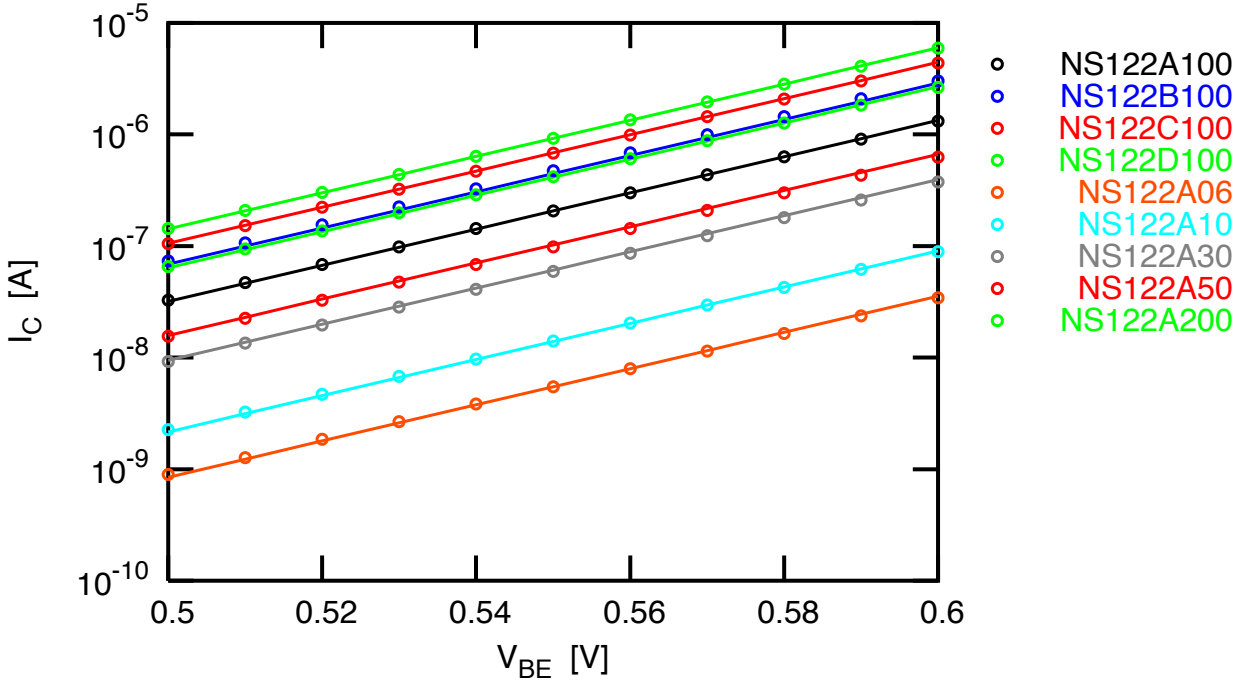
- Specific parameters obtained only from transistors with variable emitter width allow now to reproduce the geometry dependence of transistors with variable length, even for the smallest devices (see page 6 for comparison)




$\gamma_C$ = 58.3 nm

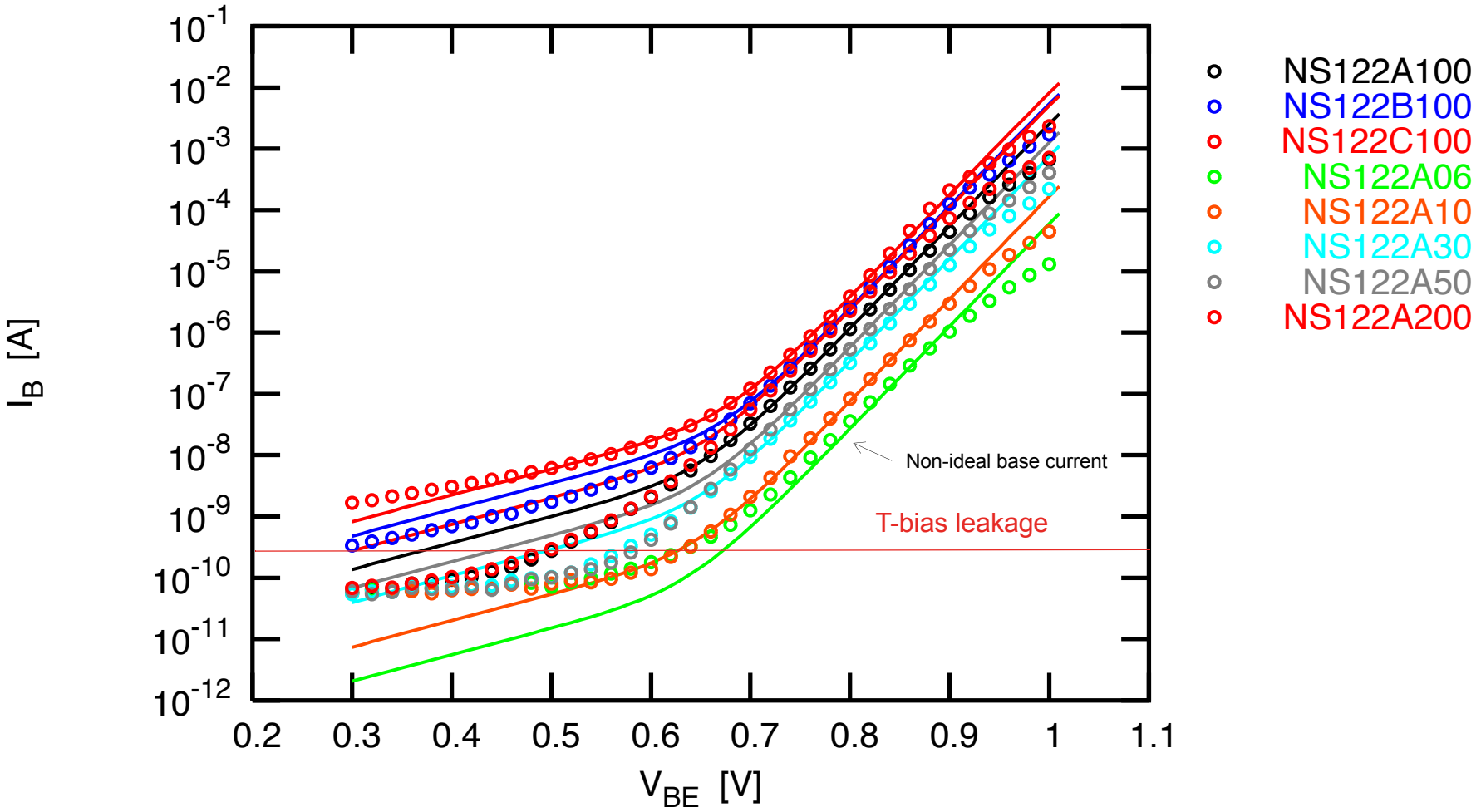



$C_{10A}$ = 5.60 $10^{-16}$ fC.A.µm$^{-4}$ $Q_{P0A}$ = 3.87 fC.µm$^{-2}$ $\gamma_C$ = 58.3 nm



# Base current

- Same remark for the base current

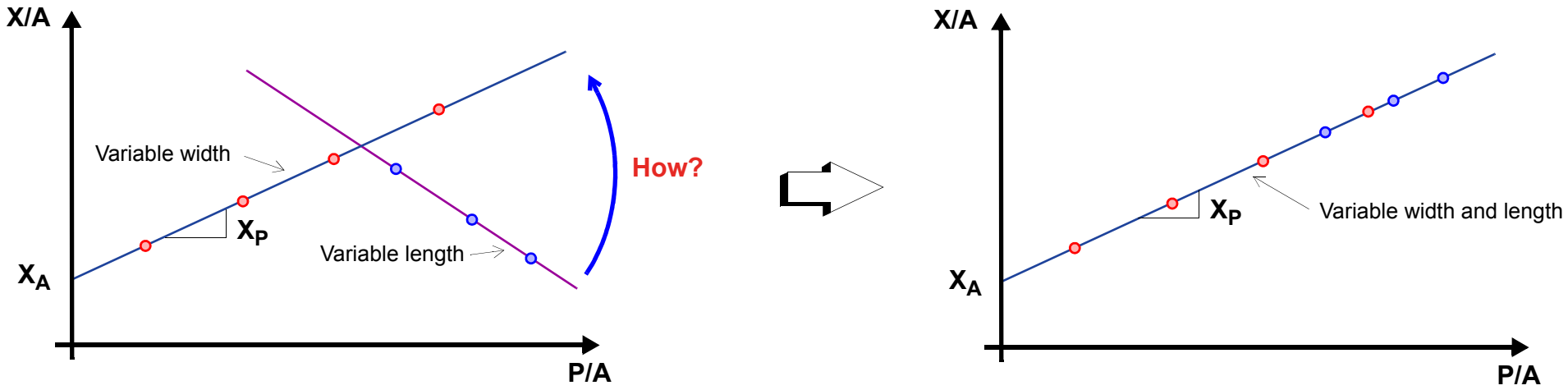


# First conclusion

- We have shown that the knowledge of the actual emitter sizes on wafer is essential to build an accurate bipolar scalable model valid for both variations with the width and the length of the device.
- Using the dimensions coming from SEM pictures that allow to accurately fit all electrical values (currents, capacitance, transit time, ...) which depend on the emitter size
  - that means the effect of the variation of the transistor dimensions is more sensitive *on the geometry-scaling issue* than a possible variation of the vertical doping profile with the size of the transistor
- No need of new geometry-scalable equations
- No need of new extraction procedures
- But, this approach (SEM pictures) cannot be systematically used
  - Not easy to do
  - Time consuming
  - Not performed on the same wafer and on the same die which will be after used for the parameter extraction
- In consequence, now the objective is to find a way to estimate the actual size of the transistor directly from the analysis of electrical measurements
  - Myth or reality?... We will see!...

# Principle

- Must be simple in order to obtain robust and reproducible results
- Objective




- Prerequisite and assumption
  - For 2D devices the process is scalable, that is to say the characteristics X/A vs. P/A are linear.
  - In consequence, the slope $X_P$ and intercept $X_A$ are known

  That means the uncertainty we have on A and P is negligible for 2D devices (L>>W). This assumption is verified from the SEM pictures.
- Question
  - Is it possible to compute from electrical measurements the actual values (W,L) of the transistors which are not aligned with the 2D devices?

# Principle

- We assume that for all devices the relations between the supposed emitter sizes and the actual dimensions on silicon are defined by

$$\begin{cases} W_{actual} = W + \Delta\mathbf{W} \\ L_{actual} = L + \Delta\mathbf{L} \end{cases}$$

- Therefore, for all devices the actual area A and perimeter P can be written (see Appendix A)

$$\begin{cases} A = (W + \Delta\mathbf{W}) \cdot (L + \Delta\mathbf{L}) - \alpha \\ P = 2 \cdot (W + \Delta\mathbf{W} + L + \Delta\mathbf{L}) - \beta \end{cases}$$

$\alpha$ and $\beta$ are used to take into account the corner rounding.

- A geometry-scalable value (collector current) can be written

$$X = X_A \cdot A + X_P \cdot P = X_A \cdot \{(W + \Delta\mathbf{W}) \cdot (L + \Delta\mathbf{L}) - \alpha\} + X_P \cdot \{2 \cdot (W + \Delta\mathbf{W} + L + \Delta\mathbf{L}) - \beta\}$$

• XA, XP, W, L, $\alpha$, $\beta$ are known
• $\Delta\mathbf{W}$ and $\Delta\mathbf{L}$ are the unknown

or

$$X = X_A \cdot \{A_0 + W \cdot \Delta\mathbf{L} + L \cdot \Delta\mathbf{W} + \Delta\mathbf{W} \cdot \Delta\mathbf{L}\} + X_P \cdot \{P_0 + 2 \cdot \Delta\mathbf{L} + 2 \cdot \Delta\mathbf{W}\} \quad (5)$$

with

$$\begin{cases} A_0 = W \cdot L - \alpha \\ P_0 = 2 \cdot (L + W) - \beta \end{cases}$$

# Principle

- Rearranging (5) we can deduce

$$X - X_A \cdot A_0 - X_P \cdot P_0 = \Delta\mathbf{L} \cdot \{X_A \cdot W + 2 \cdot X_P\} + \Delta\mathbf{W} \cdot \{X_A \cdot L + 2 \cdot X_P\} + X_A \cdot \Delta\mathbf{W} \cdot \Delta\mathbf{L} \quad (6)$$

- $\Delta\mathbf{W}$ and $\Delta\mathbf{L}$ are supposed small enough allowing to neglect $X_A.\Delta\mathbf{W}.\Delta\mathbf{L}$
  - Therefore (6) is equivalent to

$$Y = a_1 \cdot f_1 + a_2 \cdot f_2$$

with

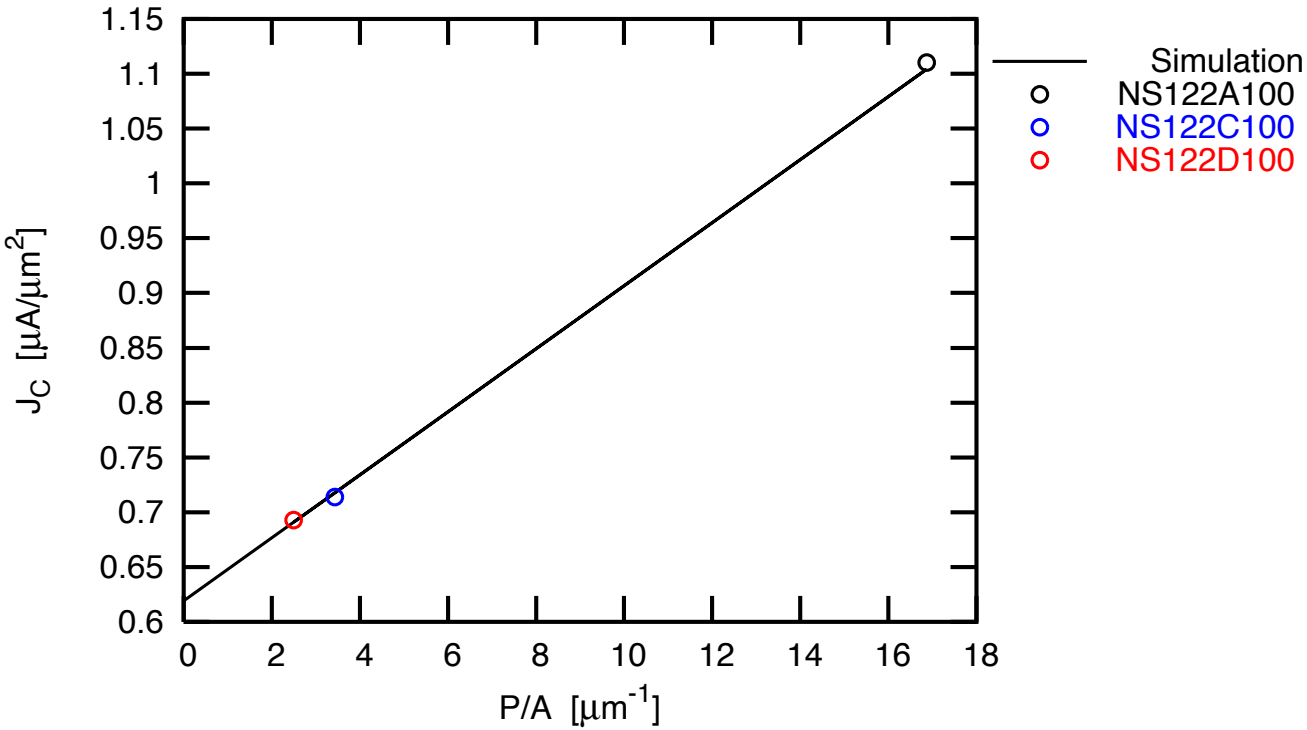
$$\begin{cases} Y = X - X_A \cdot A_0 - X_P \cdot P_0 \\ f_1 = X_A \cdot W + 2 \cdot X_P \\ f_2 = X_A \cdot L + 2 \cdot X_P \end{cases} \quad \text{and} \quad \begin{cases} a_1 = \Delta\mathbf{L} \\ a_2 = \Delta\mathbf{W} \end{cases}$$

- Knowing $f_1$ and $f_2$, $a_1$ and $a_2$ can be easily determined with multi-variable linear regression.

# Extraction steps

## Step 1: extraction of specific collector currents from 2D devices

- $V_{BE}$ = 0.6 V and $V_{BC}$ = 0 V
- Transistor NS122B100 was removed because it was not pecfectly aligned with the others

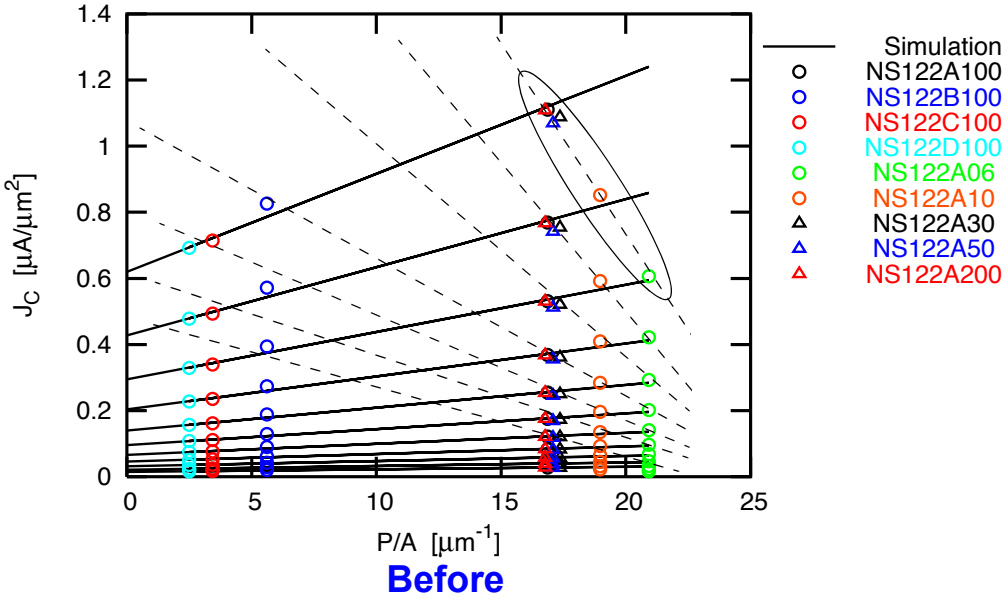



## Step 2: computation of ΔW and ΔL for the devices which are not aligned with the 2D devices

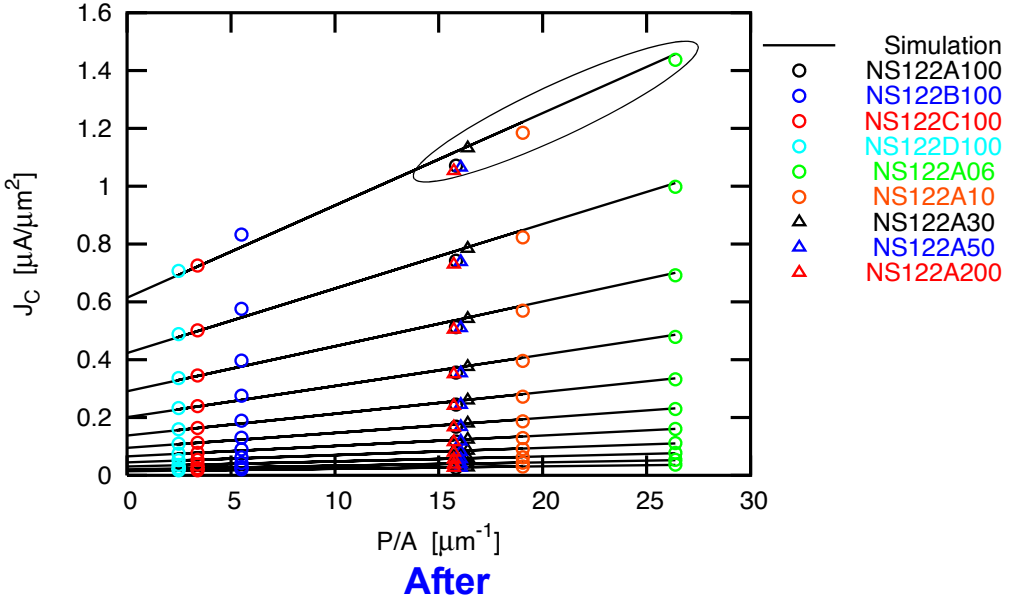
- NS122A06, NS122A10, NS122A30
- **ΔL = -0.284 µm**
- **ΔW = -0.008 µm**

# Extraction steps

## Step3: verification on all devices

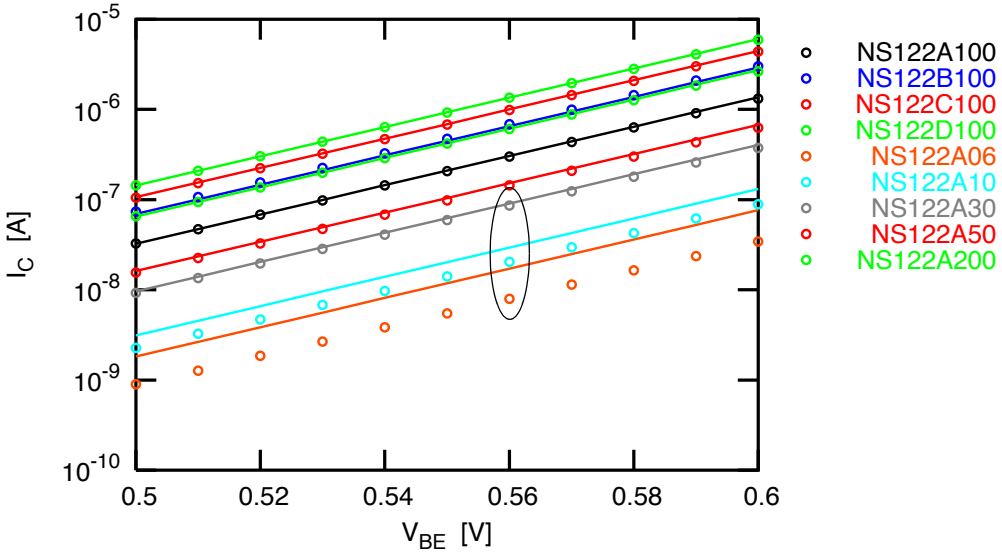



**Before**

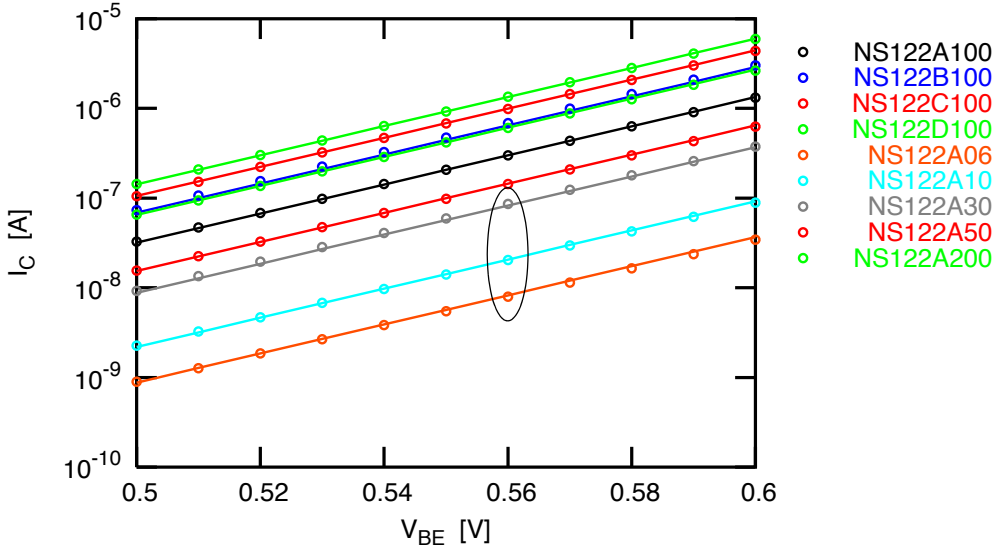



**After**

$C_{10A}$ = 5.60 $10^{-16}$ fC.A.µm$^{-4}$ $Q_{P0A}$ = 3.87 fC.µm$^{-2}$ $\gamma_C$ = 48.2 nm

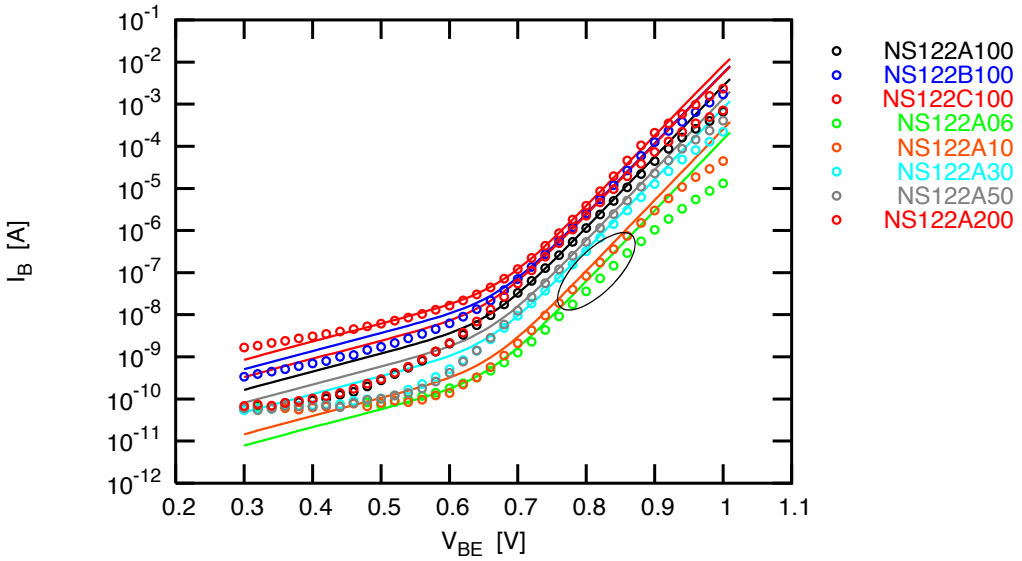


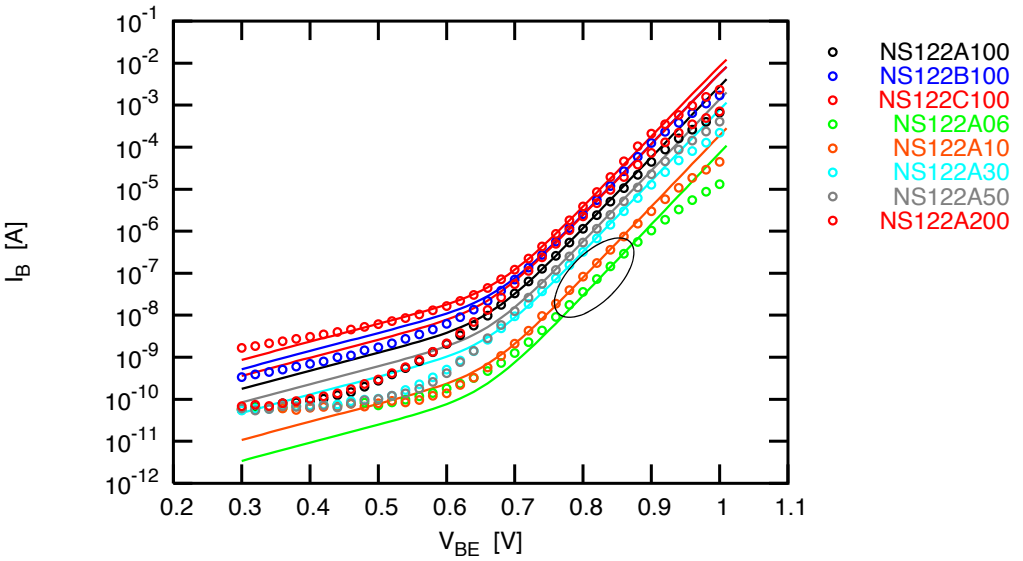

$C_{10A}$ = 5.77 $10^{-16}$ fC.A.µm$^{-4}$ $Q_{P0A}$ = 3.88 fC.µm$^{-2}$ $\gamma_C$ = 44.0 nm



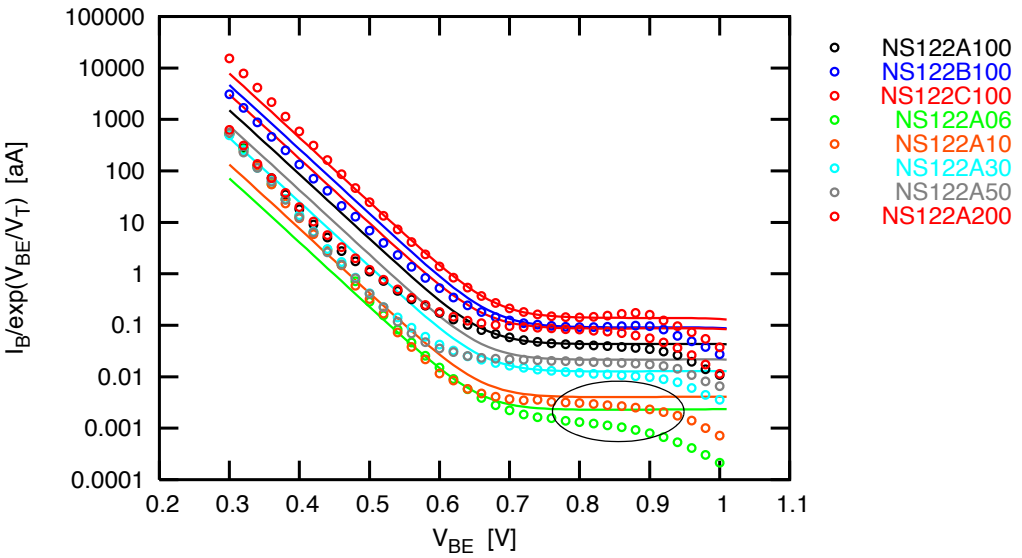
# Validation on base currents

- Similar improvements on the base current (*base current not ideal on the smallest device*)

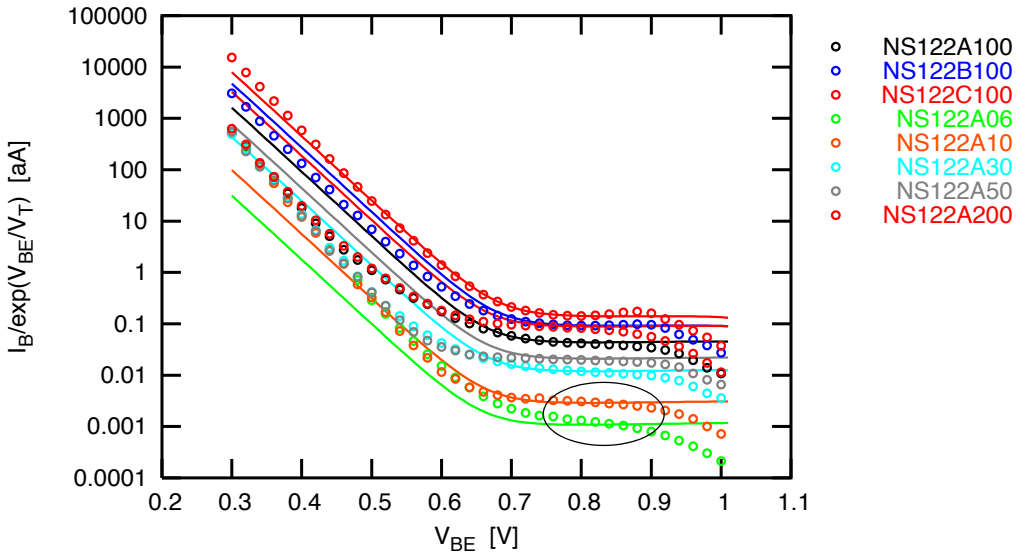



**Before**



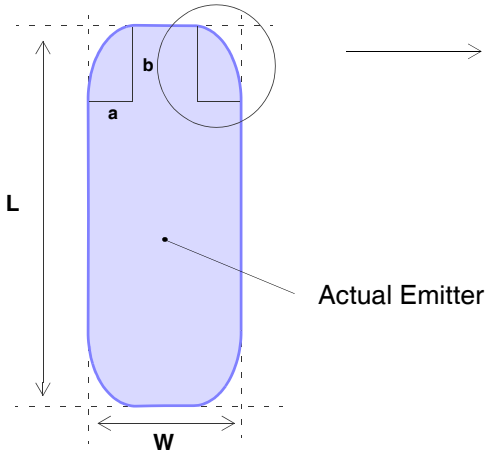

**After**

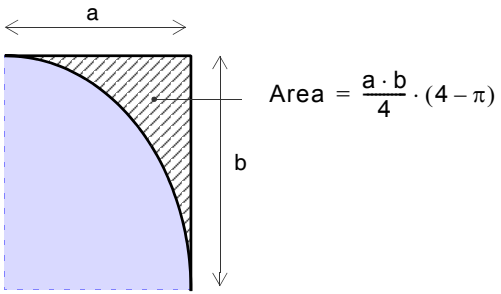


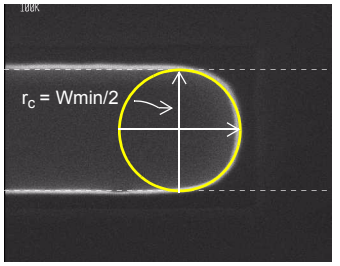
# Summary and conclusion

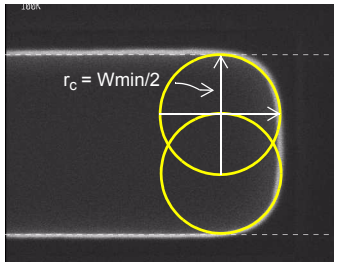
- The knowledge of the actual emitter size on wafer is crucial for reliable bipolar specific parameter extraction
- For that, 2 ways were explored
  - Determination of the actual emitter area from SEM measurements and building a simple model which allows to link the drawn dimensions to the actual size of the devices.
  - Determination of the actual sizes from electric measurement (small devices) with some assumptions
    - 2D devices are geometry-scalable and not affected by the uncertainty of the sizes.
    - Same deviation between the estimated and the actual emitter dimensions for all devices
- Both approaches gives excellent results for all measured transistors
- The first method is difficult to set up, time consuming and cannot be done systematically on the die which will be used for specific parameter extraction. For these reasons, the second method is preferred.
- This methodology is totally compatible with the existing geometry-scaling laws, and the concept of effective emitter area used in HICUM
  - Only one set of equations (see Appendix A) must be added in other to better estimate the actual sizes of the device on silicon from the mask sizes.

# Appendix A: Corner rounding




## Spherical angles

- $\begin{cases} A = WL - ab(4-\pi) \\ P = 2(W+L) - 4 \cdot (a+b) + \pi \cdot \{3(a+b) - \sqrt{(3a+b) \cdot (a+3b)}\} \end{cases}$

## Circular angles

- a = b = r
- By default r = $W_{min}/2$ (good approximation)

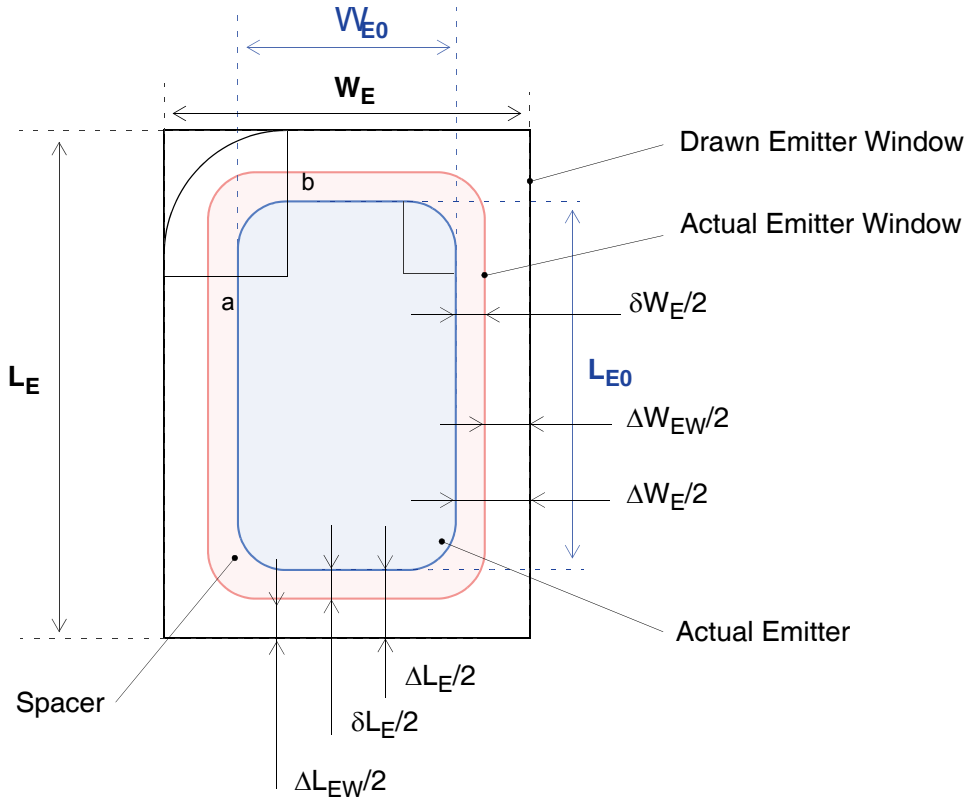
- $\begin{cases} A = WL - r^2(4-\pi) \\ P = 2(W+L) - 2r(4-\pi) \end{cases}$

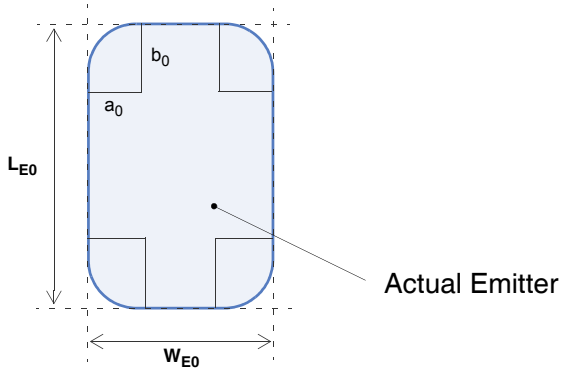
## General expression

- $\begin{cases} A = WL - \alpha \\ P = 2(W+L) - \beta \end{cases}$ where $\alpha$ and $\beta$ are used to take into account the corner rounding

# Corner rounding

## From drawn dimensions to actual emitter sizes




- with $\begin{cases} W_{E0} = W_E - \Delta W_E \\ L_{E0} = L_E - \Delta L_E \\ a_o = a - \Delta W_E \\ b_o = b - \Delta L_E \end{cases}$ and $\begin{cases} \Delta W_E = \Delta W_{EW} + \delta W_E \\ \Delta L_E = \Delta L_{EW} + \delta L_E \end{cases}$

- $\Delta W_{EW}$ and $\Delta L_{EW}$ are the difference between drawn and actual emitter window size
- $\delta W_E$ and $\delta L_E$ are the spacer width

# Appendix B: On the bias dependence of $\gamma_C$

## Simple explanation of bias dependence of $\gamma_C$ at low current densities

- $\gamma_C$ has been defined as the ratio of the peripheral collector current to the area collector current, $\gamma_C = J_{CP}/J_{CA}$
- Why this ratio is not constant with $V_{BE}$?
- Study at low current densities (and $V_{BC}$=0V) in order to avoid the voltage drop in the series resistances and the high injection effects.
- Using the Gummel-Poon formulation, $J_{CA}$ is proportional to $\exp(V_{BE}/V_T)$ via the saturation current $J_{SA}$. Moreover, $J_{CA}$ depends on the internal BE depletion charge, which can be modeled, with some approximations, by introducing an area reverse Early voltage $V_{ERA}$

$$J_{CA} \approx J_{SA} \cdot \left\{1 - \frac{V_{BEi}}{V_{ERA}}\right\} \cdot e^{\frac{V_{BEI}}{V_T}}$$

- In the same manner, by introducing a peripheral saturation current $J_{SP}$ and a peripheral reverse Early voltage $V_{ERP}$, we can define $J_{CP}$

$$J_{CP} \approx J_{SP} \cdot \left\{1 - \frac{V_{BEi}}{V_{ERP}}\right\} \cdot e^{\frac{V_{BEI}}{V_T}}$$

- Therefore $\gamma_C$ can be calculated

$$\gamma_C = \frac{J_{CP}}{J_{CA}} = \frac{\left\{1 - \frac{V_{BEi}}{V_{ERP}}\right\}}{\left\{1 - \frac{V_{BEi}}{V_{ERA}}\right\}} \cdot \frac{J_{SP}}{J_{SA}} = \frac{\left\{1 - \frac{V_{BEi}}{V_{ERP}}\right\}}{\left\{1 - \frac{V_{BEi}}{V_{ERA}}\right\}} \cdot \gamma_{C0} \quad \text{with} \quad \gamma_{C0} = \frac{J_{SP}}{J_{SA}}$$

# On the bias dependence of $\gamma_C$

- Assuming $V_{ERA}$ and $V_{ERP}$ large enough in comparison with $V_{BEi}$ (not really exact for advance HBTs) we can write

$$\gamma_C \approx \left\{1 - \frac{V_{BEi}}{V_{ERP}} + \frac{V_{BEi}}{V_{ERA}}\right\} \cdot \gamma_{C0} = \left\{1 - V_{BEi} \cdot \left(\frac{1}{V_{ERP}} - \frac{1}{V_{ERA}}\right)\right\} \cdot \gamma_{C0} \qquad (7)$$

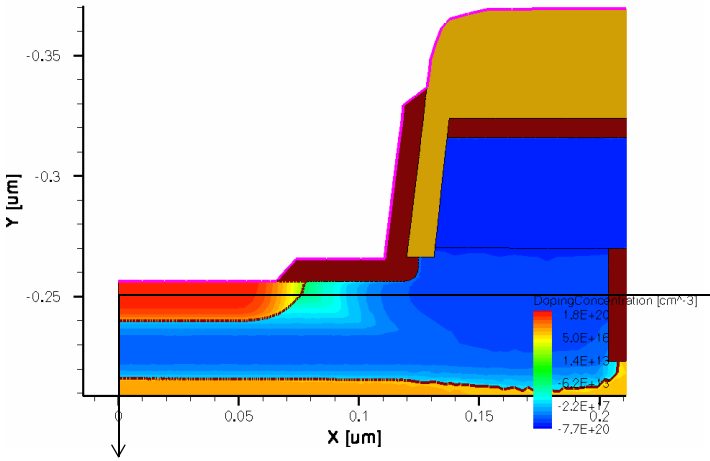
- If $V_{ERP}$ is not equal to $V_{ERA}$, $\gamma_C$ depends on $V_{BEi}$

## Dependence of $V_{ER}$ with process parameters

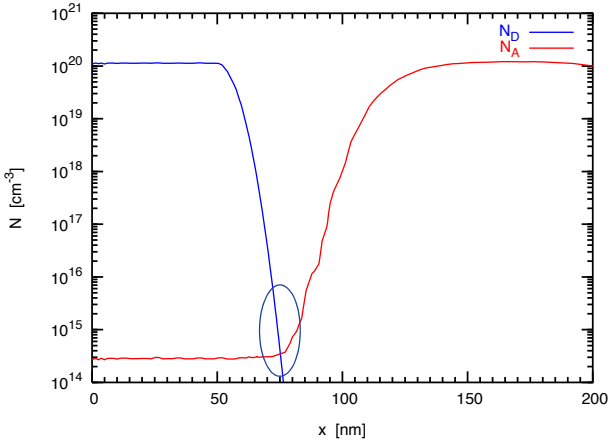
- The reverse Early voltage is used to model the charge stored in the BE depletion region. In first approximation
- $V_{ER} \approx \frac{Q_{B0}}{C_{JE}}$ $\quad Q_{B0} \propto N_{AB} \cdot W_{B0} \cdot A_E$ and $\overline{C_{JE}} \propto A_E \cdot \sqrt{N_{AB}}$ which gives finally
- $V_{ER} \propto \sqrt{N_{AB}} \cdot W_{B0}$
- Therefore, $V_{ER}$ depends strongly on the base doping. For advanced HBTs, the lateral base doping and the base doping under the emitter are very different (see next page), that can explain why $V_{ERA}$ is not equal to $V_{ERP}$.

# On the bias dependence of $\gamma_C$

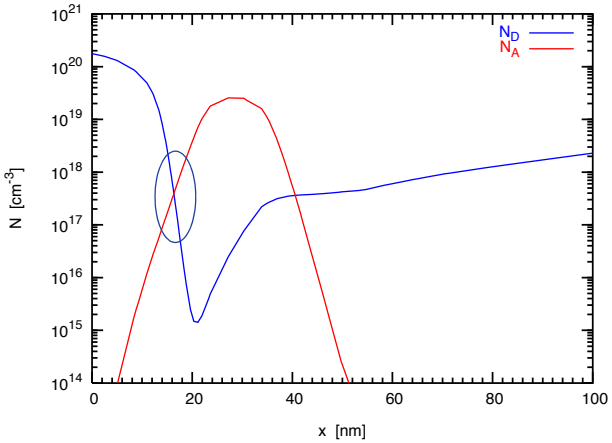
- Vertical and lateral BE doping profiles in advanced HBTs




Lateral profile




Vertical Profile




- The BE vertical and lateral profiles are very different
- The lateral base doping (at BE the junction) is lower than the vertical base doping
- $V_{ERP}$ cannot be equal to $V_{ERA}$. $V_{ERP}$ must be lower than $V_{ERA}$.
- From equation (7), that explains the decease of $\gamma_C$ with $V_{BE}$

# On the bias dependence of $\gamma_C$

## New HICUM $I_T$ formulation

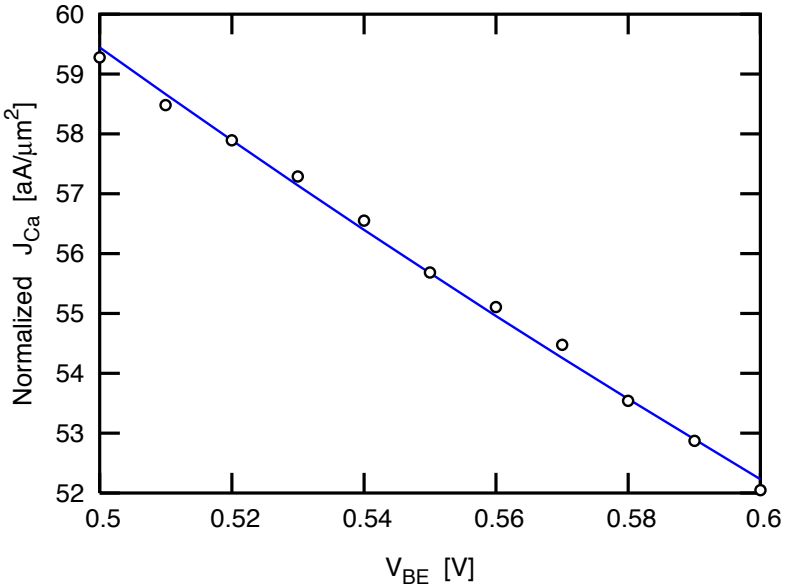
- We can demonstrate that a peripheral reverse Early effect different than area reverse Early effect can be taken into account by introducing a new $h_{jEi}$ parameter ($h_{jEp}$) for the peripheral part of the collector current. At low current densities and $V_{BC}$=0V, the transfer current can be then written

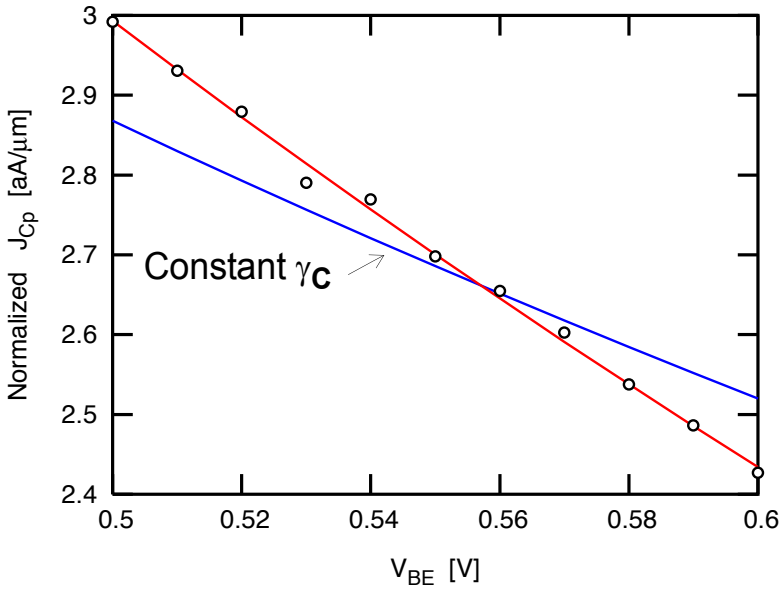
$$I_T \approx \frac{J_{SA} \cdot A \cdot \left\{1 + \gamma_{co} \cdot \frac{P}{A}\right\} \cdot e^{\frac{V_{BE}}{V_T}}}{1 + h_{jEi} \cdot \left\{\frac{1 + \gamma_h \cdot \gamma_{co} \cdot \frac{P}{A}}{1 + \gamma_{co} \cdot \frac{P}{A}}\right\} \cdot \frac{Q_{jEi}}{Q_{p0}}} \qquad (8)$$

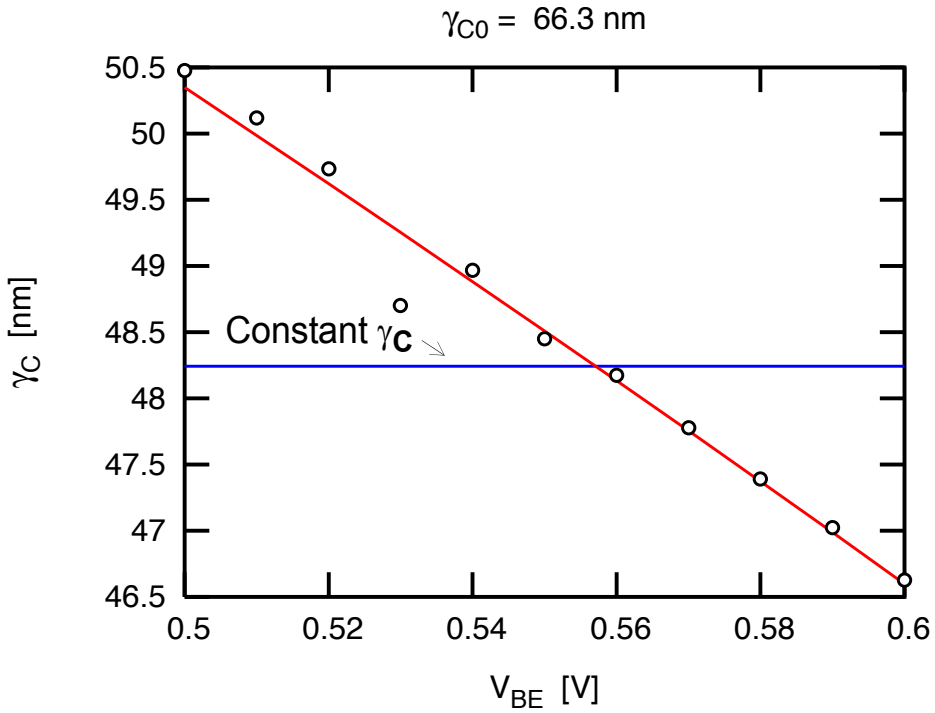
- with $\gamma_h = \frac{h_{jEp}}{h_{jEi}}$ and $\gamma_{C0} = \frac{J_{SP}}{J_{SA}}$ where $J_{SA}$ and $J_{SP}$ are respectively the area part and the peripheral part of the saturation surrent $I_S = C_{10}/Q_{P0}$
- If the area and peripheral Early effect are similar ($\gamma_h$ = 1), equation (8) is identical to HICUM/L2 formulation.

# On the bias dependence of $\gamma_C$

## Experimental results



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[1] http://www.dotfive.eu

[2] D. Céli, “Review of some HICUM Geometry Scaling Laws: Issue and Proposal“, 7th HICUM Workshop, Dresden, June 2007.

[3] D. Céli, “B3T: Emitter Dimension - Part II”, Internal ST document, dm138.09, September 2009.