HICUM Status in Eldo/EldoRF

Ahmed Fathy Abo-Elhadeed
Senior Development Engineer
Device Modeling Team

Outline

- **Introduction**
- **Speed comparison**
- **V2.23 parameters default**
- **Conclusion**

Introduction

Version 2.22

- ddx() was first used in the VerilogA code
- ddx() conversion was not supported inside “Motorola ADMS”
- Based on communications with the model developers, we reverted back to V2.21 implementation for the code portions using ddx() as these parts in V2.21 were 100% equivalent to those in V2.22
- NQS was not handled in the VerilogA code
- We inserted the NQS analytically (from older implementation) for V2.22

Introduction

Version 2.23

- ddx() is still used in this version
- Recently, we enhanced the converter to handle ddx()
- We implemented this version twice using two techniques:
  - Direct implementation: Using the developed converter
  - Optimized Mentor implementation: Using the developed converter with some manual optimization.
- NQS is now handled in the VerilogA code using external nodes
- We followed the same technique (extra nodes) to implement the NQS inside Eldo

Speed comparison

We did two types of speed comparisons:

1. **V2.23:**
   - **We compared the speed of the two implementations done using the Direct method and the optimized Mentor method to see the effect of the code optimization.**

2. **V2.23 vs. V2.22:**
   - **We compared speed of the optimized V2.23 and that of V2.22 to see how slow/fast is the new version compared to the old one for the QS mode.**
   - **We also detected the speed loss due to NQS extra nodes in v2.23 by comparing the speed loss (QS/NQS) for V2.22 (analytically based) and the same quantity for V2.23 (extra nodes).**

Speed comparison

- **Comparison done on a Linux 32 bits machine.**
- **Testcases used are all running transient simulations.**
- **10 testcases were used for the comparison:**

Test1	**3 BJT design**	**Test6**	**23 BJT design**
Test2	**3 BJT Mixer**	**Test7**	**27 stage inverter, 27 BJT**
Test3	**8 BJT Mixer**	**Test8**	**6 stage inverter, 12 BJT**
Test4	**6 BJT Latch**	**Test9**	**23 BJT Gilbert cell**
Test5	**51 BJT design**	**Test10**	**2 BJT amplifier**

Speed comparison (V2.23)

	Time (s)	Time (s)	Speed up
Circuit	Normal	Mentor	Normal/Mentor
Test1	4827	980	4.93X
Test2	463	106	4.37X
Test3	764	161	4.73X
Test4	2778	766	3.63X
Test5	6156	1140	5.4X
Test6	2401	535	4.84X
Test7	4302	952	4.52X
Test8	1813	401	4.52X
Test9	682	175	3.9X
Test10	2160	474	4.56X
Total	26346	5690	4.63X
Average			4.54X

It should be noted that the both techniques show exactly the same results, number of iterations and device calls.

Speed comparison (V2.22 versus V2.23)

	Time (s)	Time (s)	Speed up
Circuit	V2.22	V2.23	V2.23/V2.22
Test1	912	1010	0.90X
Test2	116	111	1.04X
Test3	144	161	0.89X
Test4	708	773	0.92X
Test5	1052	1137	0.92X
Test6	440	597	0.74X
Test7	886	973	0.91X
Test8	345	402	0.86X
Test9	159	173	0.92X
Test10	440	481	0.90X
Total	5195	5818	0.89X
Average			0.90X

Speed comparison (V2.22 versus V2.23)

	Time (s)	Time (s)	Speed loss	Time (s)	Time (s)	Speed loss
Circuit	V2.22 (QS)	V2.22 (NQS)	V2.22(QS) / V2.22(NQS)	V2.23 (QS)	V2.23 (NQS)	V2.23(QS) / V2.23(NQS)
Test1	950	943	1.01X	1009	1065	0.95X
Test2	113	128	0.89X	107	115	0.93X
Test3	152	253	0.6X	163	340	0.48X
Test4	712	723	0.98X	797	828	0.96X
Test5	1057	1191	0.89X	1137	1257	0.90X
Test6	438	512	0.86X	534	619	0.86X
Test7	844	925	0.91X	934	1034	0.90X
Test8	343	349	0.98X	400	484	0.83X
Test9	160	165	0.97X	173	197	0.88X
Test10	430	543	0.79X	472	514	0.92X
Total	5199	5732	0.91X	5727	6453	0.89X
Average			0.89X			0.86X

V2.23 parameters default

- **The default of the following parameters are set to zero:**
  - **t0 → Low current forward transit time at VBC=0V**
  - **dt0h → Time constant for base and B-C space charge layer width modulation**
  - **tbvl → Time constant for modeling carrier jam at low VCE**

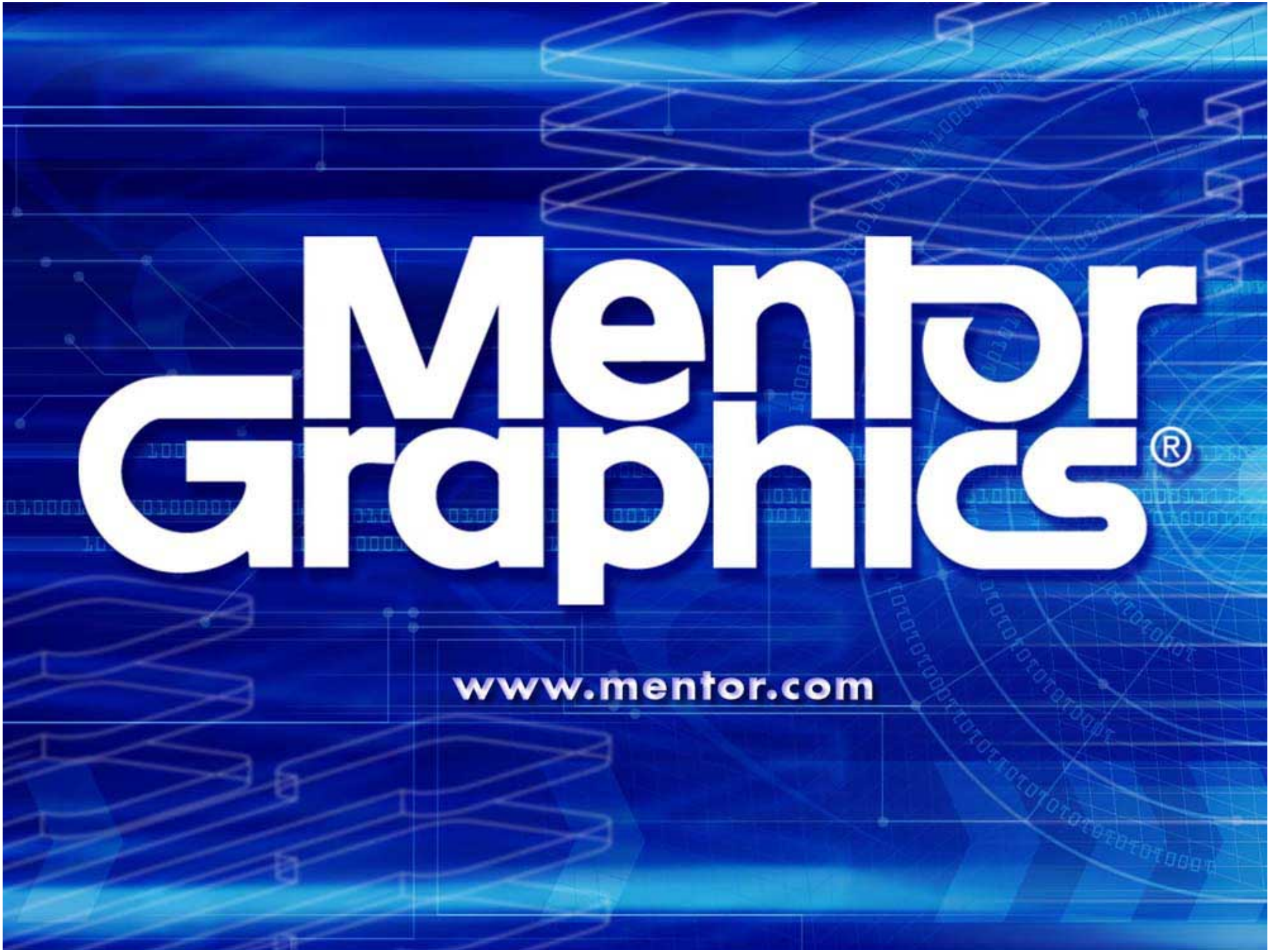
- **Physically, these parameters are in the range of Pico seconds**

- **If a user defines the NQS parameters (alqf, alit, flnqs) without defining t0, dt0h and tbvl, leaving them to take the zero default, a crash will occur**

- **We suggest to change the default of the parameters t0 , dt0h, tbvl to 1ps OR to switch off the NQS if these parameters are equal zero to avoid the problem**

Conclusion

- **The performance of an optimized implementation for V2.23 was presented showing a speed up of 4.54X compared to the direct implementation**
- **The results of both implementations are exactly matching the original Verilog-A results**
- **Using the optimized technique the performance of V2.23 is almost the same as the older version V2.22**
- **The new optimized V2.23 will be in the AMS 2009.2 release**
- **There is almost no speed loss between V2.23 and V2.22 despite the use of extra nodes to model the NQS effect for the new version**
- **It is required to change the default values of the parameters t0, dt0h and tbvl to avoid a probable issue if NQS is active**


Mentor Graphics®
www.mentor.com