Design and Simulation of Wideband LNAs up to 60 GHz

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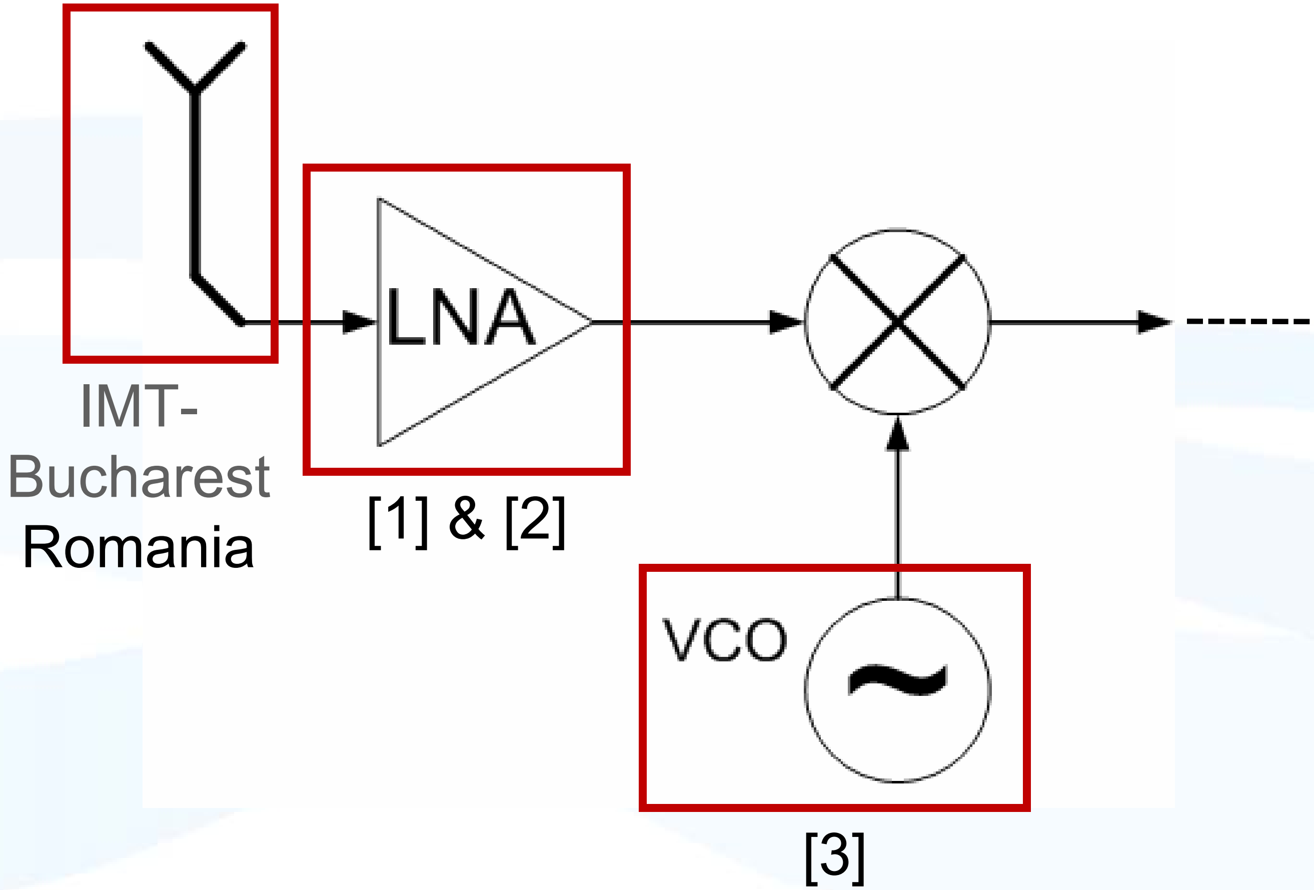
Department of Electrical, Electronic & Computer Engineering
Kgoro ya Merero ya Mohlagase, Elektroniki & Bointšinere bja Khomphutha

Research framework



Previous narrowband 60 GHz LNA attempt

- Inductive emitter degeneration input matching
- 22 dB Gain (3 stages)
- 100 mW power consumption

- Limited simulation due to HIT-kit incompatibility with Mentor Graphics IC flow
  - No DRC was possible

Real-world applications

60 GHz LNA:

- High data rate short range wireless networks
- *'Cable free'* home theatre systems

UWB & Ku-band LNAs:

- Software radio type applications
- 1-18 GHz receiver with 800 MHz bands

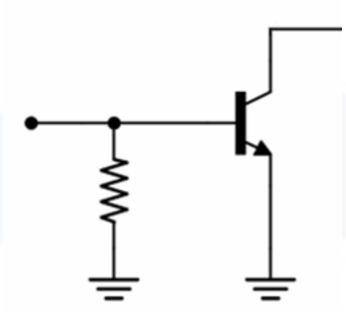
Ku-band SiGe BiCMOS LNA

Bandwidth	1 – 18 GHz
Gain	18 – 22 dB
NF	< 4 dB
P_{1dB}	-10 dBm

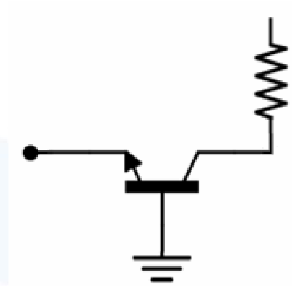
Parameter	**IBM 8HP**	**IBM 7WL**
β	600	140
f_T (peak)	200 GHz	60 GHz
r_b	20 Ω	20 Ω

Cadence Virtuoso
as design tool

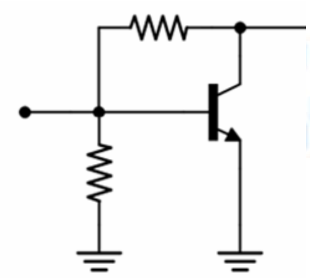
Current matching techniques



Resistive termination

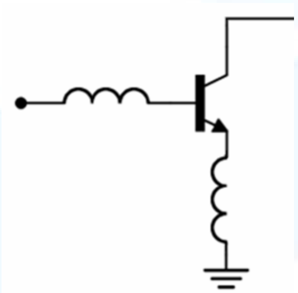


$1/g_m$ termination

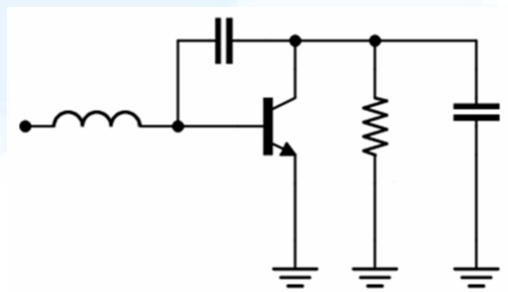


Resistive

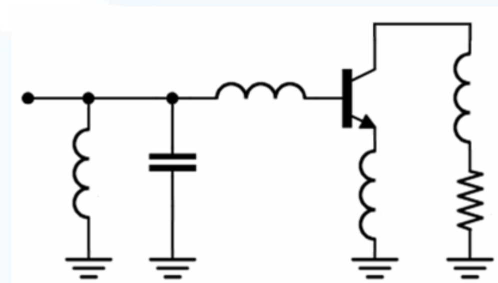
shunt-shunt feedback



Inductive degeneration



Capacitive shunt-shunt feedback



LC-ladder and inductive degeneration

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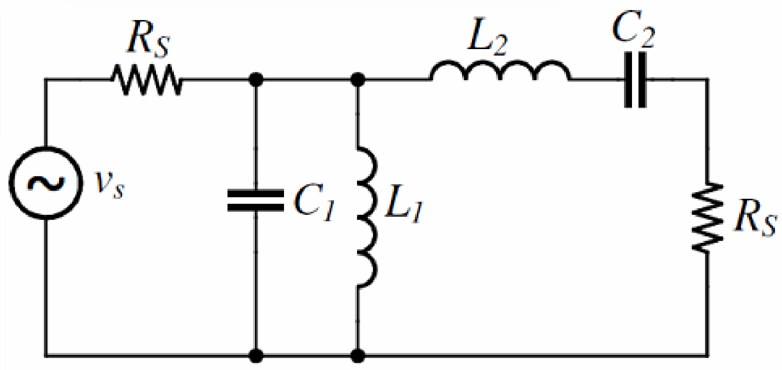
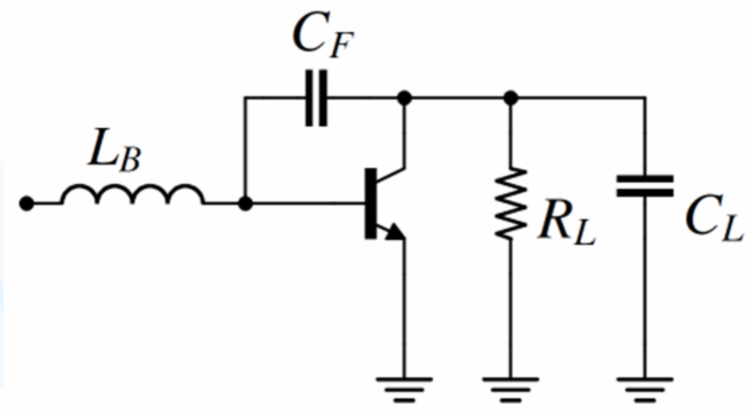
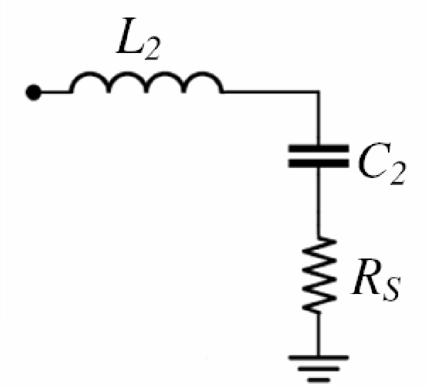
LC-ladder & capacitive feedback configuration





$$Z_M = \frac{1}{j\omega \underbrace{C_F\left(1+g_m R_L\right)}_{C_M}} + \underbrace{\frac{R_L}{1+g_m R_L}\left(1+\frac{C_L}{C_F}\right)}_{R_M} \Rightarrow$$



$$C_2 = C_\pi + C_M \qquad R_S = R_M\left(\frac{C_M}{C_M + C_\pi}\right)^2$$

Gain

Stage 1:

$$G_{M1} = g_m - j\omega C_{BC}$$

$$Z_{L1} = R_L \left\| \frac{1}{j\omega(C_{BC} + C_L)} \right. = \frac{R_L}{1 + j\omega R_L (C_{BC} + C_L)}$$

Stage 2:

$$A_{v,2} = j\omega L_3 g_{m2}$$

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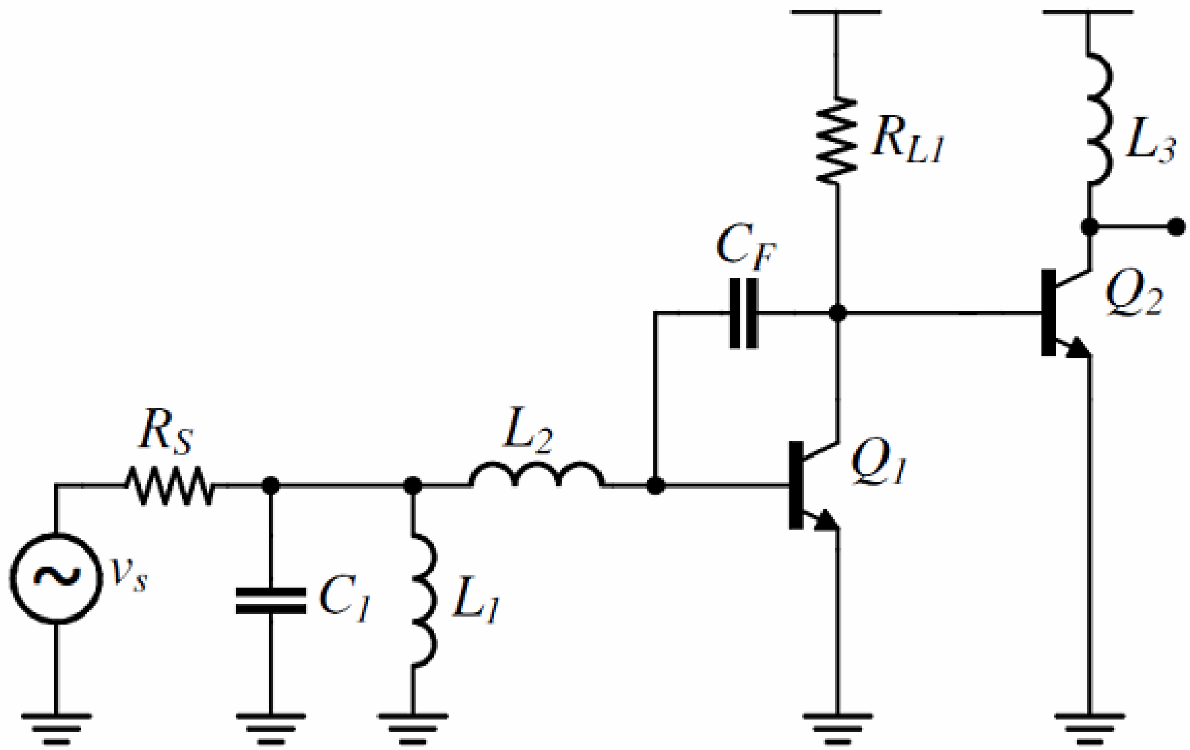
Proposed LNA schematic



Design equations

$$L_1 \approx \frac{R_S}{\omega_L} \qquad C_2 \approx \frac{1}{\omega_L R_S}$$

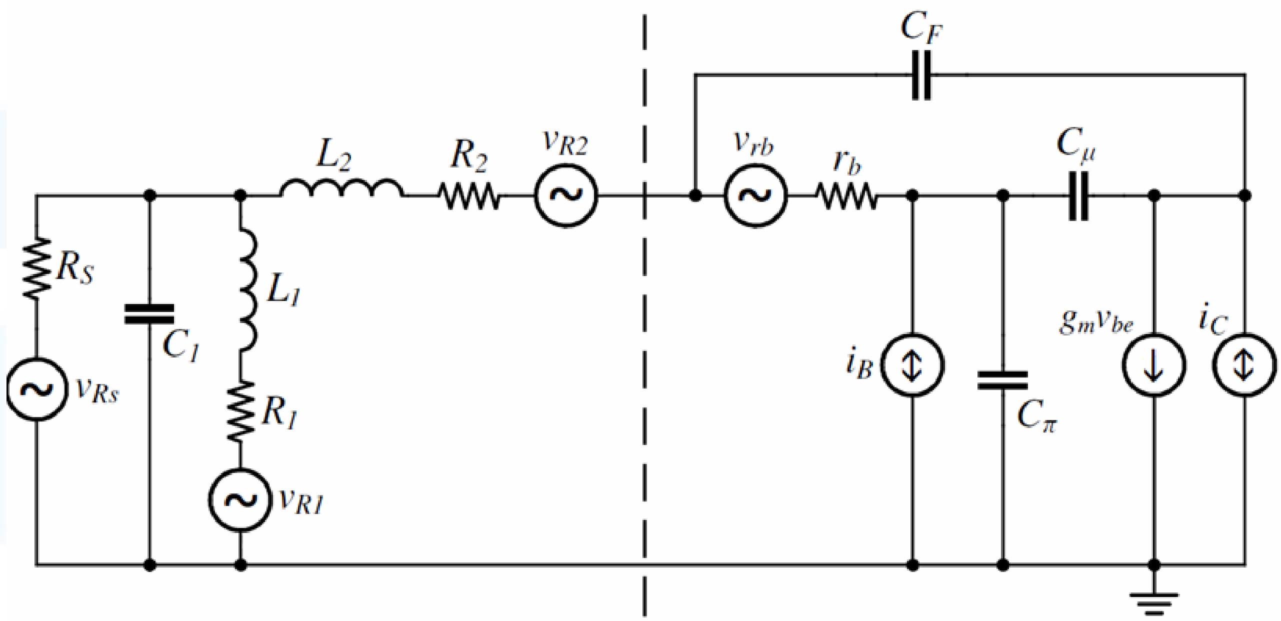
$$L_2 \approx \frac{R_S}{\omega_U} \qquad C_1 \approx \frac{1}{\omega_U R_S}$$

$$C_2 = C_\pi + (1 + g_m R_L)(C_\mu + C_F) \quad \Rightarrow \quad C_F = \frac{C_2 - C_{\pi 1}}{1 + A_{v1}} - C_{\mu 1}$$

$$R_S \approx \frac{1}{g_m}\left(1 + \frac{C_L}{C_{BC}}\right) \quad \Rightarrow \quad I_C \approx \left(1 + \frac{C_L}{C_{BC}}\right)\frac{V_T}{R_S}$$

$$\left[g_m R_L >> 1 \quad \text{and} \quad C_M >> C_\pi\right]$$

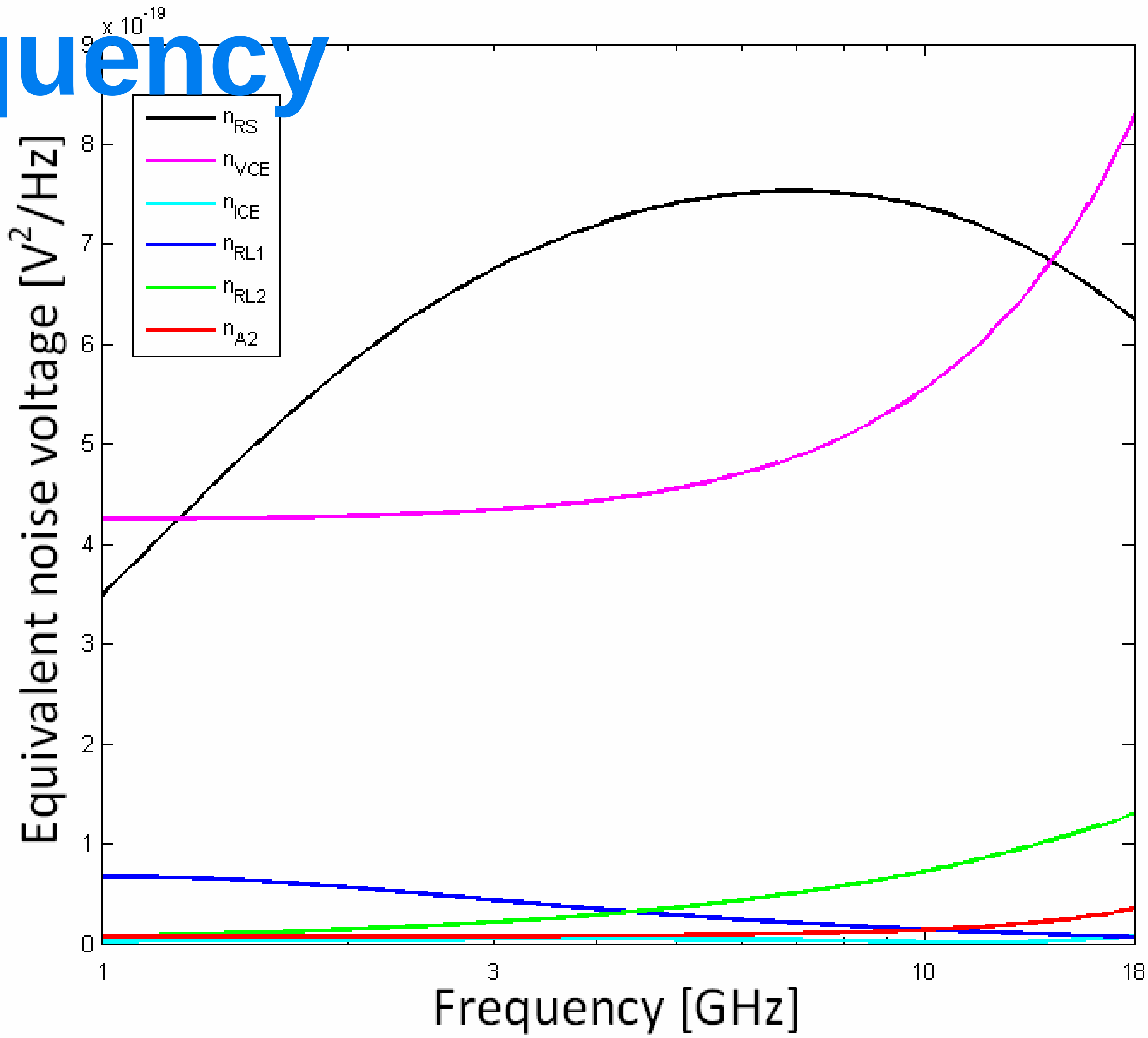
Noise figure



$$F_1 = \frac{\overline{v^2_{\pi,veq}} + \overline{v^2_{\pi,ieq}} + \overline{v^2_{\pi,R1}} + \overline{v^2_{\pi,R2}} + \overline{v^2_{\pi,RS}}}{\overline{v^2_{\pi,RS}}}$$

$$= \left[\left(\frac{1}{|Z_S|^2} + \left|1 + \frac{Z_2}{Z_S}\right|^2 \cdot |\omega C_F|^2\right)\overline{v^2_{CE}} + \left|1 + \frac{Z_2}{Z_S}\right|^2 \overline{i^2_{CE}} + \frac{1}{|Z_1|^2}\overline{v^2_{R1}} + \frac{1}{|Z_S|^2}\overline{v^2_{R2}} + \frac{1}{R_S^2}\overline{v^2_{RS}}\right] \cdot \frac{R_S^2}{\overline{v^2_{RS}}}$$

Noise contributions vs. frequency



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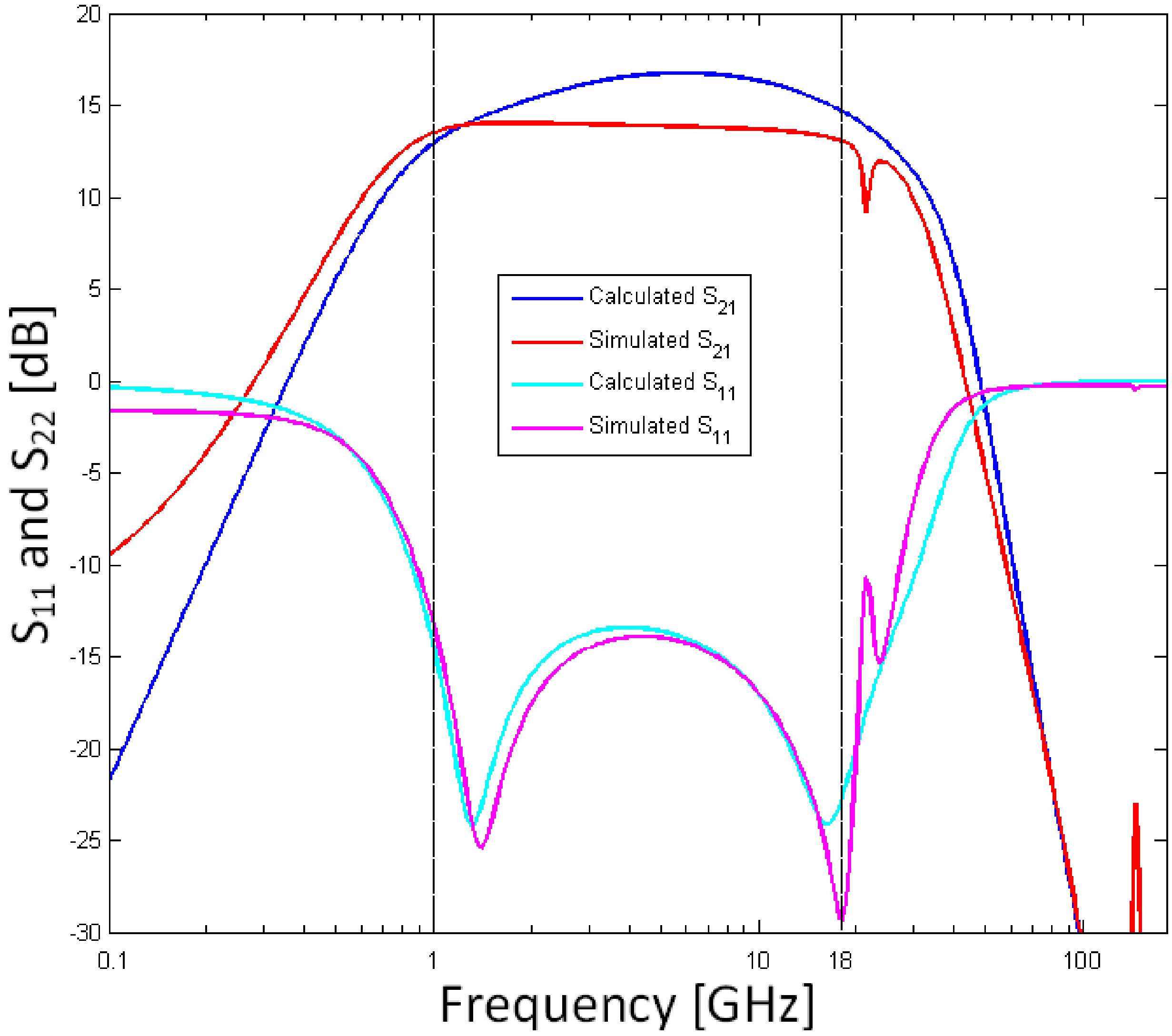
S_{11} and gain results



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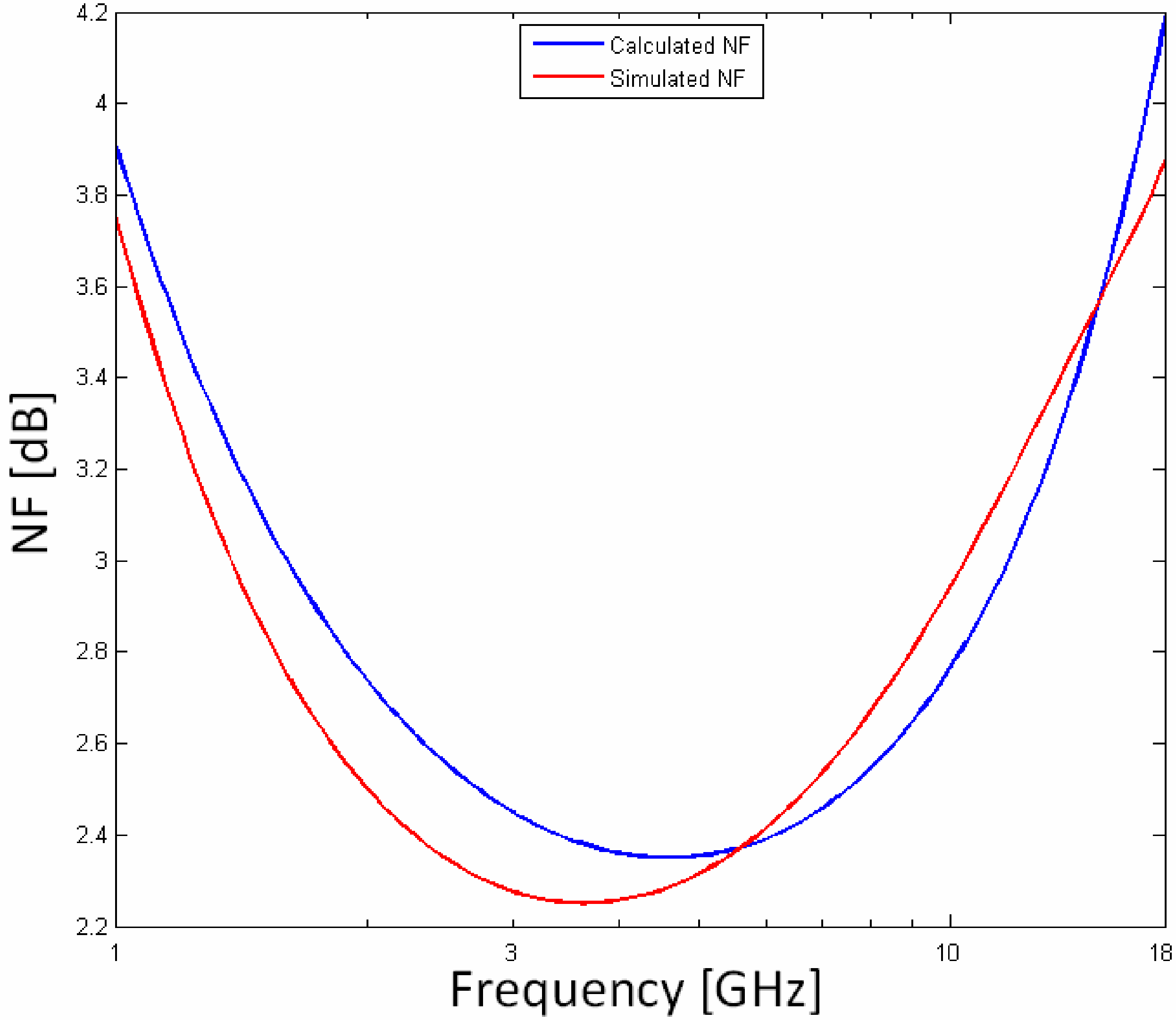
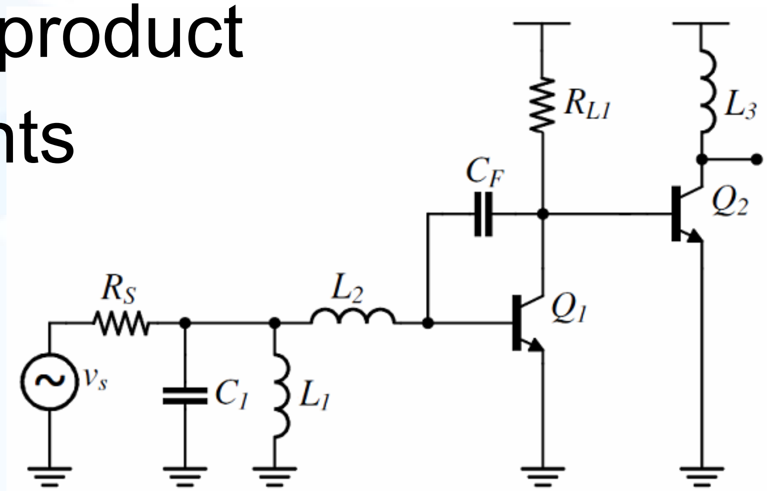
Noise figure results



Design at 60 GHz

Design limitations:

- Input impedance approximation
- Transistor gain-bandwidth product
- On-chip passive components

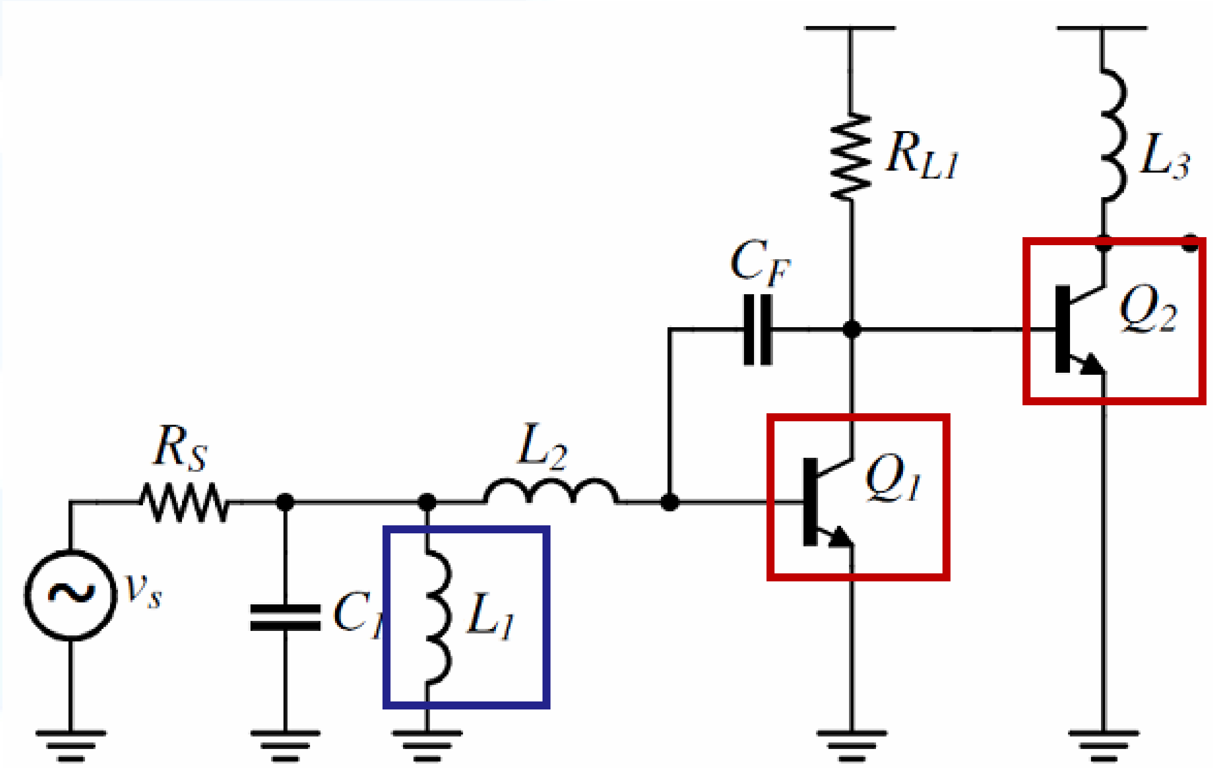


Performance trade-offs:

- NF vs. Bandwidth
- Parasitic capacitance vs. ω_L

Monte Carlo Analysis

Dominant Sensitive Components



Monte Carlo Analysis – S_{11} & S_{21}

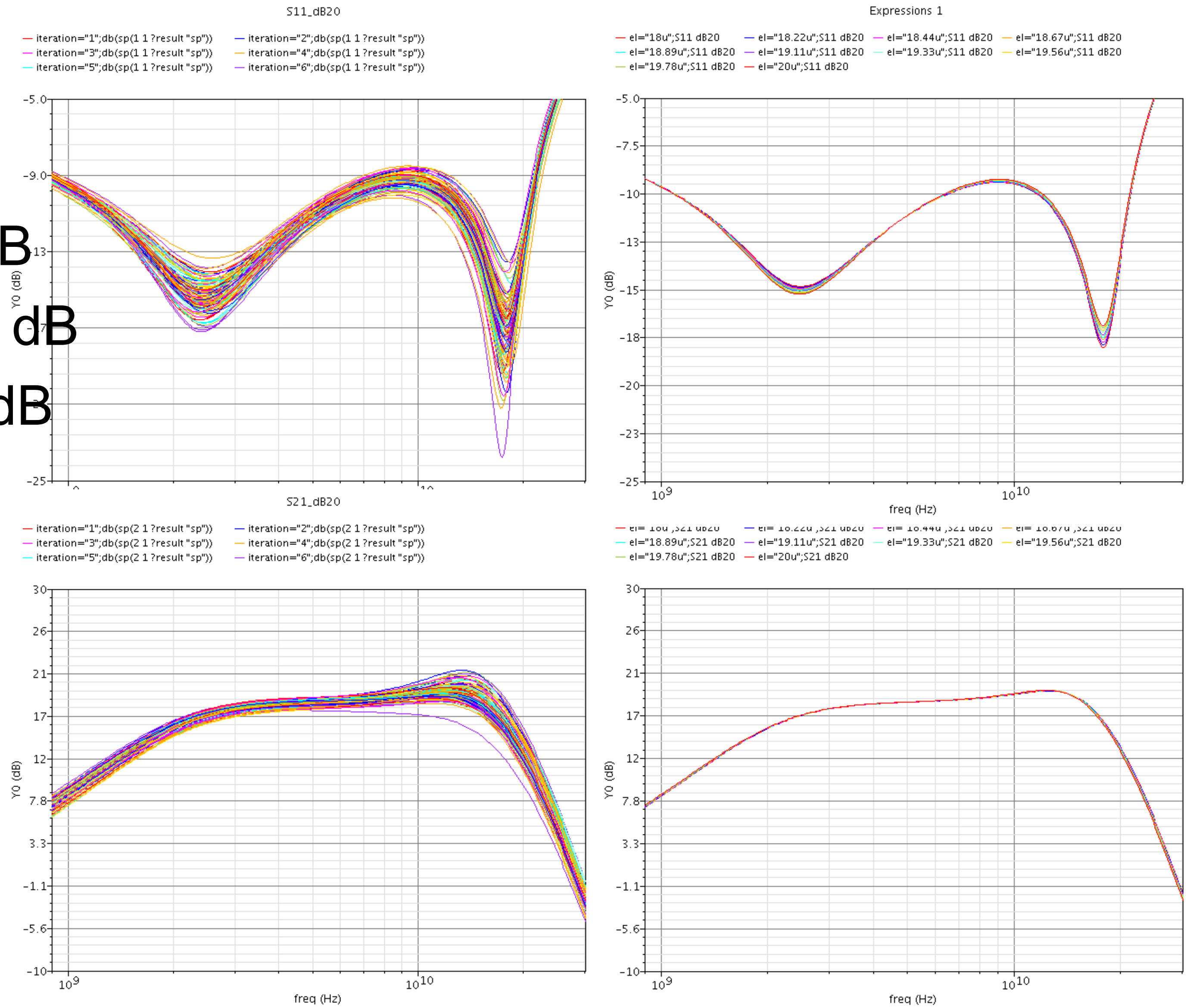
$\Delta S_{11@3GHz} \approx 3$ dB

$\Delta S_{11@3GHz} \approx 1.8$ dB

$\Delta S_{11@18GHz} \approx 7$ dB

$\Delta S_{21} \approx 1.2$ dB

$\Delta S_{21peak} \approx 3$ dB



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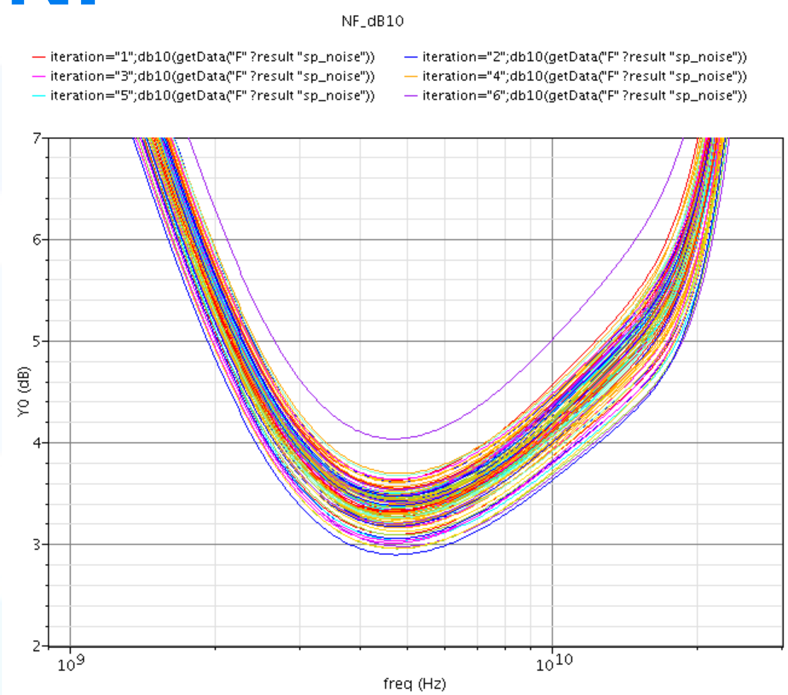
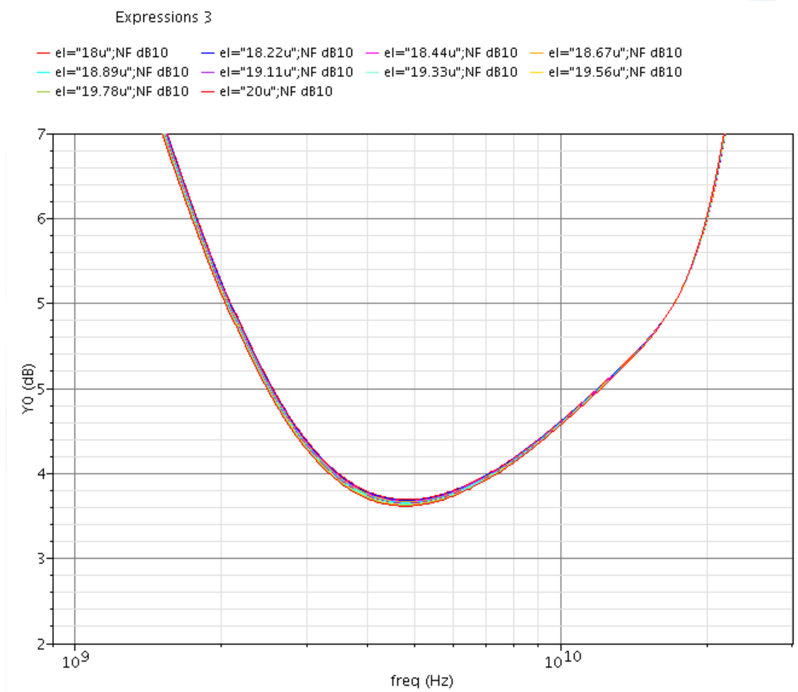
Monte Carlo Analysis – NF





ΔNF ≈ 1 dB

Future work

During internship at TU-Dresden:

Simulate using HICUM models and compare with well documented theoretical and simulation results thus far.

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[1] M. Weststrate and S. Sinha, "Analysis of a Low Noise Amplifier with LC-Ladder Matching and Capacitive Shunt-Shunt Feedback," *Proc. IEEE Africon 2009*, Nairobi, 23-25 September 2009.

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Feedback/Questions

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