Influence of Probe Tip Calibration on Measurement Accuracy of Small-Signal Parameters of Advanced BiCMOS HBTs

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***Abstract* — This paper presents investigation results of the probe-tip calibration impact on the BiCMOS HBT small-signal parameter measurement accuracy. Three popular calibration procedures were applied on the same data set and followed by the two-step de-embedding from the device dedicated Compete-Open and Complete-Short dummy elements. Experimental results showed that the observed difference in cold HBT parameters and parameters of passive devices was minimized by the de-embedding step. The f_T and f_{MAX} demonstrated higher sensitivity to the probe-tip calibration residual errors.**

***Index Terms* — Silicon-germanium HBT, silicon bipolar/BiCMOS process technology, calibration, bipolar modeling and simulation, S-Parameters, RF circuits, de-embedding.**

I. Introduction

With pushing device operation frequencies towards THz range [1], improving of conventional device characterization techniques becomes a crucial challenge. Today, RF device characterization uses the two steps approach:

1) probe-tip calibration (off-wafer) that is performed on a commercially available alumina calibration substrate and uses well characterized impedance standards (ISS);
2) de-embedding of the silicon backend parasitics using wafer-embedded test structures such as Open, Short, etc. (also called "dummies").

Each dummy is designed to represent a part (series or parallel) of the backend parasitic impedances. After measurement, these impedances are subtracted by a step-wise procedure yielding characteristics of the device under test (DUT).

A good understanding of possible sources of errors and potential room for improvement of each step are the key factors for increasing the accuracy of device characterization. In this work, we evaluate the impact of three popular probe-tip calibration procedures SOLT[1], LRM+[2], and multiline TRL[3] on some Figure of Merits (FoM) and parameters of an advanced BiCMOS HBT.

Si/SiGe:C HBTs offered in ST Microelectronics' BiCMOS9MW process technology feature a 130 nm emitter real width and a self-aligned double-polysilicon architecture with a selective epitaxial growth (SEG) of the base. The technology is based on a CMOS core process with a 6-level copper back-end for which the two highest layers are 3 µm thick. For the experiments in this paper, a 260/350 GHz f_T/f_{MAX} HBT called B3T was used [2].

Section II describes the calibration procedures that were evaluated and Section III presents the experimental setup and obtained results for some passive devices as well as for a test HBT under cold and hot (S-parameters) operation conditions. Chapter IV summarizes the observations and gives some practical recommendations for further accuracy improvement.

II. Probe Tip Calibration

For this work, we selected three calibration methods: SOLT, LRM+ and the multiline TRL (or mTRL). These methods have the widest variation from each other in:

1) systematic error models they are built on;
2) types of required calibration standards;
3) definition of calibration reference impedance Z_{REF};
4) sensitivity to standards non-ideality.

A. SOLT

The SOLT method is based on the 10-Term model of systematic measurement errors [3]. It requires three reflection standards at each VNA measurement port (highly-reflective elements, such as Open and Short, and the well matched 50 Ω Load) and one transmission standard Thru.

[1] Short-Open-Load-Thru

[2] Line-Reflect-Match, advanced

[3] Thru-Reflect-Line

Because required 10 error terms are calculated from only 10 measurements (six for reflection and four for the transmission standard), there is no information redundancy when solving the system of linear equations. Therefore, all electrical characteristics of standards must be fully known. As a result, the calibration accuracy critically depends on the fabrication and characterization of standards. It remains a challenge to achieve reliable SOLT calibration at high frequencies.

B. LRM+

This method is derived from the generalized calibration theory and it is based on the 7-Term error model [3]. It uses one transmission (the Thru) and two reflection elements: the Load, also called "Match", and the highly reflective Open or Short, also called "Reflect". Reflection standards are measured on each VNA ports. This combination leads to eight total measurements to be taken to find seven error terms. Due to this redundancy, the Reflect standards can be partly known and its reflection coefficient is a free parameter. This is an important advantage as the realization of a well-defined highly reflective element at the probe tip end is a very challenging task, especially at high measurement frequencies.

Any arbitrary impedance element can be used as the Load. The LRM+ method is capable to set the reference impedance Z_{REF} to 50 Ω as soon as the impedance of the Load standard Z_{LOAD} is known.

C. Multiline TRL

This method is based on the 7-Term error model. It was developed at NIST to solve the frequency limitation of the conventional TRL procedure [5]. Operating with many lines, it applies an extensive statistical analysis of the redundant information. In conjunction with the method proposed in [6], this procedure allows precise setting of the calibration reference impedance Z_{REF} to 50 Ω.

Because it relies on the measurement of sections of transmission lines and does not require any definition of the reflection standards impedance, the multiline TRL become the accuracy benchmark for comparing wafer-level calibrations.

III. Experimental Results

The experimental measurements were carried out on a broadband S-parameter measurement system from Cascade Microtech, consisting of a PM8 manual probe station, 100 micron pitch Infinity probes model SP-i110-A-GSG-03, ISS 104-783A calibration substrate, and equipped with the 110 GHz PNA network analyzer from Agilent Technologies. Also, to suppress a possible influence of higher order propagation modes and to reduce coupling effects especially at high measurement frequencies, we used the ceramic chuck add-on that carried the ISS and the test wafer.

The VNA instability over the experimental time (typically many hours) and the contact repeatability on aluminum pads can significantly impact the accuracy of any calibration comparison. Therefore, the measured data of the ISS standards, the de-embedding structures and the test transistor were acquired in raw format (with the S-parameter calibration turned off). The calibration and error correction were performed for the same data set outside of the VNA on a computer. We used WinCal®[4], MultiCal®[5], and proprietary IC-CAP®[6] script for this purpose, while device parameters were extracted using IC-CAP.

Also, it is important to note that due to their size, ($0.12 \times 14.86\ \mu m^2$) the selected test transistors required extremely low input power of about minus 40 dBm.

A. Verification of Passive Elements

The set of dummies included Pad-Open, Pad-Short, and Complete-Open and Complete-Short elements. The Pad-Open and the Pad-Short give the parasitic impedance of the contact pads and can be used in multi-step de-embedding method or for moving the measurement reference plane to the metal 6 level (Fig. 1). The pairs of Complete-Open and Complete-Short structures were designed for de-embedding of complete backend parasitics of a specific device geometry and are device dependent.

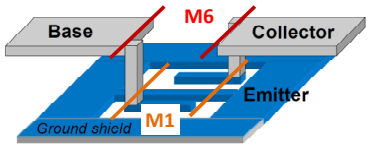

Fig. 1. Location of the measured reference plane after the de-embedding from Pad-Open and Pad-Short (M6) and Complete-Open and Complete-Short (M1).

The propagation constant γ and measured the characteristic impedance Z_0 of the ISS lines were extracted using the method from [6]. It resulted in a capacitance per unit length of C=1.481 pF/cm. The reference impedance of the multiline TRL was set back to 50 Ω and the measurement reference plane was move

[4] WinCal is a wafer-level calibration software package available from Cascade Microtech.
[5] MultiCal is available from NIST
[6] IC-CAP is a product of Agilent Technologies

closed to the probe tip ends. After that, the multiline TRL established well-defined calibration conditions and could be used as the accuracy benchmark.

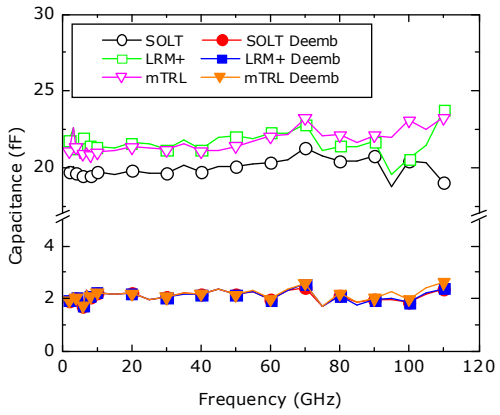

Fig. 2. Capacitance *C1* of the Complete-Open extracted with respect to different probe-tip calibrations as well as probe-tip calibration follow by the de-embedding from the Pad-Open. *C2* exhibits similar behavior.

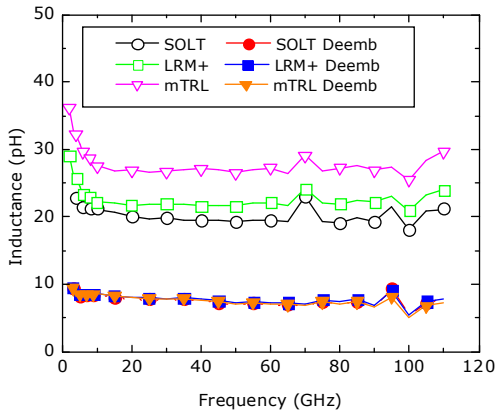

Fig. 3. Inductance *L1* of the Complete-Short extracted with respect to different probe-tip calibrations as well as probe-tip calibration follow by de-embedding from the Pad-Open and Pad-Short. *L2* exhibits similar behavior

Raw measurement data of all de-embedding elements were calibrated by the probe-tip SOLT, LRM+ and multiline TRL methods.

Assuming the Π-equivalent circuit for the Open and the T-equivalent circuit for the Short dummies, we extracted equivalent capacitances *C1*, *C2* and *C3* and inductances *L1*, *L2*, and *L3* for the Pad-Open, Pad-Short as well as for the Complete-Open and Complete-Short elements respectively. Table I summarizes the extracted results. *C3* and *L3* are negligible.

The capacitance of the Complete-Open varies from 19.7 fF to 22.3 fF and the inductance of the Complete-Short varies from 19.6 pH to 26.7 pH for SOLT and mTRL methods respectively. Results for the LRM+ are within these variation regions. Such a noticeable difference can be caused by residual calibration errors.

The de-embedded Complete-Open capacitances *C1* and *C2* are about 2 fF and the Complete-Short inductances *L1* and *L2* are about 7.5 pH for all methods (Fig 2, 3). Because de-embedding subtracts parameters, the major part of calibration residual errors is vanished.

TABLE I
EXTRACTED PARAMETERS OF DUMMY ELEMENTS

Parameter	**Probe Tip Calibration**		
	SOLT	LRM+	mTRL
Pad-Open			
C1, fF	17.5	19.4	19.1
C2, fF	17.5	19.3	20.3
Pad-Short			
L1, pH	11.5	13.4	19.0
L2, pH	11.8	13.7	19.3
Complete-Open			
C1, fF	19.7	21.6	21.3
C2, fF	19.6	21.4	22.3
Complete-Short			
L1, pH	19.6	21.9	26.7
L2, pH	19.4	21.3	26.3

B. Verification for a Transistor

As an active device, we measured S-parameters of a HBT having 14.86 µm length and 0.12 µm emitter stack width at different bias conditions: in a cold-S mode with V_B=-1 V…0.5 V, V_C=0 V and in hot-S (active) mode V_B=0.7 V…1 V and V_{CB}=0 V (emitter grounded in both cases). We extracted some key transistor characteristics: junction capacitances C_{BE} and C_{BC}, f_T and f_{MAX}. f_T was calculated at 20 GHz using a single spot frequency method. The f_{MAX} was defied with the Mason's gain. All results were de-embedded from the Complete-Open and Complete-Short dummies. Comparison of the extracted parameters is summarized in the Table II (Fig. 4, 5).

We found that the probe-tip calibration does not significantly influence de-embedded junction capacitances C_{BE} and C_{BC} up to 67 GHz.

TABLE II
EXTRACTED PARAMETERS OF TEST TRANSISTOR

Parameter	Probe Tip Calibration		
	SOLT	LRM+	mTRL
C_{BE}, fF (V_{BE}=V_{BC}=0V)	32.2	32.0	31.9
C_{BC}, fF (V_{BE}=V_{BC}=0V)	22.8	22.8	22.8
f_T, GHz (V_{BC}=0V, V_{BE}=0.89V)	236	238	238
f_{MAX}, GHz (V_{BC}=0V, V_{BE}=0.89V)	329	287	296

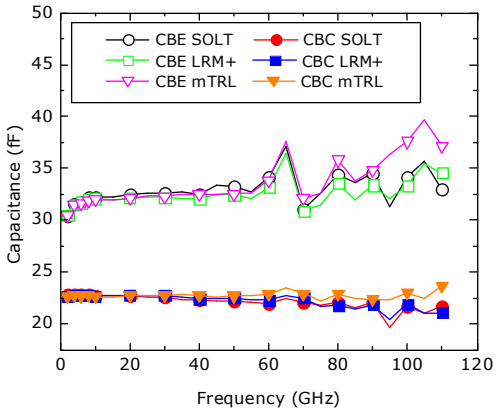

Fig. 4. Extracted junction capacitances C_{BE} and C_{BC} of a test HBT for V_C=0 V with respect to three probe-tip calibrations. Results are de-embedded from the Complete-Open and Complete-Short dummies.

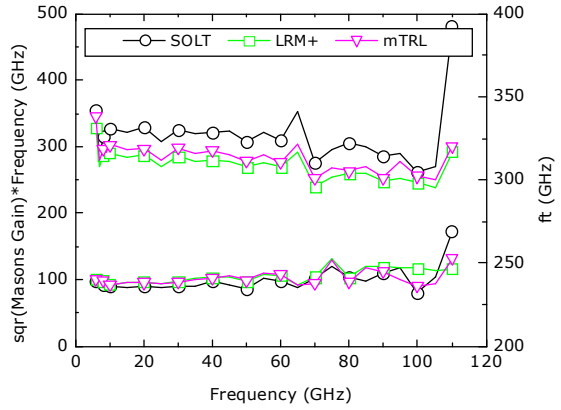

Fig. 5. f_{MAX} and f_T of a test transistor calculated at 20 GHz for different probe-tip calibration methods. Results are de-embedded from the Complete-Open and Complete-Short dummies.

The f_T is 238 GHz for both multiline TRL and LRM+, and it is 2 GHz lower for the SOLT. The f_{MAX} shows variation of about 42 GHz in total with highest value of 329 GHz for the SOLT, which might be overestimated. Further investigations are required to prove it.

IV. CONCLUSION

In this work, we investigated the impact of the probe-tip calibration on the measurement accuracy of advanced BiCMOS HBT small-signal parameters. We proved that for frequencies below 67 GHz, the accuracy is mainly defined by the de-embedding step. Due to low input power our results were affected by the noise at higher frequencies. This fact did not allow drawing a clear conclusion for this range.

It is important to note that the experimental setup had optimized measurement boundary conditions [7].

The obtained results showed that the further improvement steps should be focused on:

1) reducing the equivalent impedances of the silicon backend parasitics. This can be achieved by replacing the probe-tip (off-wafer) calibration with the in-situ (on-wafer) calibration step;
2) optimizing layout of the de-embedding structures.

Additional experiments undertaken on the dedicated W-band setup can further prove our statement for measurement frequencies above 67 GHz.

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