Designing On-Wafer Calibration Standards for Advanced High-Speed BiCMOS Technology

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***Abstract*— This work presents design methodology of on-wafer calibration standards covering frequencies up to 110 GHz and optimized for the BiCMOS processes. We discuss such topics as layout optimization of distributed and lumped standards, measurement and verification of electrical characteristics along with the definition of the on-wafer calibration reference impedance and measurement reference plane. Also, we present calibration verification results and some characteristics of an active DUT implemented in Si/SiGe:C ST Microelectronics' BiCMOS9MW process technology.**

I. Introduction

With further improvement of silicon RF device performance and increasing operation frequencies up to 110 GHz and beyond, the de-embedding of the device under test (DUT) from the influences of backend parasitics [1] has become a significant challenge. Alternative methods, such as the on-wafer calibration are required [2, 3].

Over the past years, substantial achievements have been made characterizing planar standards in processes with a conductive substrate (e.g. [4, 5]), establishing a solid background for accurate calibration on silicon. However, the design optimization is still a challenge, especially for measurement frequencies beyond 50 GHz.

In this work, we present the design of the test set that incorporates calibration standards and de-embedding structures for BiCMOS processes. The standards enable the distributed (such as multiline TRL[1], or mTRL for short) and the lumped-standard based calibration schemes (such as LRM+ [2] or similar). We discuss topics such as layout optimization, measurement and verification of the electrical characteristics of standards along with the definition of the on-wafer calibration reference impedance and measurement reference plane. The de-embedding dummy elements used are optimized to characterize residual parasitic impedances.

Also, we show calibration verification results for some figures of merit (FoM) of an active DUT implemented in Si/SiGe:C ST Microelectronics' BiCMOS9MW process technology featuring 130 nm emitter width and a self-aligned double-polysilicon architecture with a selective epitaxial growth (SEG) of the base [6].

II. DUT Launch and Test Structures

The customized on-wafer calibration and de-embedding set includes: three Lines of a different length, a Thru, a Pad Open, a Pad Short, a symmetrical Reflect, a serial Attenuator, Load, as well as DUT Open and DUT Short. All elements have a 100 micron pitch GSG pad.

A. Design the of RF Contact Pad

The structure of the RF pads consists of a metal 1 (M1) ground shield located between the substrate and the probe pads. The ground plane eliminates the losses in a resistive substrate. Also, it makes the parasitic of the signal pads purely capacitive and facilitates the de-embedding up to high frequencies. Transistors are laid out in the common collector configuration, i.e. the emitter and the substrate are shorted to the ground preventing high frequencies resonances.

In order to reduce the substrate effects, all transistors have a P+ guard-ring at a minimum distance of the N epitaxial well and it is connected to the ground shield. Signal pads consist only of the upper metal minimizing the parasitic pad capacitances to the ground (Fig. 1). The size of the pads is reduced to the smallest possible dimension.

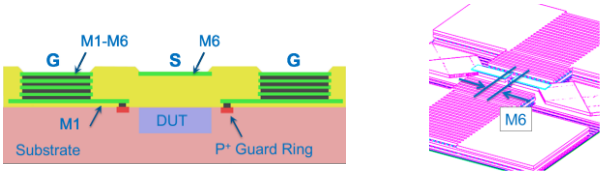

Fig. 1 Design of the DUT RF pad (a) and the location of the measurement plane at metal 6 level M6 (b).

[1] Thru-Reflect-Line
[2] Line-Reflect-Match, advanced

B. Calibration and De-Embedding Elements

The Thru and the Lines are designed as M1-shielded 50 Ω top metal grounded coplanar waveguide (CPW, Fig. 2, d). The effective length is: 51, 549, 1545, and 3039 µm respectively, covering the frequency range from 1 GHz to 110 GHz.

The Pad Open removes the parallel impedance contribution from the DUT measurements. It keeps the signal pads (drawn at the top metal only) and the ground pads (Fig. 2, a). A small piece of line remains to include the transition between the pad and the line.

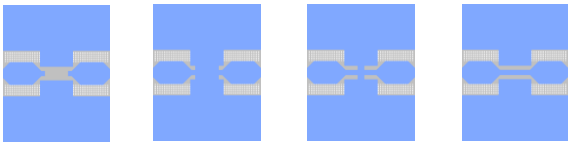

Fig. 2 De-embedding Pad Open (a) Pad Short (b) and calibration Reflect (c), and Thru (d) elements.

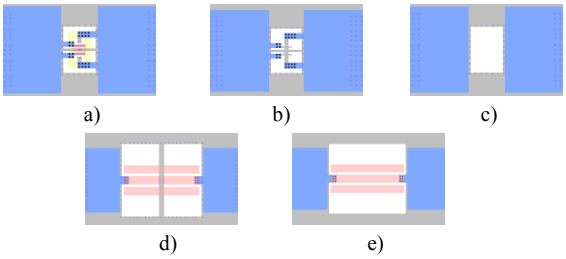

Fig. 3 Design of the DUT (a), the DUT Short (b), the DUT Open (c) the Load (d) and serial Attenuator (e) elements. The load has a single (per measurement port) 50 Ω N+ salicided poly resistor located at the M1 level. The picture shows the zoomed view of each element.

The Pad Short has a piece of top metal between the extremity of the pads and the closest ground metal stack (Fig. 2, b). The symmetrical Reflect is a CPW short located at the M1 level (Fig. 2, c). The Load is a single (per port) symmetrical 50 Ω N+ salicided poly resistor located at the M1 level (Fig. 3, d).

TABLE I
LOCATING THE REFERENCE PLANE

	Reference Plane		
	Probe Tip	**M6**	**M1**
ISS calibration	Straight	De-embedding: PAD OPEN, PAD SHORT	De-embedding: DUT OPEN DUT SHORT
On-wafer calibration	n/a	Straight	De-embedding: DUT OPEN DUT SHORT

The DUT Open is drawn removing the DUT and all metals used to connect it except the top metal (Fig. 1, 3, c). In the DUT Short dummy, the via stack between M6 and M1 is kept and all M1 terminals are shortened over the DUT (active DUT is removed, Fig. 3, b). The test chip also includes a symmetrical attenuator for calibration verification [2].

According to design of calibration elements, the measurement reference plane can be set to an arbitrary position at the top metal (M6) level (metal used for CPW layout) or close to transistor terminals M1 level (Fig. 1, 3, Table I).

III. CHARACTERIZATION OF STANDARDS

The experimental measurements were carried out on a broadband S-parameter measurement system from Cascade Microtech, consisting of a manual PM8 probe station, 100 micron pitch Infinity probes model SP-i110-A-GSG-03, ISS 104-783A calibration substrate, and equipped with the 110 GHz PNA network analyzer from Agilent Technologies. Also, to suppress a possible influence of higher order propagation modes and to reduce the probe-to-probe coupling especially at high measurement frequencies, we used the ceramic chuck add-on that carried the ISS and the test wafer.

The measured data of the ISS standards, the de-embedding structures and the test transistor were acquired in raw format (with the S-parameter calibration turned off). The calibration and error correction were performed for the same data set outside of the VNA on a computer. We used WinCal XE®[3], MultiCal®[4], and proprietary IC-CAP® script for this purpose, while device parameters were extracted using IC-CAP[5].

We measured the characteristic impedance of the ISS lines using the method from [7, 8]. The reference impedance of the ISS multiline TRL was set back to 50 Ω. After that, the ISS multiline TRL established benchmarking calibration conditions.

A. Extraction Line Parameters

The propagation constant γ as well as the characteristic impedance Z_0 of a CPW line are the parameters that are respectively required to shift the measurement reference plane to an arbitrary position and to transform the calibration results to the 50 Ω system reference impedance.

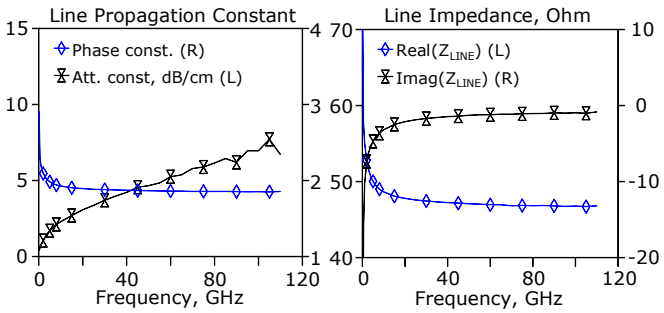

Fig. 4 The relative phase, the attenuation constants (left) and the characteristic impedance Z_0 (right) of the calibration Line.

We extracted γ and Z_0 of the Line using methods from [7, 8] (Fig. 4). The conventional lumped-load method results a capacitance per unit length of C=1.296 pF/cm.

[3] Commercially available from Cascade Microtech
[4] Available from NIST
[5] IC-CAP is a product of Agilent Technologies

B. *Extraction of the Load Reactance*

The load standard takes a crucial position when defining the reference impedance of a lumped-standard based calibration (such as LRM+). Load resistance should be measured since it is affected by fabrication process variability. The Load reactance is mainly represented by the equivalent reactance of the via stack (the distance between the plane M6 and M1, Fig. 1), as the on-wafer calibration already removes the backend parasitics.

Both probe-tip calibration extended by the Pad Open, Pad Short de-embedding and the on-wafer multiline TRL demonstrated good agreement for measured Load reactance (Fig. 5).

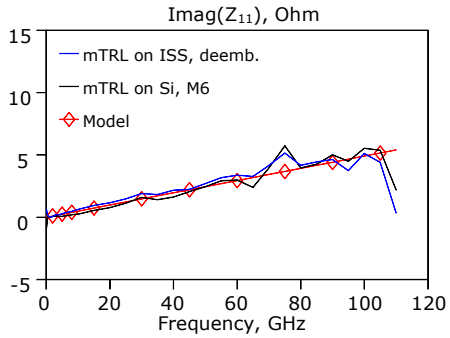

Fig. 5 On-chip Load reactance measured with respect to a probe-tip mTRL followed by the Open-Short de-embedding and the on-wafer mTRL.

C. *M6-M1 Parasitic Impedance Verification*

We used DUT Open and DUT Short dummy elements to verify the accuracy of the on-wafer calibration.

When the on-wafer calibration is applied, the majority of the contact pad and interconnect parasitics are calibrated out. As a result, the equivalent capacitances C1 and C2 of the DUT Open are decreased by a factor of ten and are nearly negligible: from 22 fF to less than 1 fF for C1 and to about 2 fF for C2.

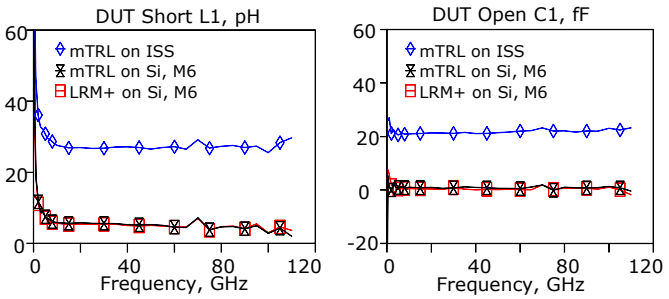

Fig. 6 The inductance L1 of the DUT Short dummy (left) and the capacitance C1 of the DUT Open dummy (right) extracted with respect to the probe-tip mTRL, on-wafer mTRL and on-wafer LRM+ calibration.

The equivalent inductances L1 and L2 of the DUT Short are decreased from 27 pH to 6 pH (Fig. 6).

IV. Verification for DUT

As an active device, we measured a HBT having 14.86 µm length and 0.12 µm emitter stack width: in a cold-S mode with VB=-1 V…0.5 V, VC=0 V and in hot-S (active) mode VB=0.7 V…1 V and VCB=0 V (emitter grounded in both cases).

We extracted some important FoM, such as CBC, CBE, f_T, and f_{MAX} (Fig. 7, 8). The reference plane of the on-wafer calibration was moved down to the DUT terminals (M1) using the DUT Open and the DUT Short.

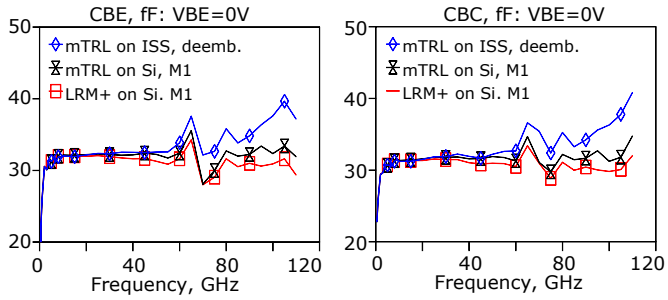

Fig. 7 CBE (left) and CBC (right) of the DUT extracted with respect to the probe-tip mTRL followed by the de-embedding, on-wafer mTRL and on-wafer LRM+ calibration.

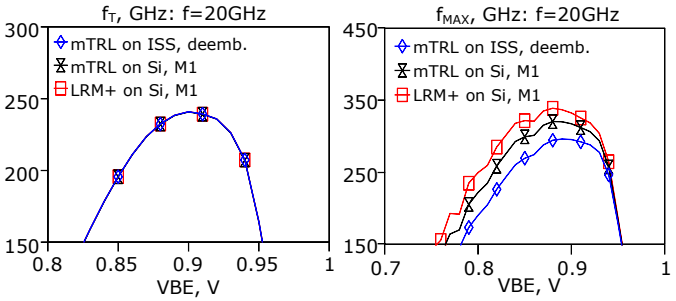

Fig. 8 f_T (left) and f_{MAX} (right) of the DUT extracted with respect to the probe-tip mTRL followed by the de-embedding, on-wafer mTRL and on-wafer LRM+ calibration (zoomed view).

Due to the low input power of -40 dBm, the measurement results are less accurate in the W-band. However, one can conclude that the extracted capacitances are closer to the expected value (less frequency dependent) above 40 GHz for on-wafer calibration schemes.

The on-wafer calibration demonstrated improvement for the f_{MAX}: from 296 GHz (for the reference calibration) up to 340 GHz for the on-wafer LRM+. The f_T did not show sensitivity to the calibration scheme and was close to 240 GHz for all methods.

V. Conclusion

This paper presented the test elements that enable both distributed- and lumped-standard based calibration methods for an advanced BiCMOS process. The standards are optimized to calibrate out the major part of the backend parasitics and to move the measurement reference plane close

to the DUT terminals in one step. Results proved that the on-wafer calibration is the preferable choice for accurate broadband device characterization.

We also showed that the load reactance can be characterized using a two-step de-embedding method. This significantly reduces the size of the test chip as the long calibration lines are not required.

ACKNOWLEDGMENT

We are thankful to Prof. Michael Schroter, Chair for Electron Devices, at Dresden University of Technology, as well as to Ralf Doerner from Ferdinand-Braun-Institut fuer Hoechstfrequenztechnik (FBH, Berlin) for providing characterization lab access. Cascade Microtech also acknowledges Agilent Technology EEsof division and Franz Sischka for supporting with IC-CAP.

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