An overview on the state-of-the-art of Carbon-based radio-frequency electronics

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Abstract - **Carbon-based electronics is still in its infancy, and its progress is presently still largely dominated by the natural science community. This paper provides an overview on Carbon-based electronics from an electrical engineering and RF analog applications point of view. Important material properties, resulting device structures, their fabrication and the most relevant modeling concepts are briefly reviewed. Furthermore, most recent results on device and circuit performance are presented in the context of practical requirements and applications.**

Index Terms - Carbon nanotube, graphene, RF transistors.

I Introduction

With the physical limits of incumbent semiconductor technologies built on materials such as Si approaching quickly, Carbon-based electronics have received increasing interest - so far mostly among the natural science community though - as potential candidate for extending the semiconductor roadmap. The first wave started with the discovery of the carbon nanotube (CNT) in 1991 [1], while the second wave was triggered in 2004 by the first realization of graphene [2]. The high interest in Carbon-based devices stems from the extraordinary electronic intrinsic material properties compared to existing semiconductors.

CNTs exhibit one-dimensional (1D) carrier transport which significantly reduces the scattering probability and, therefore, leads to a large mean free path, high current carrying capability, and low thermal noise. Employing CNTs as channels in a field-effect transistor (FET) has led to predictions of THz performance [3] due to the high carrier velocity (up to $8{\cdot}10^7$cm/s) and the very small quantum capacitance in a 1D conductor. Furthermore, a highly linear relation between drain current and gate-source voltage is expected for (near-) ballistic transport [4]. These features make CNTFETs very attractive for future RF applications such as amplifiers, mixers and switches. Extremely high mobilities have also been measured in graphene. Embedding a graphene layer as channel in a FET appears to be a natural extension of a MOSFET structure and of existing fabrication processes.

However, achieving the predicted performance and device features requires to overcome various technological obstacles related to material growth and overall device fabrication. Most recently, transit frequencies (f_T) as high as 300 GHz have been reported for a graphene FET (GFET) in [5]. However, such values are valid only for the *intrinsic* material, while the f_T of the actual device in [5] as required for practical circuit applications reduces to about 2.4 GHz for the complete device. Reports such as the one above have caused confusion among the RF circuit design community as to the actual application prospects of Carbon-based electronics.

This paper provides an overview on both CNT and graphene-based electronics from an electrical engineering and RF applications point of view. The relevant material properties, resulting device structures, their fabrication and the most relevant modeling concepts are covered to an extent that should give electrical engineers a feel for the actual status, challenges, and potential of these emerging technologies. Furthermore, most recent results on device and circuit performance are presented. For more detailed information, the reader is referred to the references and especially the literature therein.

II Material Properties

Graphene is a single-atomic layer Carbon (C) sheet as sketched in Fig. 1a. Fabricated samples showed a *low-field* mobility of up to $0.3...2.5{\cdot}10^4$ cm^2/Vs at room temperature [2, 6]. The often cited values of $2...2.5{\cdot}10^5$ cm^2/Vs were either estimated from just infrared transmission experiments on bulk graphene [8] or measured electrically on a suspended graphene sheet in vacuum at 5K [6] and thus do not apply to transistor structures. Such values, along with the idea of replacing silicon by graphene in the channel of a FET, are a major reason for the rapidly increasing research interest in this material and the associated funding allocations. However, measurements (and theoretical calculations) show that graphene does not have a bandgap (W_g) and hence behaves like a (quasi-) metal from a carrier transport point of view [2]. However, since the charge density is very low, it can be influenced to a certain extent by the voltages typically existing in a transistor or circuit (cf. Section VII). The *density of states* for a two-dimensional (2D) atomic sheet does not depend on energy and is given by $D_{2D} = 4\pi m^*/h^2$, with m^* as effective mass and h as Planck constant.

It is possible to open up a bandgap in graphene by (i) reducing the width of the sheet to a few nm, thus creating a narrow graphene nanoribbon (GNR) as shown in Fig. 1b, (ii) using a stack of graphene layers, (iii) layer strain, or (iv) applying a very large perpendicular electric field to bi-layer graphene. However, for instance, a field induced bandgap yields only about 14meV per 10^3kV/cm [7]), and compressive strain is predicted to increase the bandgap to about 0.3eV [9], while a range of 0.2...1.3eVnm/width is possible for narrow GNRs ([9], refs. in [10]) depending on the layer chirality. Multi-layer graphene can also have larger bandgaps but at the expense of significant reduction in mobility. Thus, from a circuit application point of view, the narrow GNR looks like the only viable method for creating a practically useful bandgap. The caveat of reducing the width though is that edge roughness effects (i.e. the C sheet chirality and type of the bindings at the edge) can cause the bandgap to vary widely [9] and even disappear. Furthermore, even in a suspended GNR the mo-

bility decreases rapidly with decreasing width due to scattering at the edge. The corresponding theoretical calculations have been confirmed by experiments (cf. section III).

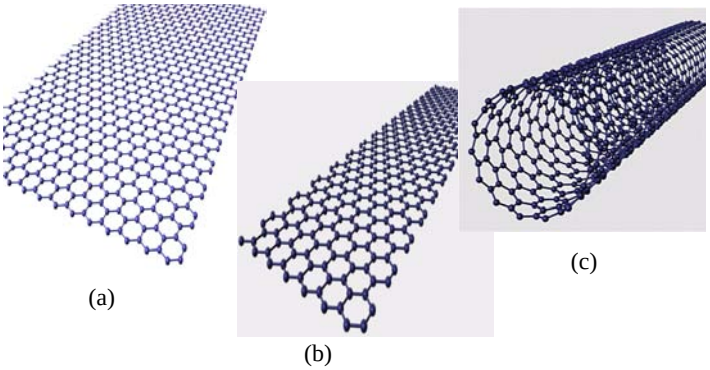

Fig. 1: Sketch of (a) graphene sheet, (b) graphene nanoribbon and (c) carbon nanotube.

Edge effect related scattering can be circumvented by rolling up a GNR into a CNT, which happens "naturally" under certain (process) conditions. This way, semiconducting CNTs with a bandgap of around 0.88eVnm/diameter can be obtained. Typical diameters are around 1.6nm, yielding a bandgap of 0.55eV which is suitable for transistor applications. However, as for GNRs, metallic behavior is observed in CNTs depending on the chirality. A more detailed analysis reveals that one out of three possible ways of rolling up a graphene sheet to a tube yields a metallic tube (e.g. [11]). At practically useful diameters, CNTs are basically one-dimensional (1D) conductors. The corresponding density of states depends on the energy level W and the ν^{th} subband conduction band edge $W_{C\nu}$:

$$D_{1D,\nu} = \frac{\sqrt{8m^*}}{h}\frac{1}{\sqrt{W - W_{C\nu}}}. \qquad (1)$$

Moreover, the double degeneracy of the CNT conduction band allows a twice as large carrier injection per voltage increment compared to graphene which only has a single degeneracy.

Carrier transport in CNTs occurs at the surface and in tube axis direction. Such 1D transport significantly reduces the scattering probability. Associated low-field mobilities at room temperature of up to about $8{\cdot}10^4$ cm^2/Vs have been measured [12], which corresponds to a mean free path of several hundred nm. 1D transport also is expected to lead to extremely low thermal noise and low self-heating. The current carrying capability of CNTs has been estimated to be up to 10^4 mA/µm^2 [13], which is orders of magnitude higher than in metals presently used by the semiconductor industry. This offers also the option of realizing CNT-based vias and interconnect with high reliability in future technologies (see [14] and refs. therein). Finally, CNTs have a very robust mechanical structure.

Common features of graphene and CNTs are (i) their susceptibility to adsoption of many other materials and (ii) the ambipolar electrical behavior. The former makes carbon-based electronics very suitable for sensor applications, while the latter is considered to be useful for reconfigurable circuits. Note that in both materials the mobility drops significantly at high fields due to optical phonon scattering. Detailed information on CNTs and related devices can be found in [15, 16].

III Device Structures

In research labs, G(NR)FETs and CNTFETs have often been realized without a top gate, i.e. the semiconductor (usually silicon) substrate acts as a backgate. While this minimizes the fabrication effort, it only allows DC characterization. For RF characterization and circuit applications, those structures are not useful for various reasons. Therefore, only transistors with top-gate will be considered here. Furthermore, structures with additional field electrodes for inducing a bandgap or a different conduction polarity (i.e. ambipolarity) have very high parasitic capacitances, making them unsuitable for RF applications, or require very large voltages, which are typically not available in high-speed integrated circuits.

Fig. 2a shows the schematic cross-section of a planar multi-tube CNTFET with a top gate. The CNTs are placed on an insulating substrate and directly connect the drain (D) and source (S) contact (as opposed to tube thin-films consisting of percolation networks). The middle region of the tubes can be electrically controlled by a gate (G) which is separated from the tubes by a thin gate oxide. The S/D contact metal covers or wraps around the CNTs, which are typically significantly longer than the S/D distance (i.e. the channel). Since the S/D metal typically forms a Schottky-contact with the tube, the regions between G and S/D (called S/D-G spacer) should be doped as highly as possible. However, the tube region underneath the G should be left intrinsic or only lightly doped for maximizing carrier modulation by the gate and minimizing scattering. In the CNT and graphene literature, doping is usually called functionalization, although the latter indicates a more generic chemical processing that not necessarily only leads to doping.

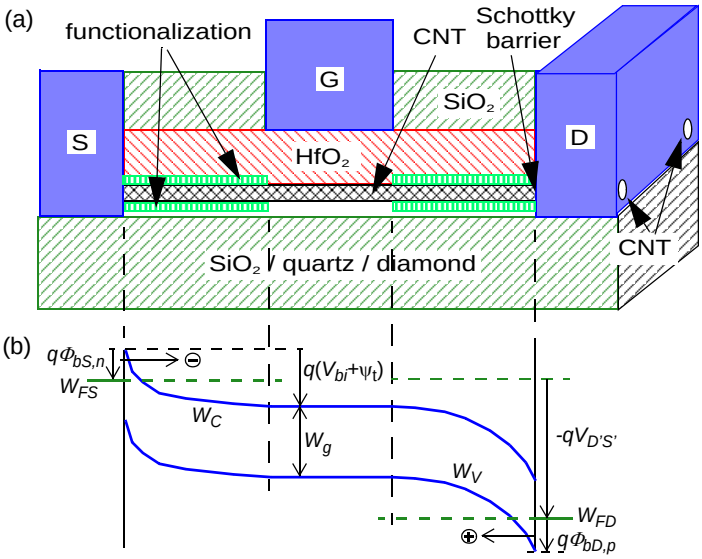

Fig. 2: (a) Schematic cross-section of a top-gate multi-tube CNTFET and (b) band diagram for $V_{DS} > V_{GS} > 0$. W_F is the Fermi level of the S or D contact reservoir. $V_{bi} = \Phi_{bS,n} - W_g/(2q)$ is the built-in voltage.

The device structure of a G(NR)FET is very similar to that of a SOI-MOSFET, except that a single or bi-layer graphene replaces

the silicon channel. In a GNRFET, the channel width becomes only a few nm. For HF applications, many ribbons need to be placed in parallel and the structure looks similar to that shown in Fig. 2a.

Embedding CNTs or a graphene layer within a transistor structure generally has a profound impact on physical parameters and electrical characteristics. Since CNTs and graphene possess only a single atomic layer, interfacing with other materials can change the bandgap and mobility as well as the Schottky barrier height and the charge density. This is due to the interactions (i.e. wave function overlap) between the materials at the interface.

At room temperature and in practically relevant FET structures where the graphene layer is sandwiched in between an oxide and bulk substrate, the mobility can drop significantly. While for wide (e.g. 1000nm) graphene layers still up to $10^4 cm^2/Vs$ have been reported, for narrow GNRs (e.g. 5nm and below) only about $200cm^2/Vs$ down to about $50cm^2/Vs$ were obtained (cf. Fig. 5b in [10] and references therein). Furthermore, in multilayer structures with 50nm wide GNRs a maximum mobility of only $460cm^2/Vs$ was reported recently [17] which is also not better than the values achieved in Si MOSFETs. These low values are due to edge related scattering. In terms of the mean free path, for graphene a value of about 300nm was reported in [18]. Therefore, when integrating a GNR in a transistor structure the resulting GNRFETs are expected to have a lower room temperature mobility than semiconducting CNTFETs (cf. Fig. 5a in [10]). Both GFETs and CNTFETs, however, allow a significant reduction of short-channel effects compared to MOSFETs.

IV Theoretical background

In general, the electron transport related drain current component of, e.g, a single-tube CNTFET can be calculated from the Landauer equation [19]

$$I_D = \frac{4q}{h}\int_{-\infty}^{\infty} T_n(W)[f_n(W, W_{FS}) - f_n(W, W_{FD})]\, dW, \qquad (2)$$

with f_n as the electron Fermi function and T_n (≤ 1) as the electron transmission factor between the bulk S and D contact, which generally includes tunneling through the Schottky-barriers and scattering along the tube. For an energy independent average transmission factor $T_{n,av}$ the remaining integral can be evaluated analytically, leading to the closed-form solution

$$I_D = T_{n,av} G_q V_T \left(ln\left[1 + exp\left(\frac{\psi_t^*}{V_T}\right)\right] - ln\left[1 + exp\left(\frac{\psi_t^* - V_{D'S'}}{V_T}\right)\right]\right) \qquad (3)$$

with he thermal voltage V_T, the quantum conductance (per tube)

$$G_q = 4q^2/h = 155\ \mu S, \qquad (4)$$

and $\psi_t^* = \psi_t - (W_{g1}/2q)$ where ψ_t is the tube surface potential and W_{g1} is the conduction band edge of the first subband.

Similar to MOSFETs and assuming the ideal case, i.e., (i) negligible impact of S and D contact as well as of functionalization and oxide charge on the electrostatic potential, and (ii) the same work function for CNT and gate material, the surface potential under the gate is related to the gate voltage through the charge balance,

$$Q_t' = C_{ox}'(V_{G'S'} - \psi_t) \qquad (5)$$

with Q_t' as tube charge and C_{ox}' as gate oxide capacitance per tube length. At sufficiently low carrier injection into the tube, Q_t' is very small and thus ψ_t closely follows the internal GS voltage $V_{G'S'}$. This bias regime is called quantum capacitance limited operation, since the very small tube capacitance C_t' (in series with C_{ox}') dominates the voltage drop and the input impedance.

For sufficiently large $V_{D'S'}$, the drain current above the threshold voltage V_{th} ($= W_{g1}/2q$ in the ideal case defined earlier) follows from (3) as

$$I_D = T_{n,av} G_q (\psi_t - V_{th}). \qquad (6)$$

Therefore, as long as ψ_t follows $V_{G'S'}$ (and $T_{n,av}$ does not depend on bias), I_D follows $V_{G'S'}$ linearly. A linear $I_D(V_{G'S'})$ relation can also be obtained in GNRFETs once one-dimensional transport is achieved by sufficiently narrow nanoribbons in the channel.

It is this linearity combined with high current carrying capability, low self-heating and high (structural) ruggedness that makes CNTFETs very interesting for analog RF electronic applications. However, as (6) and (4) show, the lowest achievable impedance of a single tube is the quantum resistance $R_q = 1/G_q = 6.45k\Omega$ (assuming $T_{n,av} = 1$). In addition, the maximum current that can be delivered by a single tube is at best in the tens of μA range. This makes single-tube transistors unsuitable for RF applications, where typically load impedances in the range of 50Ω and output powers in the mW range are required. The same argument applies to single ribbon GNRFETs. Therefore, many tubes (or ribbons) need to be connected in parallel, leading to multi-tube (MT) or multi-ribbon (MR) FETs, which can be scaled towards the desired specifications.

V Fabrication

As is typical for an emerging technology, CNTFETs are still mostly fabricated in research labs, but there are already a few companies trying to develop production-type processes for different markets. Also, companies exist that sell semiconducting CNTs (s-tubes), e.g., in solutions, in which the metallic tubes (m-tubes) have been mostly eliminated through a special "sorting" process. The fabrication method usually found in research labs consists of dispersing such a solution on a 2" wafer or an even smaller die (e.g. [20]) and then placing the S/D contacts and, if desired, the top gate with E-beam lithography. The advantages of this process are a very high ratio of s- to m-tubes and small dimensions. The disadvantage though is that intentional and wafer-scale device placement and hence circuit fabrication are not possible. This initially widely used and reported fabrication has fueled the perception that deliberate placement of CNTFETs is impossible. While this is still true for single-tube FETs it is not for MT FETs. As a consequence, the main focus for developing a production-type CNTFET technology should be on analog and RF MT FETs rather than on digital single-tube FETs.

A more attractive and increasingly found method is to grow CNTs from a catalyst directly on a wafer using a (special) CVD furnace. Various substrate materials have been used, with the most popular ones being quartz (i.e. a quartz wafer) and SiO_2 on a silicon substrate. On quartz the interaction between C atoms and the substrate during tube growth produces nicely aligned

CNT arrays [21]. However, comparing the electrical results in [22] with those in [25] it seems that the same interaction also reduces the carrier mobility by about a factor 3 to 5 compared to SiO_2. Hence, nanotube arrays grown on quartz have been transferred to SiO_2 on a silicon wafer [23]. It is questionable though whether this process is suitable for wafer-scale production.

The alternative is to use a photostepper and a silicon wafer with thick SiO_2 for electrical isolation. This way, the catalyst and thus the tubes can be placed intentionally, allowing to arrange CNTFETs with different sizes and layouts anywhere on a chip. For instance, the present process at RFNano [25], requires just three masks for building the transistor structure itself. After catalyst deposition (mask 1) on a thick oxide layer, the CNTs are grown at around 900C. With the second mask, S and D electrodes are placed on the catalyst lines. After gate oxide growth, the gate is defined by the third mask. Next the inter-dielectric isolation layer is grown and opened with the fourth mask for the vias to M1. Finally, the fifth mask defines the M1 contacts and pads. This process flow readily allows to integrate RF passive devices and to design test masks the same way as for conventional technologies. Existing test chips contain over 200 different device structures and sizes (including single-tube devices) per die on a 4" wafer with about 190 dies [25]. A three week cycle time has led to the capability of fabricating millions of CNTFETs per month and tremendous acceleration of process development.

Growing CNTs on SiO_2 unfortunately yields randomly aligned arrays and metallic tubes (s:m = 2 statistically). The s:m ratio though depends on, e.g., catalyst size and C feeding rate [21]. Generally, a compromise for the various growth conditions is required for achieving a high number of tubes per gate width (i.e. tube density), a high s:m ratio, and sufficiently long tubes to bridge the channel. Other inexpensive and wafer-scale options for eliminating m-tubes include, e.g., post-growth etching and chemical decoration making m-tubes less or not conducting [21]. One often cited option is to electrically burn m-tubes by self-heating [24]. However, this method usually leads to just an open tube with the stubs still connected to S/D and thus contributing to the capacitance and possibly also causing Schottky-barriers when crossing s-tubes in the channel. Also, the method is difficult to apply across wafer and especially in circuits.

Fig. 3 shows an example of a MT CNTFET with 20 gate fingers of 0.15µm length and 40µm width. The S-D distance is 0.8µm. The random network of tubes resulting from the growth on SiO_2 is visible underneath the fingers. The drain current is carried by those tubes that cross S and D directly (rather than through tube-tube junctions). The relaxed dimensions are a consequence of the fact that for an emerging technology like this one, investment for production-type equipment (such as lithography) is still limited. The typical tube density in CNTFETs differs significantly depending on the growth process and substrate. For quartz, tube densities well above 15/µm have been achieved [22], while for dispersion or growth on SiO_2 the density is usually significantly below of 10/µm.

Graphene is grown with reasonable uniformity (i.e. single, bi- or multi-layer) across 2" or 3" wafers (e.g. SiC, diamond) [26]. Processing temperatures range from 900 to 1450C [27]. A two-finger top-gate structure as shown in Fig. 4 [26] is widely used for HF applications. In [5], the fabrication of a self-aligned GFET was reported, using a Co_2Si nanowire as gate and Pt coverage of the S/D-G spacer region in order to provide a low-ohmic access and to eliminate the Schottky barrier at the S/D contact.

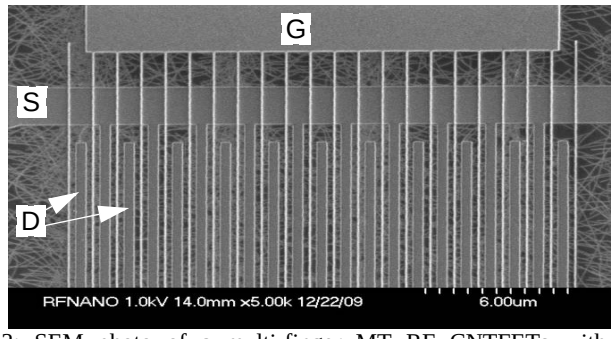

Fig. 3: SEM photo of a multi-finger MT RF CNTFETs with the underlying nanotubes visible. Note that the SEM enhances the visibility of the tubes by about a factor of 100. Courtesy RFNano Corp.

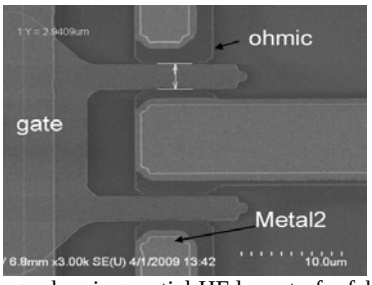

Fig. 4: SEM image showing partial HF layout of a fabricated two-finger GFET [26].

An often arising question about CNTFET technology is device uniformity and yield. These attributes are difficult to evaluate for E-beam processes or those on small dies or 2" wafers since there are just not enough devices fabricated. However, since CNTs at RFNano have been grown simultaneously across two 4" wafers, i.e. across a diameter of 8", and the previously described stepper process produces a sufficient number of dies, across-wafer uniformity and yield can be evaluated. The example for the peak transconductance in Fig. 5 shows a quite reasonable uniformity (around 11mS), considering the development in a university cleanroom and that this is still an emerging technology. These results are similar to those of earlier lots that were published in [25] also for f_T and f_{max} as well as in [28] for the maximum available power gain.

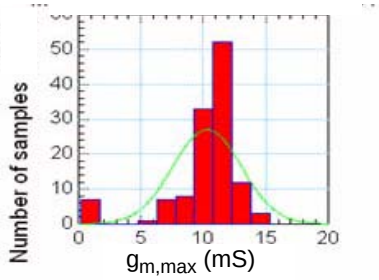

Fig. 5: Distribution of the maximum transconductance of a 20 finger 0.4x20µm^2 CNTFET measured across a 4" wafer.

Raman spectroscopy suggests the majority of the CNTs have diameters around 1.6 to 1.8nm. Electrical measurements on single tube test structures seem to indicate some fraction of multi-wall tubes, but the results are inconclusive so far. CNT growth over many wafers (usually 12 per lot) at RFnano using fixed growth recipes typically yields tube density variations in the order of 20%. In those lots the variation in the s:m ratio is much smaller though than 20%.

Fabrication of sufficiently narrow nanoribbons using conventional lithography is extremely costly and unreliable in terms of variations in width, edge roughness, and density. Alternatives such as bottom-up methods are still far from from being suitable for production. Therefore, the uniformity of narrow GNR fabrication is unknown yet.

Finally, substrate transfer of graphene layers or CNT arrays may look attractive at first glance but remains questionable from an industrial production point of view in terms of throughput and process variability. For instance, substrate transfer very likely introduces contamination of the graphene layer or the CNTs, which will cause hysteresis and uncontrollable threshold voltage variations.

VI Device Modeling

Current wafer-level technologies do not contain intentional doping of the spacers due to temperature stability issues of existing (mostly organic) dopant materials. Hence, Schottky barriers at the metal-CNT or -graphene interface and related tunneling currents impact the device behavior significantly [29]. In addition various experiments suggest that the device behavior is influenced by additional quantum phenomena. Even though the mean-free-path in CNTs is quite long, phonon scattering within the channel is not negligible in actual devices of moderate lengths [30]. Thus, distinguishing and quantifying the various contributions calls for adequate modeling and simulation capabilities. Depending on the channel length and on the phenomena of interest, several modeling approaches have been proposed such as ab-initio, effective-mass and semi-classical simulation. While first principles simulations [31] are ideally suited for material specific analysis of, e.g., the metal-CNT contact and ultra-short channels, the Schrödinger equation (SE) [32, 33] and semi-classical approach [34] along with a simplified metal-CNT interface description are more suitable for device simulation, although the SE-Poisson approach is still limited to about 100nm channel length. A serious difficulty is also the calibration of physical models to measurements, since hysteresis and the high-impedance of single tubes prevent the acquisition of consistent DC and AC data.

For circuit design, compact models are required. Although quite a number of models have been published (for a review see [35]), only very few are suitable for *RF analog* design. Of those, most are for single tube FETs only and use theoretical expressions for the tube charge without properly or at all considering scattering and the impact of the Schottky barriers.

A large-signal geometry scalable model for MT CNTFETs, which has been implemented in Verilog-A and has already been employed successfully for RF analog design (e.g. [36]) is shown in Fig. 6. The inner shell consists of two parallel networks representing the nonlinear behavior of the s- and m-tubes. The average transfer current I_T and charge portions Q_{ts}, Q_{td} of the s-tubes are modeled by smooth and nonlinear functions of both GS and DS voltage of the internal s-tube transistor, indicated by the primed nodes, while the average current through the m-tubes is a nonlinear function of the voltage between nodes D_m and S_m. A bias independent capacitance is assumed for the m-tubes. Since the integral in (2) cannot be eveluated in closed-form, an empirical analytical expression is used for describing I_T. A separate contact resistance $R_{c...}$ is included for the s- and the m-tube path, since the current through these resistances is different. The outer shell of the equivalent circuit contains the parasitic resistances and capacitances from the metallization, including fingers, vias, and connections. Excellent agreement with experimental results has been obtained for this compact model (cf. sect. VII, [25, 28]).

G(NR)FETs are typically represented by a MOSFET equivalent circuit with the equations adapted to the physics in the graphene channel.

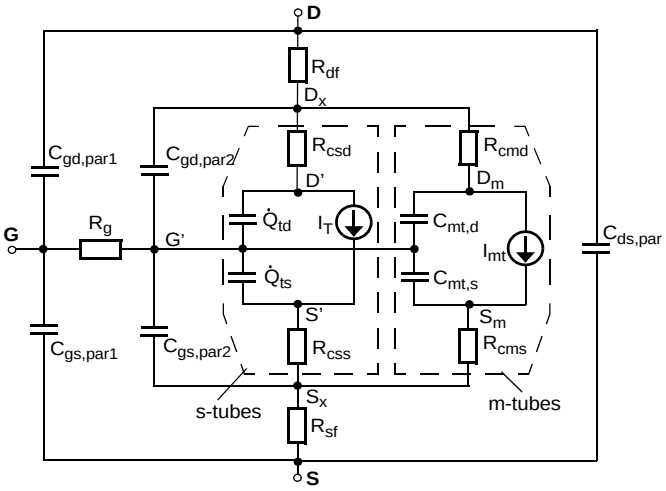

Fig. 6: Large-signal MT CNTFET equivalent circuit, including s-tubes, m-tubes, and parasitic elements. Nodes G', S', D' represent the internal s-tube transistor. Self-heating and hysteresis adjunct networks also exist but are not shown here.

VII Experimental Results

As already discussed, only MT CNTFETs and larger (or MR) G(NR)FETs are relevant for practical RF applications. For such devices, in the corresponding research literature very high transit frequencies have been reported, with f_T values up to, e.g., 80 GHz for a $2*0.3*10\mu m^2$ CNTFET [20] and, e.g., 300 GHz for a $0.144*3.7\mu m^2$ GFET [5]. Such results have led to confusing perceptions among the RF community regarding the practical suitability of these technologies for circuit design, and hence require an explanation that is typically not given in research papers. The key to understanding the meaning of the reported transit frequencies is the deembedding of parasitics.

In incumbent technologies, it is standard to report "extrinsic" RF transistor figures of merit obtained from pad-deembedded S-parameter measurements. Thus, the corresponding figures of merit still include all metal interconnect related parasitics that are required for transistor operation and connection in a circuit. Unfortunately, in the CNT and graphene community it has become

widespread practice to report "intrinsic" RF figures of merit, in particular the cut-off frequencies. These are obtained after deembedding not only the pads but also the complete interconnect metallization that connects to the tubes or graphene layer. As a consequence, the reported values are valid only for the intrinsic graphene or CNT material (if at all, see below) but are absolutely useless for circuit design purposes. It is also very important to assess the accuracy of the reported intrinsic cut-off frequencies. For example, in [5] an intrinsic transit frequency of 300 GHz is reported for a GET, while the corresponding extrinsic value is just 2.4GHz. In other words, about 99% of the total capacitance has been "deembedded". It is well-known in the RF community that with such large dominating parasitic capacitances deembedding is extremely error prone; i.e. the reported intrinsic frequency value is likely to have a large error. Therefore, only *extrinsic* HF results are shown in this paper.

Typical transfer and output characteristics of a state-of-the-art MT CNTFET with 8 gate fingers of 0.4µm length and 50µm width are shown in Fig. 7. At negative voltages, the drain current remains at a non-zero minimum value (off-current) which is caused by the m-tubes. Above a certain (negative) threshold voltage the s-tubes turn on and I_D increases. However, instead of the expected linear increase the curves start bending towards a saturation value which, assuming an s:m ratio of two, is also smaller than the expected factor three of the minimum value. The curve bending is likely due to scattering along the tubes, since they are in average even longer than the S to D distance of 0.8µm, and since the spacers are not intentionally doped and thus do not reduce the impact of the Schottky barrier. The saturation below the expected maximum I_D value at high V_{GS} is believed to be caused by hysteresis and the Schottky-barriers as well as by self-heating at the contacts and along the (m-) tubes. Towards far negative GS voltages, I_D increases due to ambipolar conduction.

The impact of m-tubes can also be seen clearly in the output characteristics (cf. Fig. 7b). The lowest curve represents the conductivity of just the m-tubes, since they determine the smallest achievable output conductance of the transistor. The curve does not increase linearly with V_{DS} due to scattering, and its conductance is superimposed on that of the s-tubes, when they are turned on. Scattering, self-heating, and hysteresis (in s-tubes only) cause the drain current to saturate at high V_{DS} values. In addition, the random tube alignment leads to crossings. Especially the crossing of a m-tube over a s-tube creates a Schottky "point" contact. According to simulations, the associated potential barrier on the s-tube has a detrimental effect on its current, if the crossing is located within the G-S spacer or the gate region.

Today's best MT CNTFETs exhibit an extrinsic transit frequency of around 10 GHz [25] rather than the often cited 80GHz [20]. The latter is again the *intrinsic* value, while the *extrinsic* value is only about 11 GHz for a 2*0.3*10µm^2 device built from solution dispersion. Typical f_T characteristics are shown in Fig. 8a. A rather peaky behavior can be observed similar to existing FET technologies. Also, increasing V_{DS} leads to increasing f_T values. The shape of f_T is very similar to that of g_m, indicating a fairly bias independent input capacitance. The latter consists mostly of contributions from m-tubes and parasitics, possibly masking a bias dependence of the s-tubes. This CNTFET exhibits a maximum available small-signal power gain of 16dB at 0.5 GHz (cf. Fig. 8b) which, along with 14dB power gain at 1GHz [25], is among the best values ever achieved for Carbon-based devices.

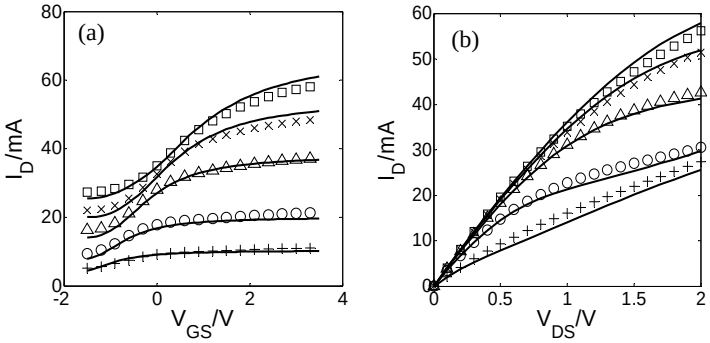

Fig. 7: (a) Transfer characteristics (V_{DS}/V = 0.25, 0.5, 1, 1.5, 2)) and (b) output characteristics (V_{GS}/V = -1.5, -0.5, 0.5, 1.5, 2.5) of a 8*0.4*50µm^2 MT CNTFET. Courtesy RFNano Corp.

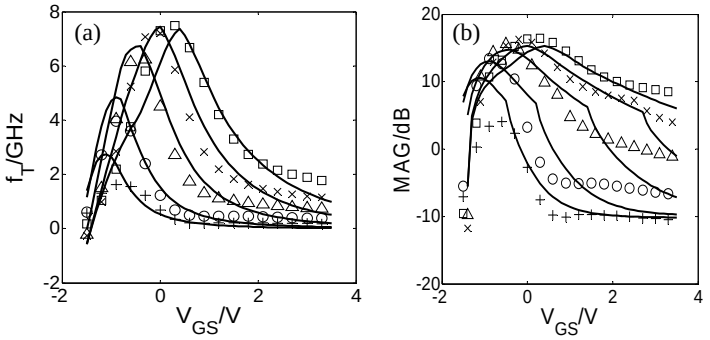

Fig. 8: (a) Transit frequency (V_{DS}/V = 0.25, 0.5, 1, 1.5, 2) and (b) corresponding maximum available power gain (at 0.5GHz) of an 8*0.4*50µm^2 MT CNTFET. Courtesy RFNano Corp.

DC characteristics of state-of-the-art GFETs are shown in Fig. 9 for a two-finger transistor with a gate length of 550nm and 40nm, respectively, and a width of 15nm [37]. The output and transfer characteristics of the long-channel device look similar to those of the CNTFET in Fig. 7. The large off-current is due to the metallic nature of the graphene layer. The on-off ratio is slightly larger than 2. However, the short channel (40nm) device reaches only an on-off ratio of only about 1.2 for the same bias region. This is attributed in [37] to the high contact resistances, which have a large impact for short channels.

For the same devices, a transit frequency of 10GHz (550nm) and 5GHz (40nm), respectively, is reported in [37, supp. inf.], but no bias dependent characteristics are shown (which, unfortunately, is typical for most of the research publications). Furthermore, a maximum available small-signal power gain of only about 0dB is achieved for the 550nm device. For the other devices in [37], unfortunately only the intrinsic figures of merit are given.

Note that essentially all Carbon-based devices exhibit more or less large hysteresis effects in the order of at least several 100mV up to several volts. This is often not mentioned in research papers, but makes the physical understanding and modelling of such devices very difficult. It can be shown that hysteresis ef-

fects can cause "apparent" linearity, i.e. bias independent f_T and g_m characteristics above the threshold voltage, which is not observed in, e.g, load-pull measurements.

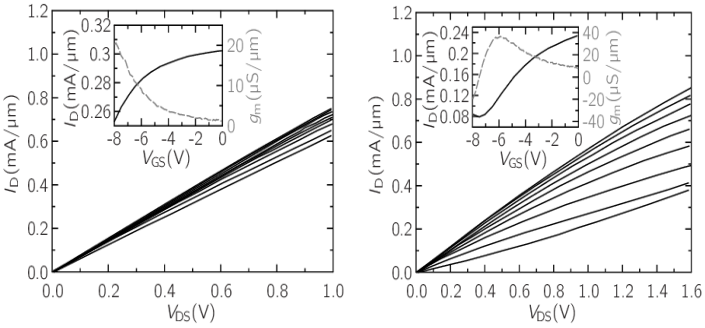

Fig. 9: Output characteristics for (a) a 2*0.04*30μm^2 and (b) a 2*0.55*30μm^2 GFET [37] with V_{GS} = -8, -7, ...-1, 0V. The inset shows the transfer current and transconductance at V_{DS} = 0.4V.

The extrinsic f_T of GFETs reported in the literature follows roughly a $1/L_g^2$ dependence as shown in Fig. 10 [7], while the best values are closer to a dependence with f_T = 10 GHzμm/L_g [26]. However, the amount of deembedding is not always clear in many of the publications. For comparison, the extsrinsic CNTFET result presented in [25] has also been inserted in Fig. 10. Note that due to the lack of a S/D-G spacer doping the *actual* average tube length is at least 1μm rather than just the gate length of 0.4μm.

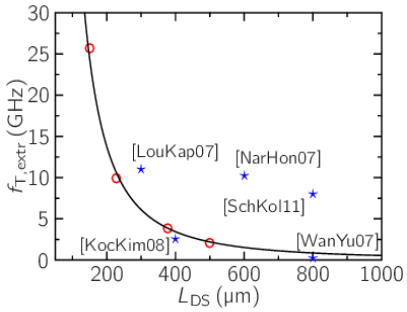

Fig. 10: Extrinsic transit frequency of GFETs (circles) vs. gate length (from [7]). The solid line is a fit through the circles. The stars correspond to CNTFET results.

The double degeneracy of the conduction band in CNTs leads to a factor of two higher transconductance and drain current saturation in a CNTFET compared to a GFET [9]. Even if the double degeneracy leads also to a larger tube capacitance, a CNTFET should still achieve a higher operating frequency as long as the performance is parasitics limited.

The reported RF-G(NR)FETs today are based on single or few-layer graphene sheets with tens of nm width. As a consequence of the missing bandgap, the transistors exhibit a very large output conductance, which has a detrimental effect on RF performance, such as power gain and cut-off frequencies. Although metallic tubes in CNTFETs have a similar effect on the transistor characteristics, the portion of metallic conductance (vs. semiconducting conductance) is relatively lower and can be significantly decreased without costly measures (cf. Section V).

Removal of a sufficient portion of metallic tubes or of their impact on electrical characteristics will significantly improve the RF performance of CNTFETs and the efficiency of amplifiers built with them. For RF analog circuit applications, a s:m ratio of at least 8 appears to be sufficient, since most analog circuits are biased at non-zero current and since competitive incumbent technologies also have a finite output conductance. Regarding linearity (e.g. OIP_3) vs. power dissipation (P_{diss}), a remaining small fraction of metallic tubes does not make much difference in RF performance (e.g., less than 1dB change in a class A amplifier).

VIII Circuit Results

This section focuses only on RF analog applications rather than on digital applications or circuits with single-tube transistors.

The very high output conductance of GFETs leads to an internal voltage gain g_m/g_{ds} of significantly less than one (e.g. 0.03...0.1 in [37] and 0.3 in [38]), making the realization of circuits with power gain and RF performance for practical applications impossible. In contrast, CNTFETs already have intrinsic voltage gains that are slightly larger than one (e.g. [25]), despite the still existing low s:m ratio. Corresponding amplifiers built by MITEQ with discrete (i.e. packaged) CNTFETs fabricated at RFNano showed 11dB power gain at 1.3GHz [39] and at least 6dB power gain at 2GHz [25].

In [27] a GFET mixer was presented that exhibits at 4GHz a conversion ***loss*** of -27dB with 20dBm LO power. Besides the huge LO power, this design actually corresponds to a passive mixer despite the use of a transistor; such results could be easier obtained with just a slightly nonlinear resistor. In contrast, mixer circuits designed with RFNano's CNTFETs achieved 8dB conversion gain with an LO power of just -2dBm at 2.4GHz [36]. These results, which are partially expected from the intrinsic voltage gain, are orders of magnitude better than those of the GFET mixer.

Finally, a very recent study published by IBM [40] has shown that CNTFETs achieve better RF performance (such as power gain and cut-off frequencies) at lower power dissipation and are thus fundamentally more suitable for RF analog applications than GFETs. This is also understandable from the superior CNT material and resulting transistor properties discussed earlier.

IX Conclusions and Outlook

An overview on Carbon-based electronics has been provided with emphasis on practical RF analog applications. Although extraordinary material properties have been predicted and already (partially) experimentally verified for both CNTs and graphene, device fabrication still faces significant challenges, such as metallic behavior/tubes, hysteresis, stable doping, and low contact resistance. Thus, today the RF performance of fabricated transistors and circuits is still far behind that of both comparable incumbent technologies and predictions based on material properties. Also, as long as the material-specific distinctive features, such as high linearity, low noise and low self-heating, cannot be retrieved from fabricated device structures, Carbon-based technologies will unlikely be successful even if the current per diameter in a CNTFET is more than four times higher than in a Si nanowire FET [41].

While many of the material related properties of graphene and CNTs are similar, there are some important differences for building transistors and circuits. Latest application-oriented considerations and simulation studies have shown that CNTFETs have fundamental advantages over GFETs from an analog RF application point of view. If the existing fabrication related obstacles for CNTFETs can be overcome and their electrical characteristics exhibit the distinctive features of the material, applications requiring high linearity, such as amplifiers and switches, operating up to about 3 GHz may be the first promising RF market. Graphene has material properties that may be more useful in other areas, such as sensor, large-scale optoelectronic, and reconfigurable circuit applications.

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