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Skalierbares Varaktormodell zur layoutabhängigen Simulation von integrierten Varaktoren

Gliederung

I) Längenskalierbarer Varaktor: Grundanforderungen und Anwendungsbereiche.

II) Technologischer Aufbau.

III) Kapazitätsverläufe und Leckstromkennlinien.

IV) Grundgedanke bei der Realisierung eines geeigneten Simulationsmodelles.

V) Ableitung eines skalierbaren Subcircuit-Varaktormodells.

VI) Allgemeine Skalierungsansätze.

VII) Kommunikation zwischen PCELL, Layout und Simulationsmodell.

VIII) Realisierte Kompakt-Simulationsmodelle.

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Scalable Varactor Device

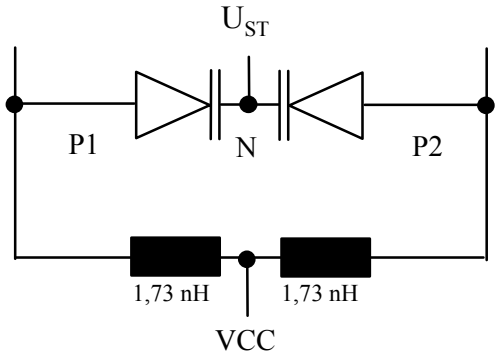
Request from circuit designers: Varactor for DECT and GSM applications.

- Differential varactor device.
- Very steep Capacitance profile.

$$\frac{C_{Var}(V_j = 0)}{C_{Var}(V_j = -2.5)} \geq 2.5$$

Vj := Varactor junction bias

Typical application circuit:



⇒ Separate implantation mask to realize a hyperabrupt doping profile.

- Scalable varactor capacitance.
- Low leakage reverse junction current.
- Acceptable quality factor up to 2.5GHz.

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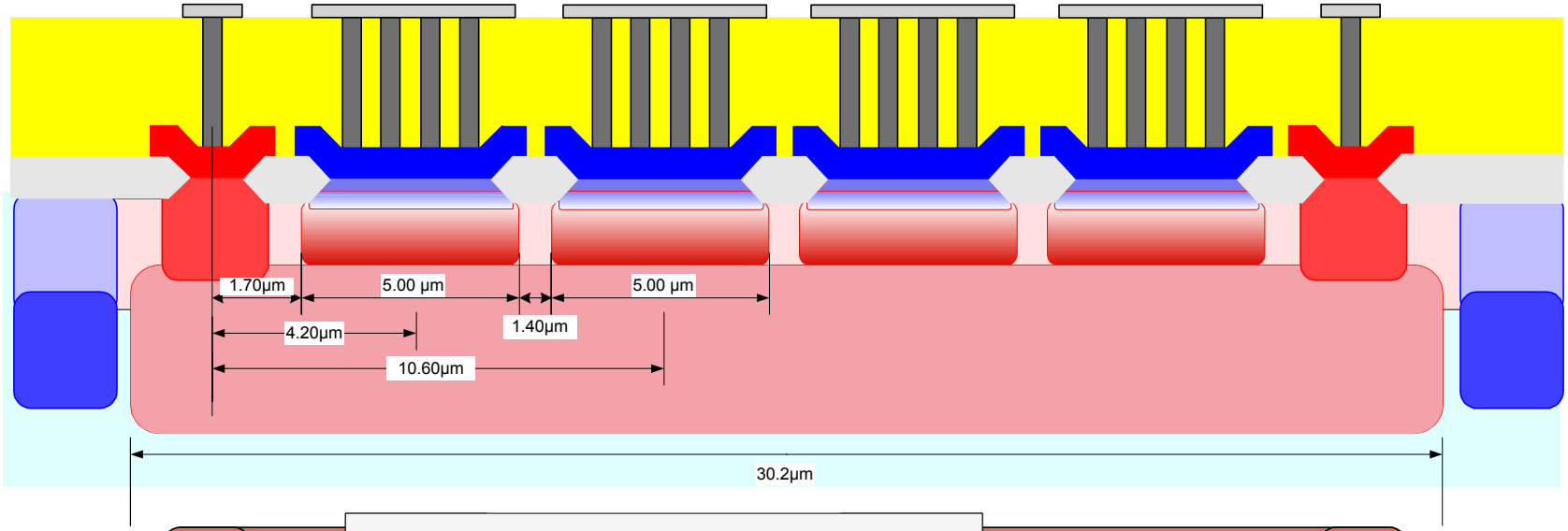
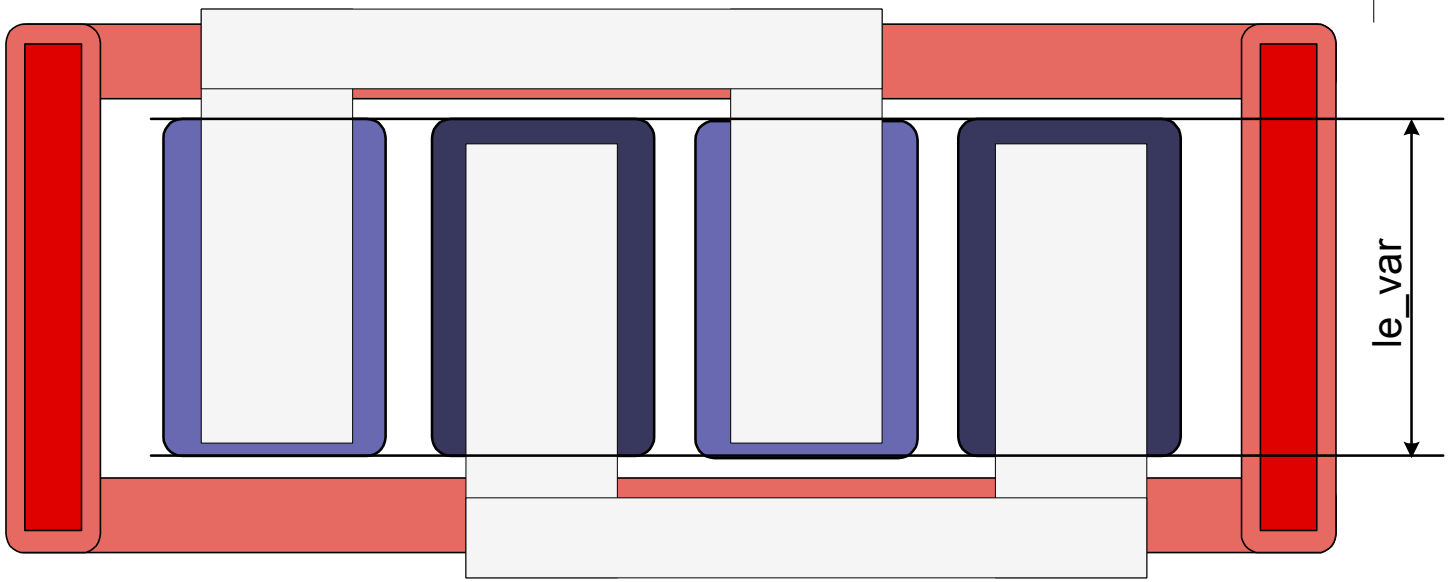
Scalable Varactor: Layout and Vertical Structure



Layout:



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Capacitance Profile of the Varactor Junction

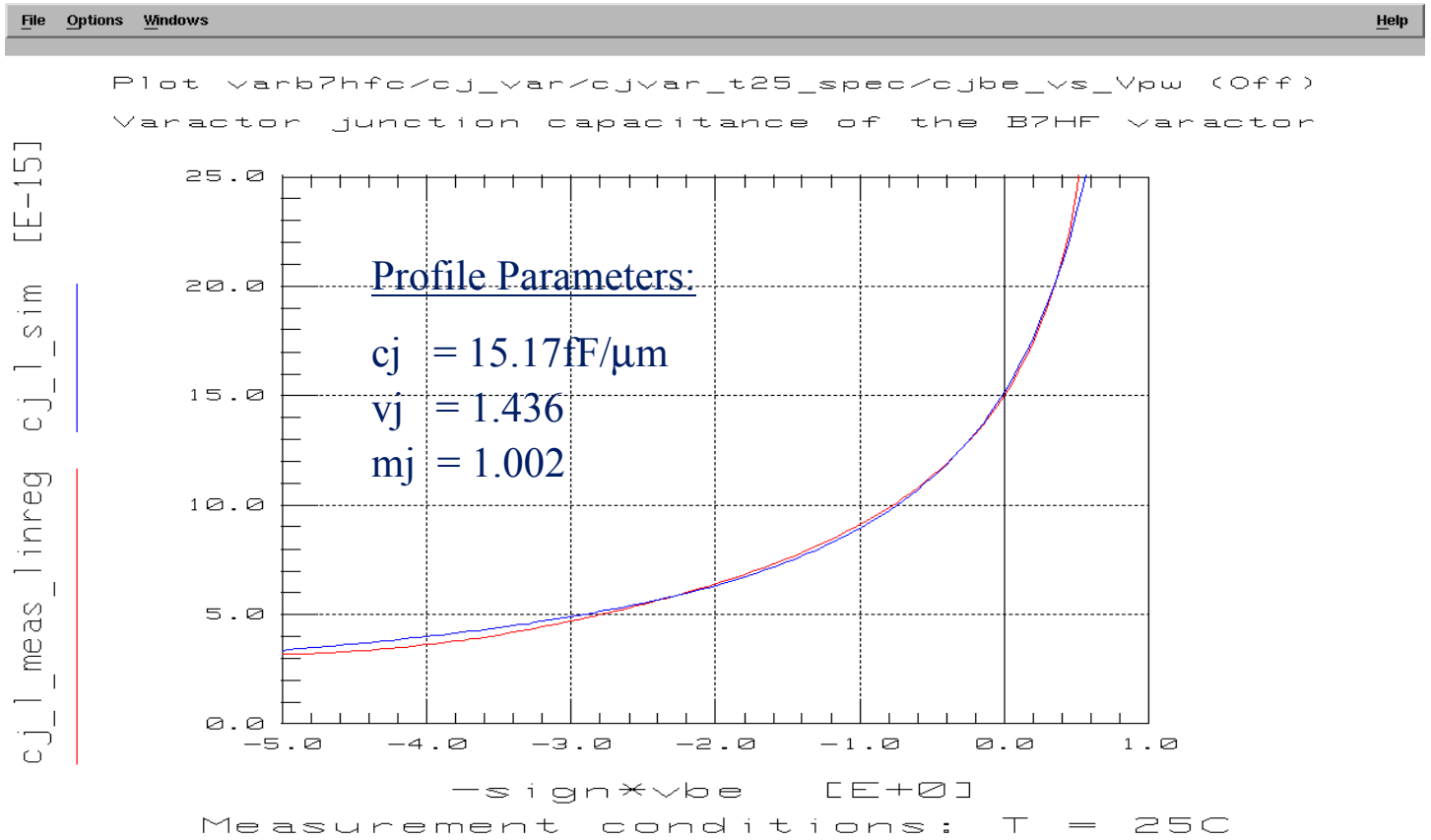

Figure : Measured and simulated varactor junction capacitances per µm unit length versus junction bias Vj. for B7HF varactor. The voltage dependence of the length-specific capacitance between node P1 and Node W was extracted from measured (red line) and simulated (blue line) data. Parasitic capacitances from contact pads and wiring were eliminated by appropriate instrument calibrating on suitable OPEN-structures. Measurement temperature was T=25°.

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Leakage currents of the Varactor Junction

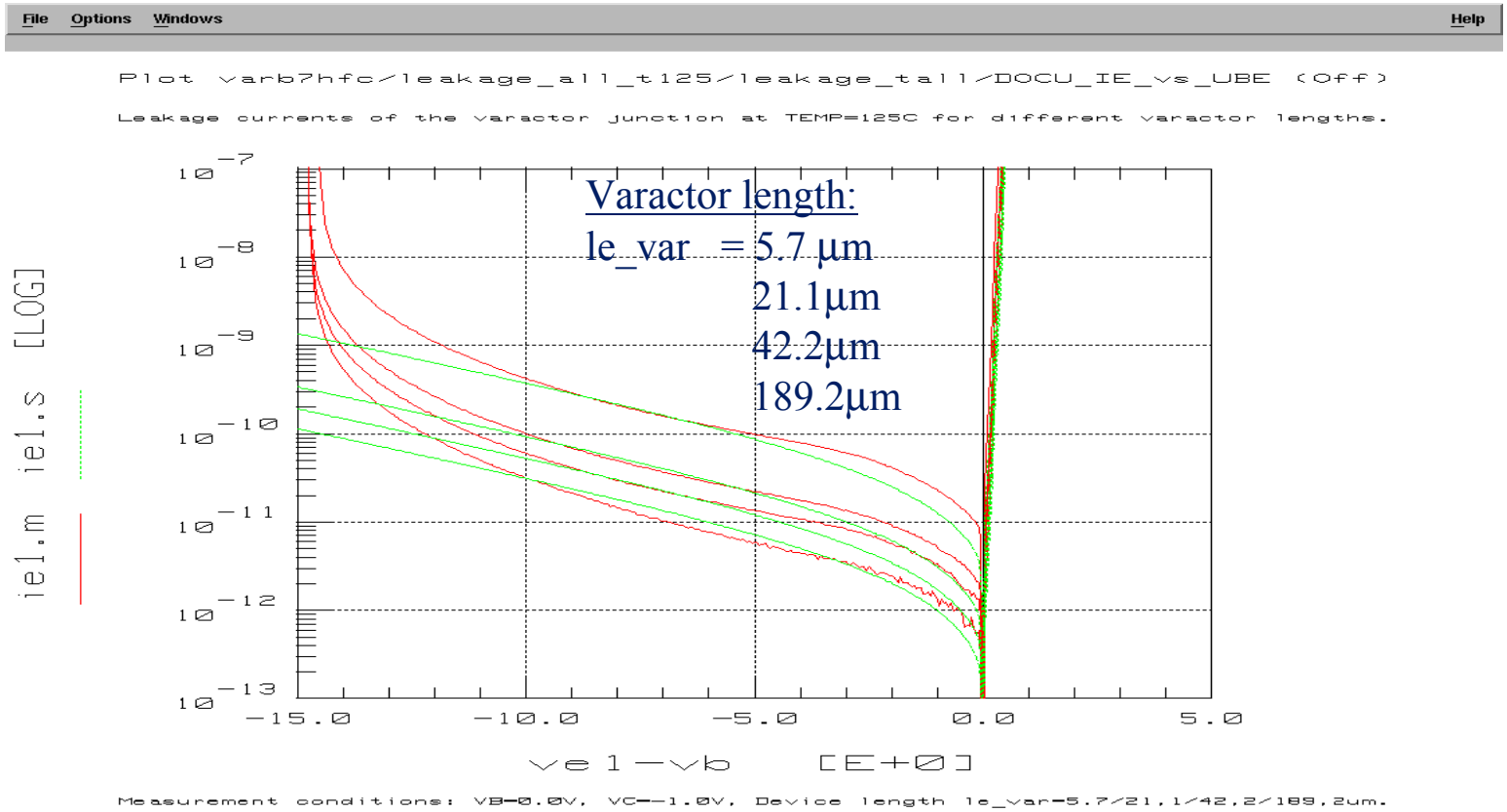

Figure : Measured and simulated varactor junction leakage currents versus junction bias Vj. for B6HFC varactor at T=+125°C for devices with different device length le_var. The length dependence of the leakage current ie1 at node P1 was measured and simulated. Therefore the voltage at node P1 was sweeped beginning from +1.0 down to -15.0V. The ie1-leakage current is shown for 4 different varactor lengths le_var=5.7 µm, 21.1µm, 42.2µm, 189.2µm. The the "base-collector"-voltage between node w and p2 was -1.0V.

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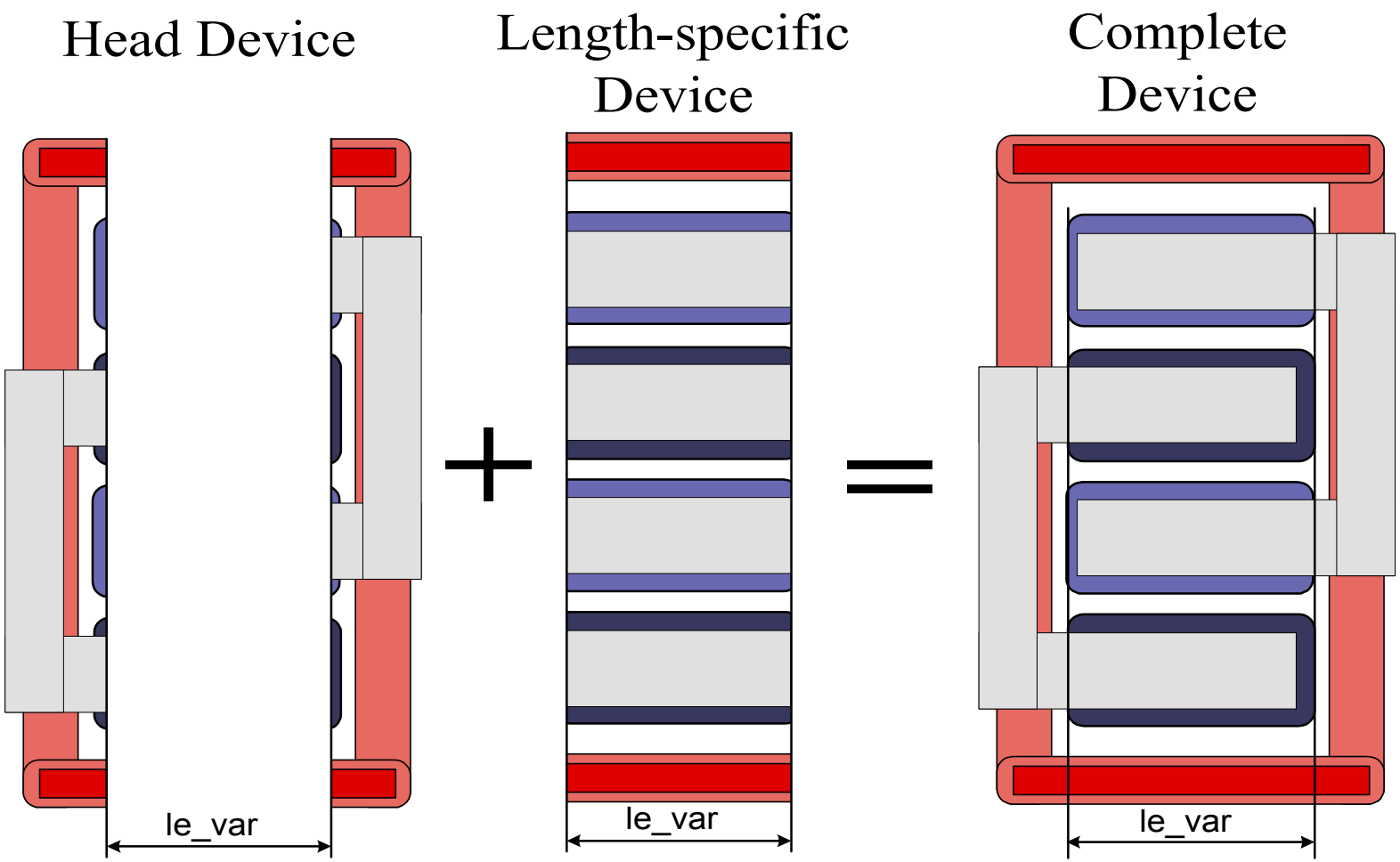
Fundamental Idea of the Scalable Varactor Model



Scaling rule for areas: $A_{dev} = A_h + le\_var \cdot A_l$

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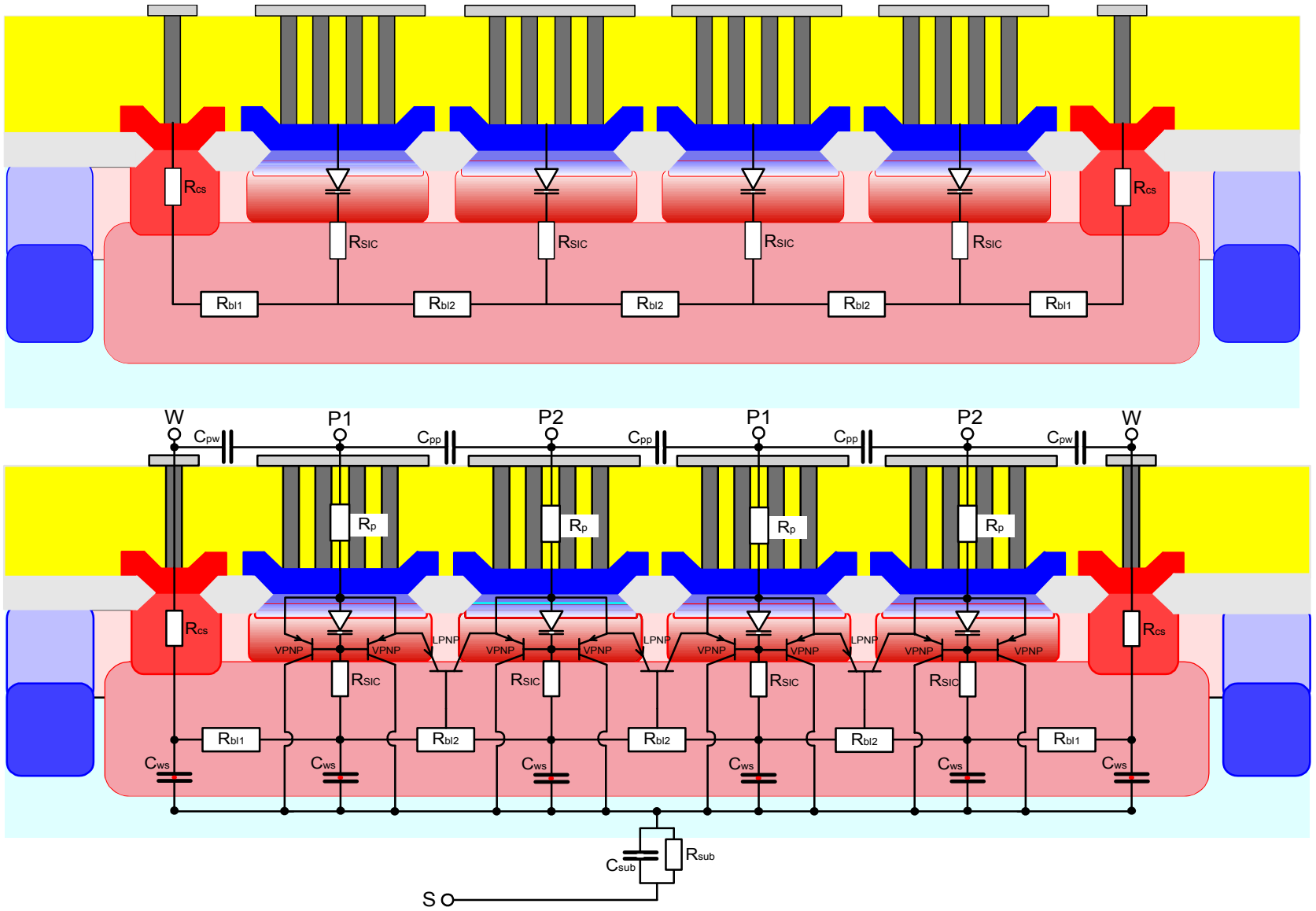
Scalable Varactor Model: Subcircuit topology.



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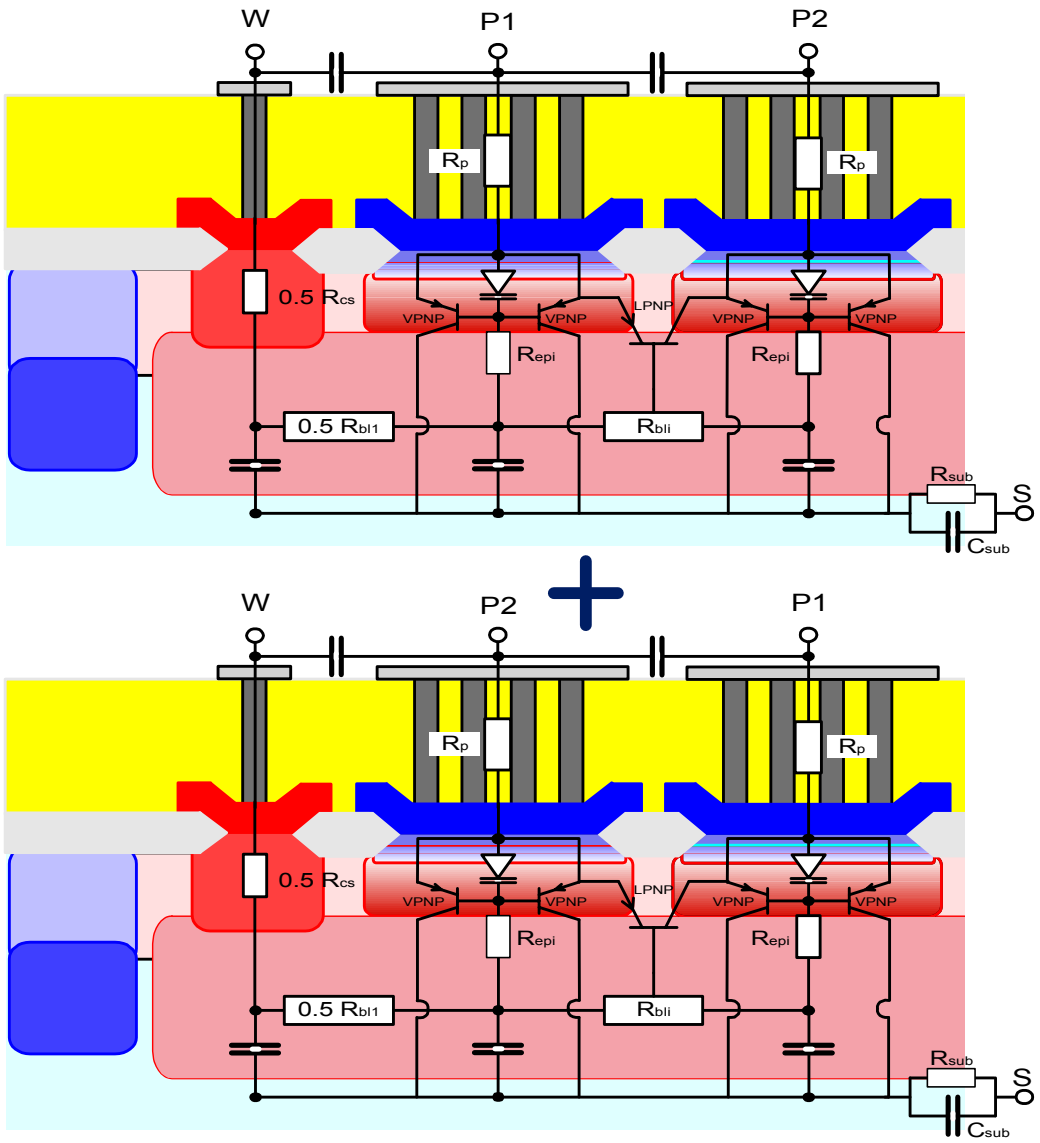
Scalable Varactor Model: Subcircuit topology.



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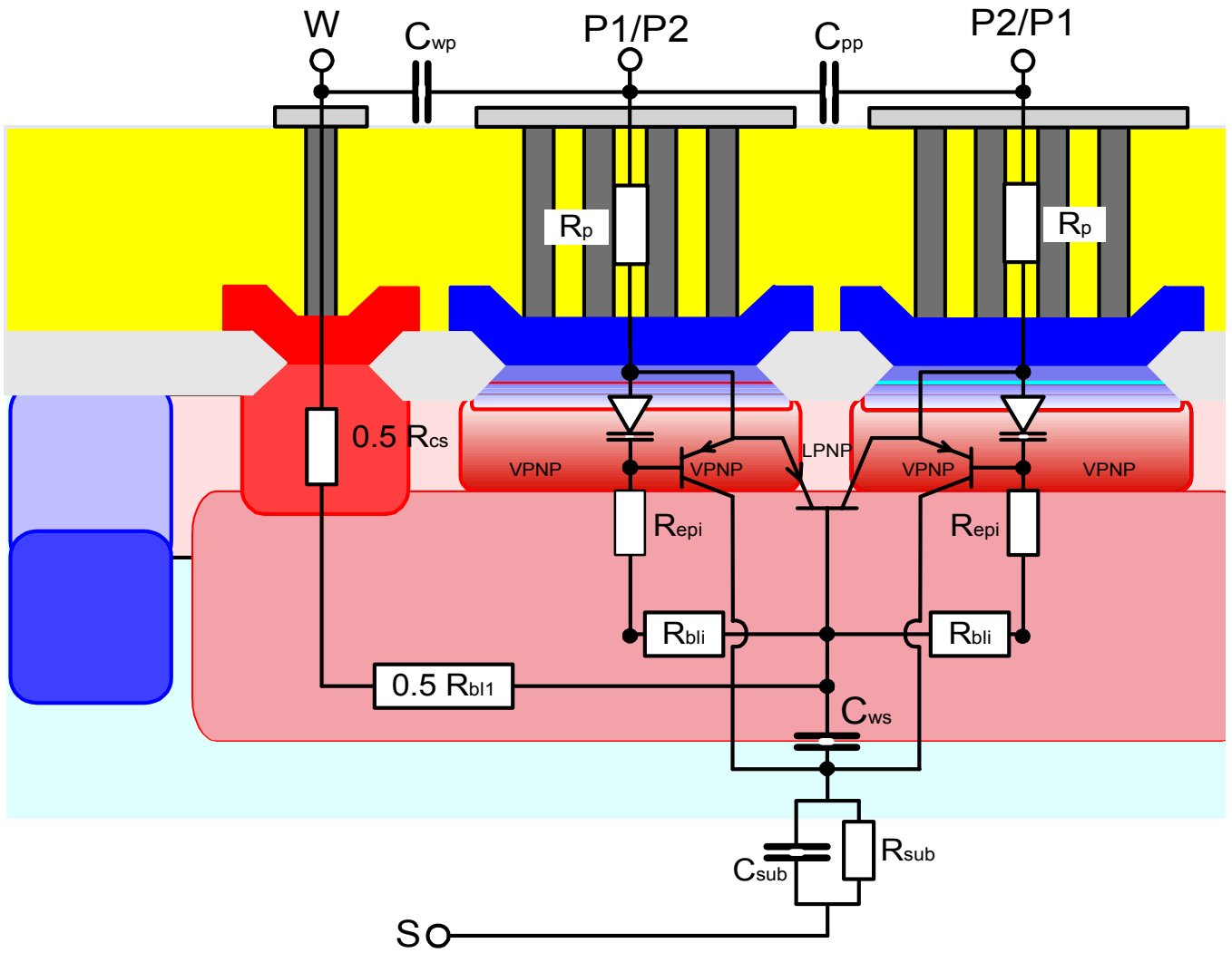
Scalable Varactor Model: Subcircuit topology.



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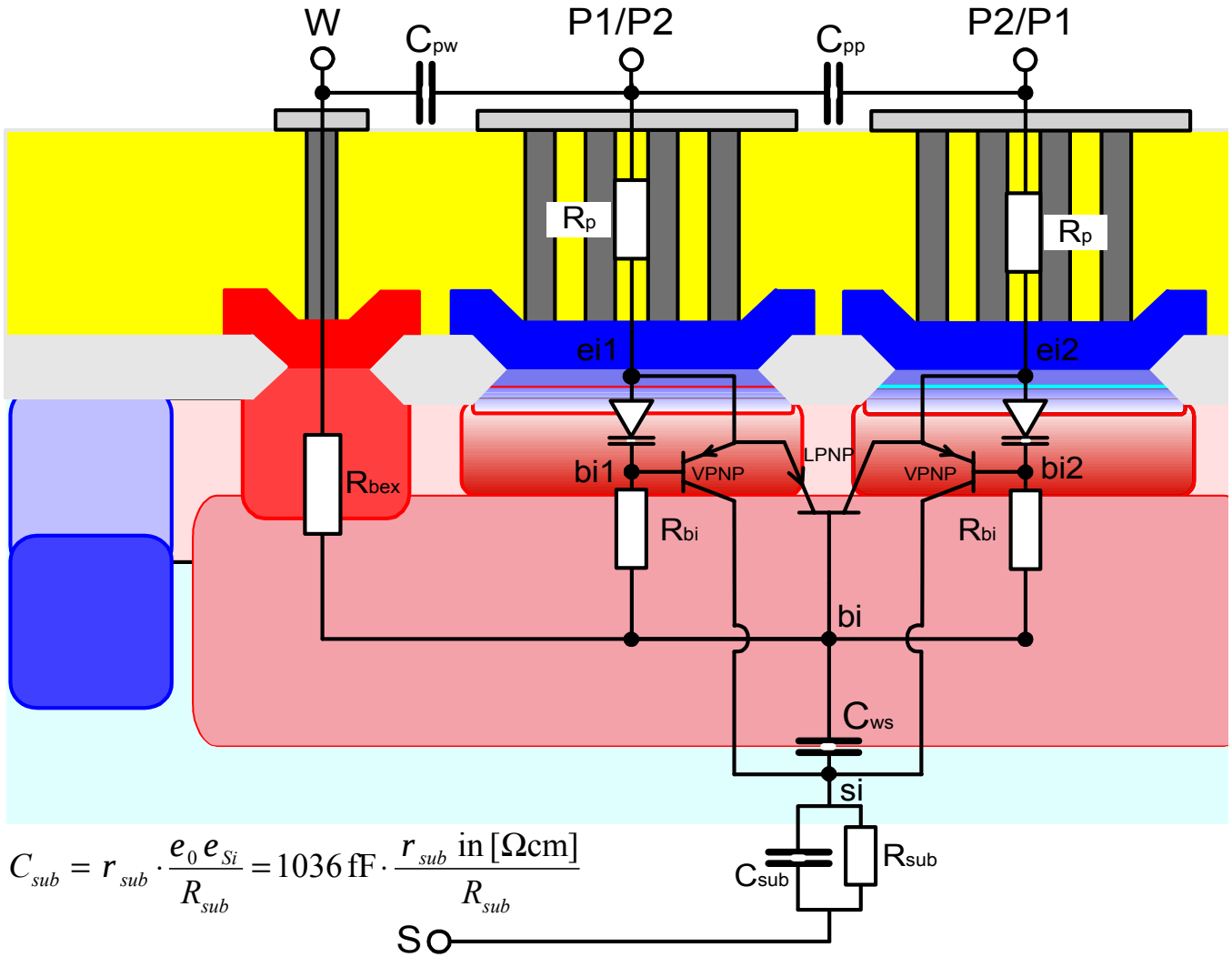
Scalable Varactor Model: Subcircuit topology.



$$C_{sub} = r_{sub} \cdot \frac{e_0 e_{Si}}{R_{sub}} = 1036\,\mathrm{fF} \cdot \frac{r_{sub}\ \mathrm{in}\ [\Omega\mathrm{cm}]}{R_{sub}}$$

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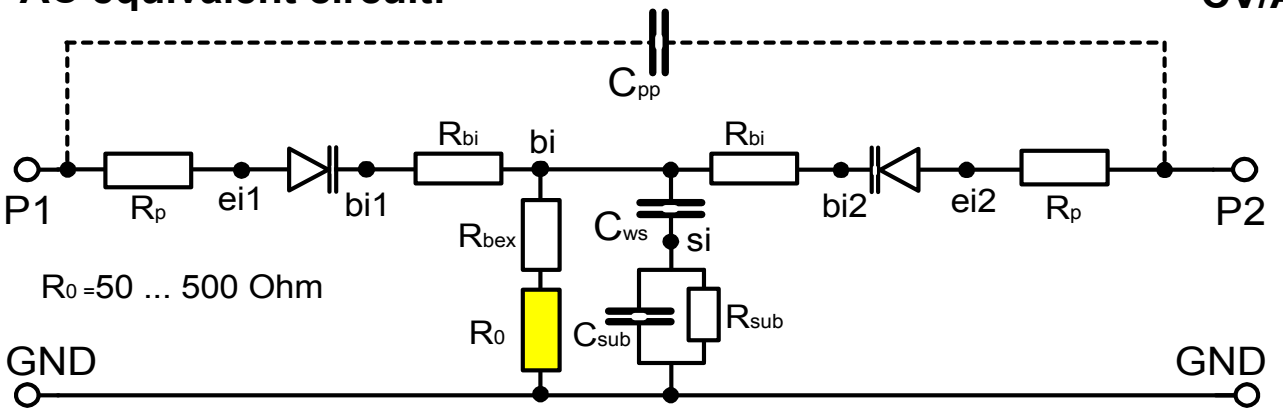
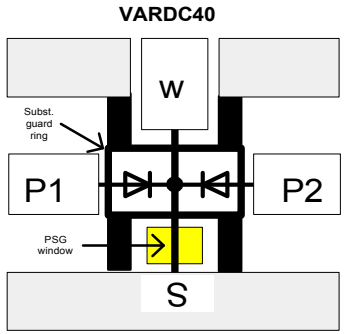
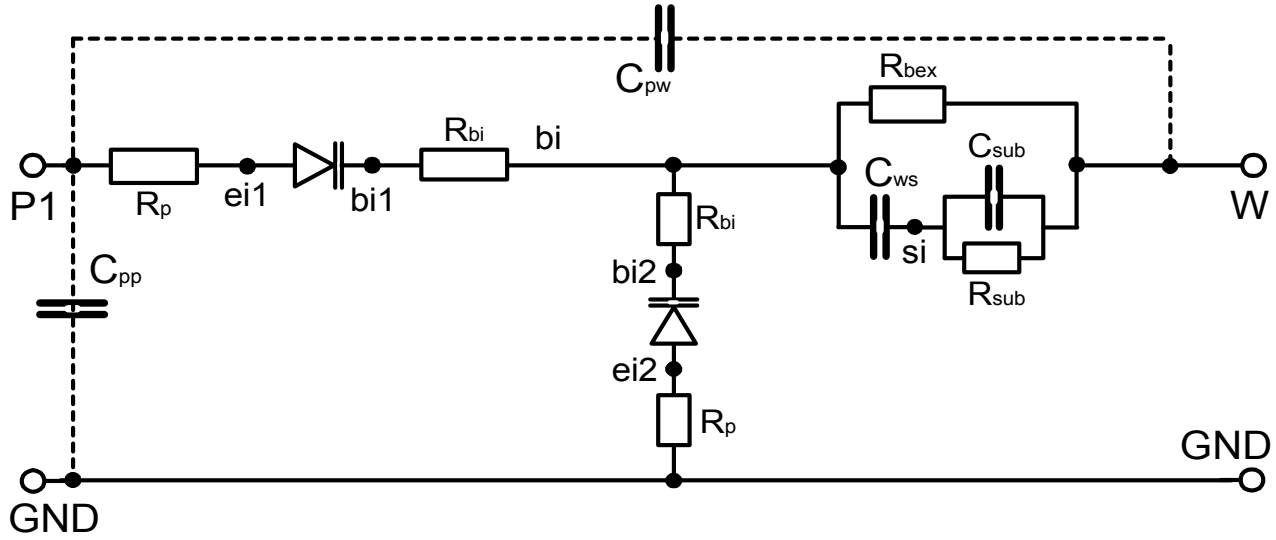
AC Equivalent Circuit Modell

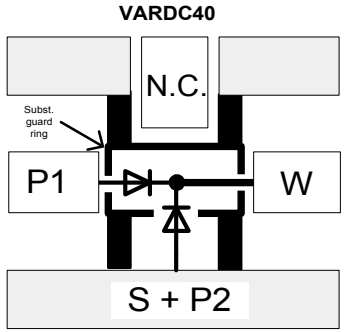
AC equivalent circuit:



CV/AC test structure:







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Basic Scaling Rule Approach

Scaling rule for capacitances:

$$C = nblocks \cdot [\ C\_h + le\_var \cdot C\_l\ ]$$

Scaling Rules for currents:

$$I = nblocks \cdot [\ I\_h + le\_var \cdot I\_l\ ]$$

Scaling rules for resistances:

$$R = \frac{R\_h \cdot R\_l}{(\ R\_h \cdot le\_var + R\_l\ ) \cdot nblocks}$$

Scaling rules for inductances:

$$L = \frac{L\_h \cdot L\_l}{(\ L\_h \cdot le\_var + L\_l\ ) \cdot nblocks}$$

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Calculation of the total varactor junction capacitance

Total junction capacitance:

$$Cjvar(V_{PW}) = nblock \left[\frac{cje\_h}{\left(1 - \frac{V_{PW}}{vje\_h}\right)^{mje\_h}} + \frac{cje\_l \cdot le\_var}{\left(1 - \frac{V_{PW}}{vje\_l}\right)^{mje\_l}} \right]$$

$$+ nblock \cdot [\, cje0\_h + cm0\_h + le\_var \cdot (cje0\_l + cm0\_l) \,]$$

V_{PW}: voltage over varactor junction between anode P1 and n-well node W.

le_var: length of one varactor block.

nblock: number of varactor blocks in parallel.

cje0_h: head specific constant capacitance.

cje0_l: length specific constant capacitance.

cje_h: head specific (bias dependent) varactor junction capacitance at V_{PW}=0.0V.

cje_l: length specific (bias dependent) varactor junction capacitance at V_{PW}=0.0V.

vje_h: built-in voltage of the head specific varactor junction capacitance.

mje_h: exponent coefficient of the head specific varactor junction capacitance.

vje_l: built-in voltage of the length specific varactor junction capacitance.

mje_l: exponent coefficient of the length specific varactor junction capacitance.

cm0_h: head specific stray capacitance between the anode strips from anode P1 and P1.

cm0_l: length specific stray capacitance between the anode strips from anode P1 and P1.

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PCELL: Interface between layout and simulation model

PCELL model controls the correct interplay between compact simulation model and varactor layout.

Three design variables are supported:

- cjvar.: Desired total varactor junction capacitance
- nblocks.: Desired number of varactor blocks
- le_var.: Desired length of one varactor block

⇒ Not all design variable combinations are allowed !!

Typical model calls:

1) vdp.v1 s w p1 p2 = cjvar=2.5p, nblocks=6
2) vdp.v2 s w p1 p2 = le_var=25.0
3) vdp.v3 s w p1 p2 = cjvar=5.0p, le_var=50.0

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PCELL: Interface between layout and simulation model

Definition of the minimum and maximum allowed block capacitances:

$$cmin = le\_em\_min \cdot \left(cje\_l + cje0\_l + cm0\_l \right) + cje\_h + cje0\_h + cm0\_h$$

$$cmax = le\_em\_max \cdot \left(cje\_l + cje0\_l + cm0\_l \right) + cje\_h + cje0\_h + cm0\_h$$

Calculation of total number of needed varactor blocks:

$$nvar = INT\left(\frac{cjvar}{cmax} \right) + 1$$

Calculation of the appropriate length for one varactor block.

$$le\_var = \frac{cjvar - \left(cje\_h + cje0\_h + cm0\_h \right) \cdot nvar}{nvar \cdot \left(cje\_l + cje0\_l + cm0\_l \right)}$$

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Verfügbare Kompakt-Simulationsmodelle

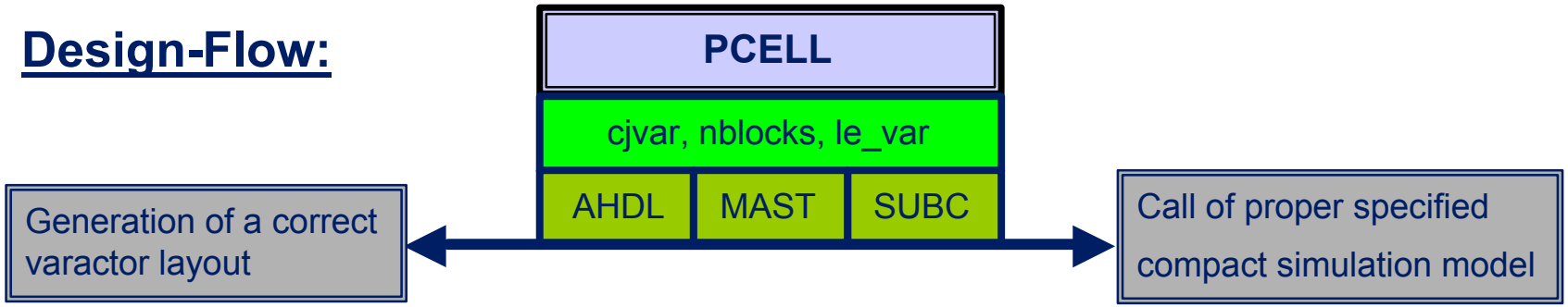
SPECTRE AHDL: Zulässige Designvariablen: cjvar, nblocks, le_var

SABER MAST: Zulässige Designvariablen: cjvar, nblocks, le_var

Subcircuit-Modell: Zulässige Designvariablen: nblocks, le_var

Subcircuit model: Modell für alle „Spice-orientierten“ Simulatoren wie z.B. HSPICE, ELDO, TITAN, ... Skalierung erfolgt über den Area-Faktor.

Design-Flow:



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Subcircuit-Simulationsmodell

```
####  BEGIN OF VARACTOR TEMPLATE DEFINITION ####
template vdpsgp01 s w p1 p2 = nblocks, le_var
number nblocks=undef, le_var = undef
electrical s, w, p1, p2
{
number re_h   = 30.0,      re_l   = 15,
       rbi_h  = 50.0,      rbi_l  = 100,
       rbm_h  = 100.0,     rbm_l  = 300,
       rs_h   = 1000,      rs_l   = 4000,
       ro_sub = 20,
       cje0_l = 1.000E-18, cje0_h = 1.000E-18,
       cjc0_l = 1.000E-18, cjc0_h = 1.000E-18,
       cmpp_l = 1.000E-18, cmpp_h = 1.000E-18,
       cmpw_l = 1.000E-18, cmpw_h = 1.000E-18

number re_ex    = (re_h * re_l)  /((le_var * re_h + re_l)  *nblocks),
       rbi_ex   = (rbi_h * rbi_l)/((le_var * rbi_h + rbi_l)*nblocks),
       rbm_ex   = (rbm_h * rbm_l)/((le_var * rbm_h + rbm_l)*nblocks),
       rs_ex    = (rs_h  * rs_l) /((le_var * rs_h  + rs_l )*nblocks),
       cbe_con  = nblocks*(( cje0_l  * le_var ) + cje0_h ),
       cbc_con  = nblocks*(( cjc0_l  * le_var ) + cjc0_h ),
       cpp_stray = nblocks*(( cmpp_l * le_var ) + cmpp_h ),
       cpw_stray = nblocks*(( cmpw_l * le_var ) + cmpw_h )

 #-----------------------------------------------------------------#
 #  Definition of parameter sets for the varactor subcircuit model  #
 #-----------------------------------------------------------------#
 # Parasitic lateral PNP model definition. Head specific amount
 q..model sgp_lpnp_h  = (        TYPE= _p,
 IS  = 1.091E-18 ,    ISE = 0         ,   NE  = 1.9       ,
 .......
 KF = 0.0          ,   TNOM= 25    ,    GMIN= 1E-12 )
 #-----------------------------------------------------------------#
```

```
# Parasitic lateral PNP model definition. Length specific amount
 q..model sgp_lpnp_l  = (        TYPE= _p,
 IS  = 4.2745E-19,    ISE = 0         ,   NE  = 1.9       ,
.......
 KF = 0.0          ,   TNOM= 25    ,    GMIN= 1E-12 )
#-----------------------------------------------------------------#
 # Parasitic substrate PNP model definition . Head specific amount
 q..model sgp_vpnp_h = (         TYPE= _P,
 IS  = 2E-20       ,    ISE = 3E-17  ,   NE  = 1.75     ,
 .......
 KF = 0.0          ,   TNOM= 25    ,    GMIN= 1E-12 )

 #-----------------------------------------------------------------#
 # Parasitic substrat PNP model definition. Length specific amount
 q..model sgp_vpnp_l = (         TYPE= _P,
 IS  = 2.4294E-20,    ISE = 1.25E-17,   NE  = 1.75  ,
 .......
 KF = 0.0          ,   TNOM= 25    ,    GMIN= 1E-12 )

 #-----------------------------------------------------------------#
 # Varactor junction leakage diode model definition. Head specific amount
 d..model d_leak_h =  (IS     = 1E-12,   rs     = 2.5   ,
 .....
 gmin   = 1E-14  )
 #-----------------------------------------------------------------#
 # Varactor junction leakage diode model definition. Length specific amount
 d..model d_leak_l =  (  IS     = 1.57E-13,   rs     = 5                    ,
 ........
 gmin   = 1E-12  )
 #-----------------------------------------------------------------#
 #     Circuit definition  of the varactor subcircuit model        #
 #-----------------------------------------------------------------#
```

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Subcircuit-Simulationsmodell

```
# VERTICAL PARASITIC TRANSISTOR
 q.tv1h si  bi1  ei1 si    =  model = sgp_vpnp_h,  AREA = nblocks
 q.tv2h si  bi2  ei2 si    =  model = sgp_vpnp_h,  AREA = nblocks
 q.tv1l si  bi1  ei1 si    =  model = sgp_vpnp_l,  AREA = le_var*nblocks
 q.tv2l si  bi2  ei2 si    =  model = sgp_vpnp_l,  AREA = le_var*nblocks

 # LATERAL PARASITIC TRANSISTOR
 q.tl1h ei2 bi ei1 si      =  model = sgp_lpnp_h,  AREA = nblocks
 q.tl1l ei2 bi ei1 si      =  model = sgp_lpnp_l,  AREA = le_var*nblocks

# VARACTOR JUNCTION PERIMETER LEAKAGE DIODE
d.dio1h   bi1  ei1        =  model = d_leak_h,  AREA = nblocks
d.dio2h   bi2  ei2        =  model = d_leak_h,  AREA = nblocks
d.dio1l   bi1  ei1        =  model = d_leak_l,  AREA = le_var*nblocks
d.dio2l   bi2  ei2        =  model = d_leak_l,  AREA = le_var*nblocks

# VOLTAGE INDEPENDENT CAPACITANCES:
c.c0p1p2 p1   p2   =  cpp_stray,  tc=[0.0, 0.0]
c.c0pw1  p1   w    =  cpw_stray,  tc=[0.0, 0.0]
c.c0pw2  p2   w    =  cpw_stray,  tc=[0.0, 0.0]
c.conp1  bi1  ei1  =  cbe_con,    tc=[0.0, 0.0]
c.conp2  bi2  ei2  =  cbe_con,    tc=[0.0, 0.0]
c.cbco   bi   si   =  cbc_con,    tc=[0.0, 0.0]
c.csub   si   s    =  1.036e-12 * ro_sub / rs_ex   # dielectric substrate capacitance.

# SERIAL RESISTORS:
r.rp1    ei1  p1   =  re_ex,      tc=[0.0, 0.0]
r.rp2    ei2  p2   =  re_ex,      tc=[0.0, 0.0]
r.rbi1   bi1  bi   =  rbi_ex,     tc=[0.0, 0.0]
r.rbi2   bi2  bi   =  rbi_ex,     tc=[0.0, 0.0]
r.rbex   bi   w    =  rbm_ex,     tc=[0.0, 0.0]
r.rsex   si   s    =  rs_ex,      tc=[0.0, 0.0]
 }
#####  END OF VARACTOR TEMPLATE DEFINITION FOR vdpsgp01   #####
```

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