IHP Technology

Vision and Roadmaps

Technology Schedules/ Development Strategies

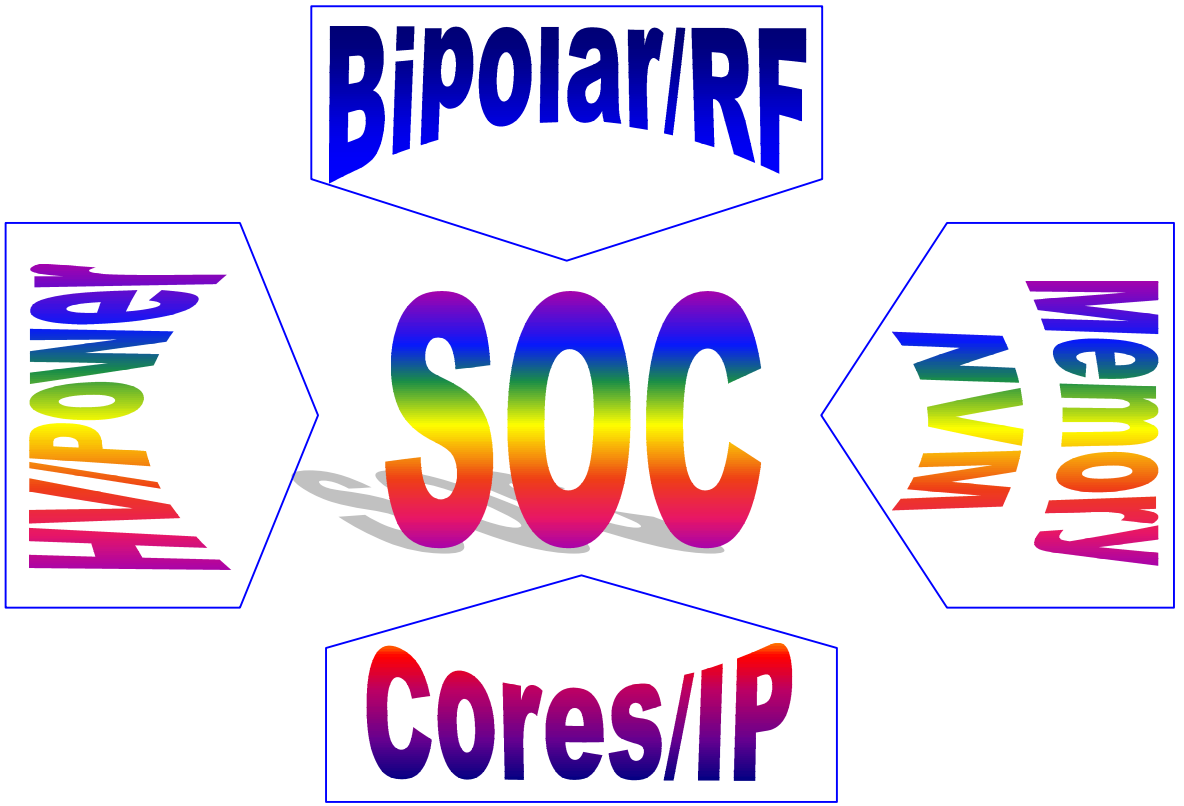
Qualification Strategy

Design Readiness

IHP Technology Vision

Develop
High Value Added Technologies
for Wireless and Broadband

Technologies for Wireless & Broadband



SiGe:C Bipolar Parameter Roadmap

Parameter	0.25 µm (Available)		0.18 µm (Target)		0.13 µm (Vision)	
	High Performance	High-Voltage	High Performance	High Voltage	High Performance	High Voltage
A_E (µm^2)	0.42 x 0.84	0.42 x 0.84	0.21 x 0.84	0.21 x 0.84	0.15 x 0.84	0.15 x 0.84
Peak f_{max} (GHz)	95	90	150	120	180	150
Peak f_T (GHz)	80	55	100	40	>120	45
BV_{CEO} (V)	2.4	3.2	2.0	5.0	1.9	5.2
BV_{EBO} (V)	4.5	4.5	3.5	3.5	2.9	2.9
BV_{CBO} (V)	6.0	9.0	4.9	12.0	4.5	12.0
β	150	150	135	135	120	120
V_A (V)	50	90	40	100	20	120
NF_{min} (dB) *)	0.8	0.8	<0.7	<0.7	<0.7	<0.7
Assoc. Gain (dB) *)	17	17	>17	>17	>17	>17
R_B (Ω)	120	120	90	90	<70	<70
C_{BE} (fF)	4.5	5	3	3		
C_{BC} (fF)	8	6	6	2		

*) special device, @ 2 GHz, I_C = 2 mA

0.18µm Research Strategy
Process Development Schedules

- **Mar '01: 0.18µm Baseline CMOS process defined (Intel)**
- **Two integration concepts being currently pursued**
  - **Advanced CMOS:**
    - Strict-drop-in module approach.
    - Reduction of process complexity
  - **Advanced Bipolar:**
    - No compromise in bipolar performance
- **March '02: Ready for full process at IHP**
  - **Parallel continuation of the conceptional work on the 0.25µm tool suite.**
- **Q1/2003: Transfer to Communicant**

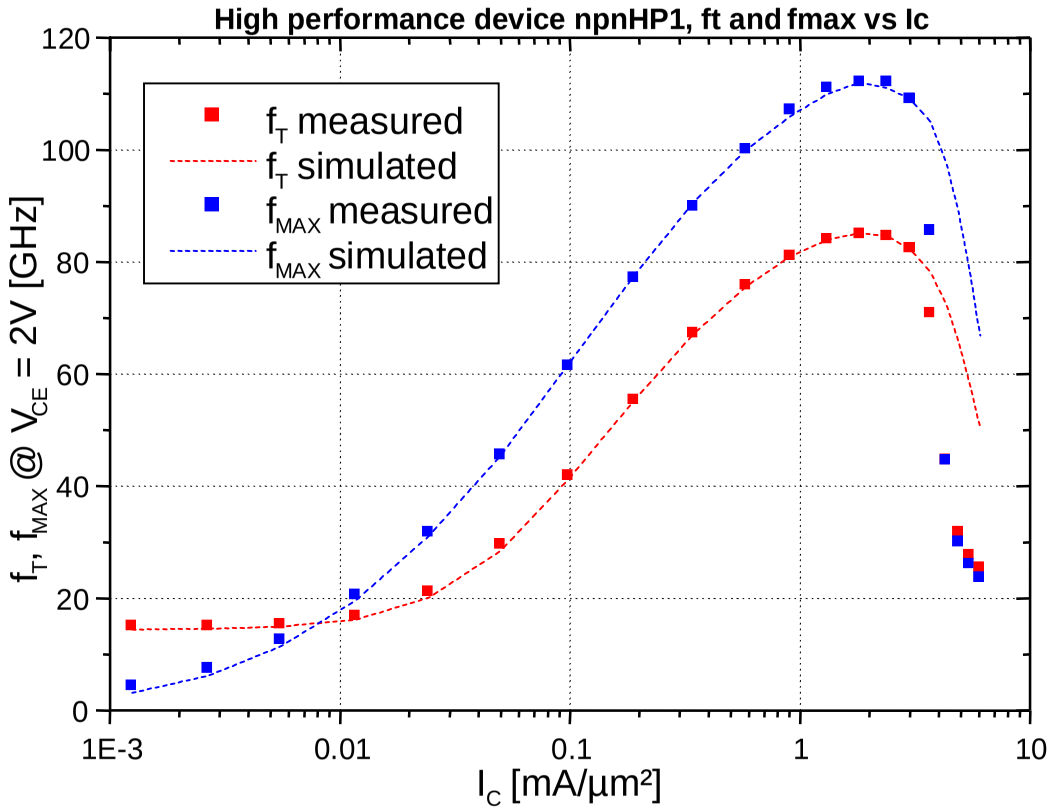
Qualification Strategy

- **Q4/02: Start 0.18µm SiGe:C BiCMOS qualification**

- **BiCMOS/Bipolar qualification vehicles yet to be defined:**
  - **Target: BiCMOS test chip + 40GBit/sec building blocks**
  - **Reference 0.25µm BiCMOS Testchip:**
    - Various yield arrays (64k bipolar transistors)
    - Ring oscillators (CML, BiCMOS)
    - Power transistors (arrays, ring oszillators)
  - **Divider (Multiplexer, Demux)**

Design Readiness
0.25µm SiGe:C BiCMOS

- 50/90 GHz ft/fmax high voltage device including statistics: April ‘01 ✔
- 80/95 GHz ft/fmax milestones:
  - Dec ’00: Mod. rev. 0.1 released for internal use ✔
  - Aug ‘01: Mod. rev. 1.0 ✔
  - Q1-2/01: Qualification
    (dep. upon actual requirements)
- Analog/Mixed Cadence based flow supported
  - Diva & Dracula verification
  - P-cells, LVS, DRC, Extract
- Digital libraries available

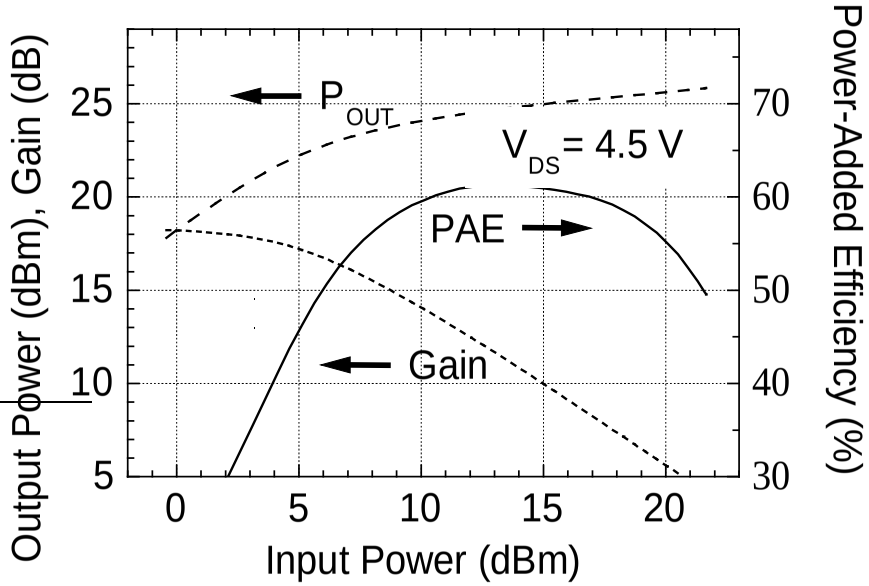


Design Readiness LDMOS

Key Electrical Parameters

Parameter	Unit	LDMOS 15	Comment
L_{DRIFT}	µm	0.6	
L_{GATE}	µm	0.245	
T_{OX}	nm	5	
I_{DSAT}	µA/µm	125	@ V_G=1.5V; V_{DS}=4V
I_R	pA/µm	<1.5	@ (V_{BR}-2V)
V_{BR}	V	15	@ 10 pA/µm
R_{ON}	Ωmm	6.2	@ V_G=2.5V
PAE_{MAX} @ 2GHz	%	70	@V_{DS}=6.5V,W=739 µm
P_{OUT}@ PAE_{MAX}	mW dBm	560 27.5	@V_{DS}=6.5V, W=739 µm
PAE_{MAX} @ 5GHz	%	60	@V_{DS}=4.5V, W=739 µm
P_{OUT} @ PAE_{MAX}	mW dBm	380 25.8	@V_{DS}=4.5V, W=739 µm
$F_{T,MAX}$@V_{DS}=4V	GHz	23	W=56µm
$F_{T,MAX}$@V_{DS}=12V	GHz	30	W=56µm
F_{MAXMAX}@V_{DS}=4V	GHz	43	W=56µm
F_{MAXMAX}@V_{DS}=12V	GHz	52	W=56µm

Output power, Gain, and PAE vs. input power for the LDMOS15 device @ 5GHz



- **Breakdown voltages adjustable via L_{DRIFT}**
- **Device included in standard process flow**
- **Very limited experience in application and therefore modeling**

Summary

- **0.25µm SiGe:C BiCMOS available**
- **Project 0.18µm Intel CMOS copy-exact transfer in progress**
- **Encouraging results on 0.18µm bipolar performance**
- **Encouraging results on novel LDMOS devices better understanding of potential application areas required**

On the road to a full communication SOC