

An Accurate Transistor Model for Simulating Avalanche-Breakdown Effects in Si Bipolar Circuits

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ABSTRACT: A physics-based scalable transistor model is described which allows to consider accurately avalanche-breakdown effects in bipolar circuit simulation. It consists of 6 lumped transistor elements, connected via elements of the base and emitter resistance, and can be applied to arbitrary transistor geometries.

1 Introduction

Modeling the breakdown behavior of Si bipolar transistors is a central problem in the design of high-speed circuits, especially for all kinds of driver and output power stages. This is because the transistors of these stages suffer from low breakdown voltage as a consequence of the demand on high current carrying capability typical for high-speed technologies (i.e. strongly doped and thin collector regions) [1]. Therefore, accurate modeling is a must to exploit the potential of advanced Si bipolar technologies as far as possible and, especially, to allow transistor operation *above* the breakdown voltage BV_{CEO} ($I_B = 0$).

Above a certain V_{CE} (mostly $\approx BV_{CEO}$) the base current becomes negative due to increased impact ionization. In [2], [3] it was shown, how instabilities in the transistor structure, which are caused by the negative base current, limit the maximum usable output voltage of Si bipolar transistors. They can lead to snap-back of the output characteristics, to parasitic oscillations, or only to discontinuities in the collector current. The onset of instability is well defined by critical base currents I_{Bcrit} which can be calculated for (quasi-)static operation by analytical relations [2], [3]. This theory has been verified by measurements as well as by a **quasi-distributed three-dimensional (3D) transistor model (QDTM)** consisting of a lot of transistor elements (e.g. > 1000) [3].

The breakdown behavior of a transistor driven by $V_{BE} \approx const.$ can still be explained by the classical transistor theory and can accurately be calculated by use of a 2-transistor model [4]. For $I_E \approx const.$ (or in the more general case of a high source impedance at the emitter node¹), the breakdown voltage is higher than for $V_{BE} \approx const.$, but not nearly as high as expected from the classical theory. This is because at a critical base current ($I_{Bcrit} = I_B^*$) the emitter current abruptly pinches in to a small area in the center of the emitter. This effect is – as in the case of $V_{BE} \approx const.$ – caused by a lateral voltage drop across the base resistance r_B but can no longer be modeled by a two-dimensional transistor model. Instead a three-dimensional model like the QDTM is required [2], [3].

The calculation of the maximum usable output voltage

¹This holds for several practical transistor stages, e.g. used in high-speed circuits, like cascode stages, emitter followers, transadmittance stages with strong negative feedback, and, to a certain extent, emitter coupled differential stages [1].

via the critical base current is restricted to (quasi-)static operations. Moreover, for driving conditions deviating from the special cases $V_{BE} \approx const.$ and $I_E \approx const.$ the calculation can be quite complicated. These restrictions would be overcome by use of the accurate QDTM which, however, is too expensive for circuit design. Therefore, the main aim of this paper is to present a new transistor model which considers the 3D character of the breakdown behavior nearly as accurately as the QDTM, but is simple enough for circuit simulation. It will be demonstrated that a model consisting of six (active) transistor elements only is an adequate compromise between the contradicting demands on accuracy and simplicity. For these elements, all kinds of transistor models can be used but – if not yet provided – they must be extended by an adequate current source between the internal base and collector node in order to model avalanche multiplication [3].

This “6 transistor model” (6TM) shows the designer the onset of avalanche induced instabilities and thus the limit of the usable operating range of the critical transistors. This holds for arbitrary emitter geometries, for arbitrary driving and loading conditions, and even for high-speed operation.

2 A 6-Transistor Model for Simulating the Onset of Instabilities

Fig. 1 shows the equivalent circuit of the 6TM and the corresponding lateral partitioning of the transistor into its elements. Due to the symmetry in x - and y -direction only a quarter of the transistor has to be considered. This means that the total (internal) transistor is partitioned into $4 \times 6 = 24$ elements. Since the transistor and resistor elements of the four quarters can be shunted, the elements in Fig. 1 and also in the equations given below represent the *complete* 6TM and not only a quarter of the transistor.

In x -direction the internal transistor is partitioned into two columns as proposed in [5], with 40 % of the emitter area for the outer and 60 % for the inner transistor elements. In y -direction partitioning into three rows with 20 % of the emitter area for the inner and 40 % for the other two rows proved to be an adequate compromise.² With $A_E = b_E l_E$ (l_E, b_E : emitter length and width, respectively), the emitter areas $A_{E\mu\nu}$ of the transistor elements $T_{\mu\nu}$ are given by:

$$A_{E11} = A_{E12} = 0.4l_E \times 0.4b_E = 0.16A_E \quad (1)$$

$$A_{E21} = A_{E22} = 0.4l_E \times 0.6b_E = 0.24A_E \quad (2)$$

$$A_{E13} = 0.2l_E \times 0.4b_E = 0.08A_E \quad (3)$$

$$A_{E23} = 0.2l_E \times 0.6b_E = 0.12A_E \quad (4)$$

²This corresponds to a division of the total emitter into 5 rows with equal width.

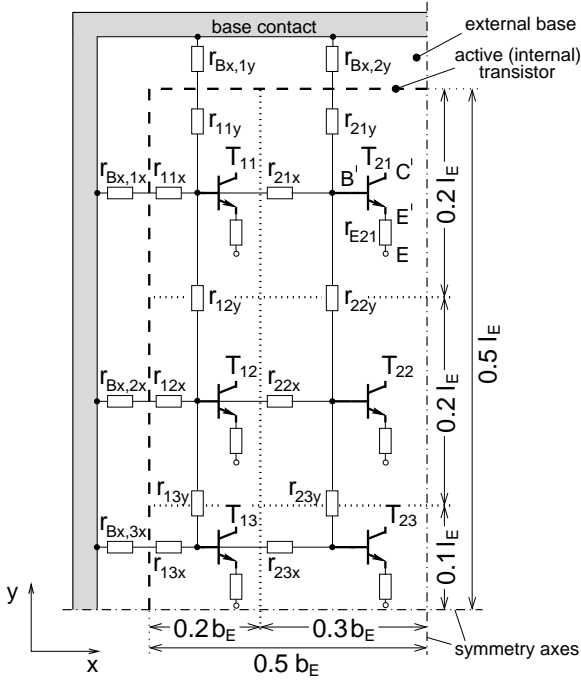


Fig. 1: Equivalent circuit of the 6TM by lateral partitioning the active (internal) transistor into 4×6 elements. The connection of the emitter nodes is not shown. The collector nodes are connected via elements of the lateral collector resistance, similar to the r_B network (not shown).

From these emitter areas, the parameters of the internal transistor elements can easily be calculated. For example, the transfer saturation current as well as the internal CB- and EB-junction capacitance are all proportional to $A_{E\mu V}$, while the emitter resistance is proportional to the reciprocal value of $A_{E\mu V}$.

The resistor elements of the *internal* base in x -direction can be calculated from length and width of the corresponding transistor elements and from the sheet resistance r_{si} of the internal base:

$$r_{11x} = r_{12x} = 2.5r_1 \quad , \quad r_{21x} = r_{22x} = 2.5r_2 \quad , \quad (5)$$

$$r_{13x} = 5r_1 \quad , \quad r_{23x} = 5r_2 \quad , \quad (6)$$

$$\text{with [5]} \quad r_1 = 0.15r_0 \quad , \quad r_2 = 0.5r_0 \quad , \quad (7)$$

$$\text{and} \quad r_0 = \frac{r_{si} b_E}{4 l_E} \quad . \quad (8)$$

The resistor elements in y -direction can be approximated by

$$r_{12y} = r_{13y} = \frac{r_{si} l_E}{4 b_E} \quad , \quad r_{22y} = r_{23y} = \frac{r_{si} l_E}{6 b_E} \quad , \quad (9)$$

$$r_{11y} = 0.5r_{12y} \quad , \quad r_{21y} = 0.5r_{22y} \quad . \quad (10)$$

The elements of the *external* base resistance can be calculated from the length-specific value r'_{Bx} and the contribution of the corresponding transistor elements to the emitter periphery. We get for x - and y -direction, respectively,

$$r_{Bx,1x} = r_{Bx,2x} = \frac{1}{2} \cdot \frac{r'_{Bx}}{0.4l_E} \quad , \quad r_{Bx,3x} = \frac{1}{2} \cdot \frac{r'_{Bx}}{0.2l_E} \quad , \quad (11)$$

$$r_{Bx,1y} = \frac{1}{2} \cdot \frac{r'_{Bx}}{0.4b_E} \quad , \quad r_{Bx,2y} = \frac{1}{2} \cdot \frac{r'_{Bx}}{0.6b_E} \quad . \quad (12)$$

Using (5)-(12) all elements of the base resistor network are given. Additional external model elements, e.g. external junction and oxide capacitances, can be calculated from the dimensions of the six transistor elements and have to be connected to the corresponding nodes.

The determination of all elements of the 6TM is simplified, if a semi-physical parameter determination program like TRADICA is already available, which allows to calculate the transistor model parameters for arbitrary transistor geometries from area- and length-specific basic data (like, e.g., specific resistances and capacitances) [6].

3 Verification of the 6-Transistor Model by Simulation

The 6TM was verified by comparison with the accurate QDTM, especially with respect to the onset of lateral instability. For this, transistors with quite different emitter geometries were investigated for different driving conditions. In the following, only few simulation examples can be presented, which are restricted to $l_E \gg b_E$, current-independent multiplication factor M and negligible emitter resistance. Moreover, the SPICE Gummel-Poon model was used for the internal transistor elements but extended by the avalanche current source mentioned before.

The simulations as well as the experimental results in Section 4 are based on a self-aligned double-polysilicon UHF technology of ATMEL Wireless & Microcontrollers, Heilbronn. The transistors under investigation have an emitter size of $A_E = 0.75 \mu m \times 20 \mu m$ and a surrounding low-ohmic poly-Si base contact. If not otherwise mentioned the version with selectively implanted collector (SIC) is used.

3.1 Transistor Output Characteristics

Figs. 2 and 3 show the d.c. output characteristics $I_C(V_{CE})$ for $V_{BE} = const.$ and $I_C(V_{CB})$ for $I_E = const.$, respectively, simulated with the 6TM and QDTM. An excellent agreement of both transistor models is observed up to the onset of instability (dotted line), i.e. the limit of the usable operating range. The simulated base currents and especially their critical values I_{Bcrit} (which determine the onset of instabilities) agree also very well but are not shown here. These results justify

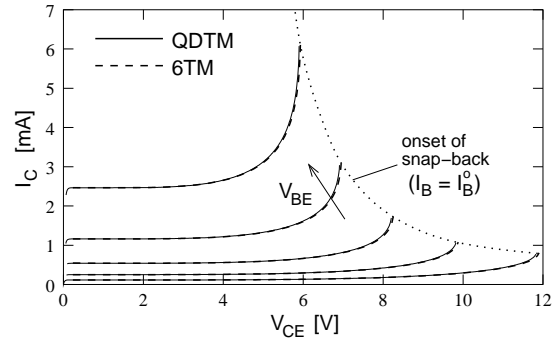


Fig. 2: Output characteristics $I_C(V_{CE})$ in common-emitter configuration with V_{BE} as a parameter – comparison of 6TM and QDTM. The characteristics are hardly distinguishable.

the drastical reduction of the number of transistor elements in the 6TM. It should be pointed out that the modeling fails beyond the dotted line. Therefore, the characteristics beyond this line are not shown here.

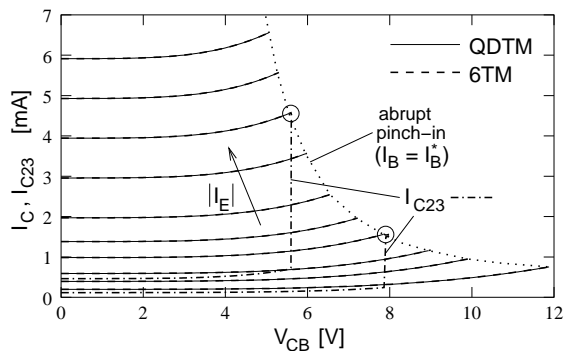


Fig. 3: Output characteristics $I_C(V_{CB})$ in common-base configuration with I_E as a parameter, up to the onset of abrupt pinch-in ($I_B = I_B^*$) – comparison of 6TM and QDTM. (The characteristics are hardly distinguishable.) Moreover, the abrupt increase in the collector current I_{C23} of the central transistor T_{23} of the 6TM is shown for $|I_E| = 1$ mA and 4 mA (dash-dotted lines).

The question arises: how can the loci of instability be detected? For $V_{BE} = const.$ the points of infinite slope and the corresponding onset of snap-back are clearly observable. But if, e.g., the transistor is driven by a constant emitter current, the abrupt pinch-in may result only in relatively small discontinuities in the output characteristics. A more pronounced indication of the onset of instability is the behavior of the base current which, at increasing V_{CB} , suddenly drops to a nearly constant value [2], [3]. However, an abrupt change of the base current can also occur during fast switching of a transistor. Therefore, we recommend to observe the emitter or collector current of the transistor element in the center of the emitter, i.e. T_{23} in the 6TM (Fig. 1), which suddenly takes over nearly the total emitter and collector current as shown in Fig. 3.

3.2 D.C. Characteristics of a Differential Stage

As a further model application, an emitter-coupled differential stage is investigated, which is a frequently used basic stage in high-speed digital circuits (as a current switch) and broad band amplifiers [1]. A simplified circuit diagram is inserted in Fig. 4.

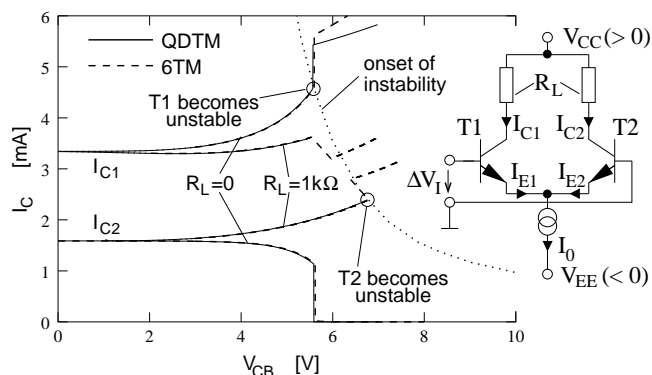


Fig. 4: Output characteristics $I_C(V_{CB})$ of a differential stage with and without ohmic load resistor, showing the onset of instability (dotted line) – comparison of 6TM and QDTM ($I_0 = 5$ mA, $\Delta V_I = 20$ mV).

During the design of such circuits (especially in the case of driver circuits) often the question arises: is the breakdown behavior of the transistors in the transient region of the cir-

cuit more similar to a voltage- or to a current-driven common-base configuration? Fig. 4 shows both collector currents of a differential stage vs. V_{CB} for different loading ($R_L = 1$ k Ω and $R_L = 0$), simulated by use of the 6TM and QDTM, respectively. Again, there is an excellent agreement between both models up to the onset of instability. The simulation results show that the onset of instability (dotted line) equals that of a current driven common-base configuration (i.e. $I_{Bcrit} \approx I_B^*$, cf. Fig. 3) and thus can easily be calculated [3].

For the case $R_L = 0$, the behavior of the collector currents can be explained as follows: Due to the positive input voltage ΔV_I ($|I_{E1}| > |I_{E2}|$) and to the equal multiplication factor M of both transistors, the base current of T1 reaches the critical value I_{Bcrit} ($= I_B^*$) first and thus triggers the onset of instability. Caused by the resulting pinch-in, V_{BE1} drops abruptly [3]. The corresponding drop of V_{BE2} ($\Delta V_I = const.$) switches T2 off so that T1 now carries the total current ($|I_{E1}| = I_0$) and I_{C1} rises abruptly to about MI_0 .

In the case $R_L = 1$ k Ω , the situation has changed: Due to the high voltage drop across R_L , the multiplication factor of T1 is now substantially lower than that of T2. Therefore, despite its lower I_C and $|I_E|$, the base current of T2 reaches the critical value I_B^* first and thus triggers the onset of instability.

3.3 Switching Operation

Up to now only d.c. operation has been discussed. Thus the questions remain: can the good agreement between 6TM and QDTM also be observed for (fast) switching operation and, moreover, is it allowed to switch through the region of d.c. instability (i.e. to cross the line characterizing the onset of abrupt pinch-in) proposed this transient is fast enough?

As an example, a transistor in common-base configuration is investigated. From a small bias current I_1 , the driving emitter current switches to a much higher value I_2 ($= 100 I_1$) and vice versa within a rise and fall time $t_s = 1$ ns. Fig. 5 shows the response of the base current³ simulated by both the 6TM and the QDTM for two collector supply voltages V_0 , which differ by 0.6 V only. In both cases the load line ($R_L = 500$ Ω) passes the region of d.c. instability. For the stable transients the results of QDTM and 6TM agree very well and are hardly distinguishable. In the unstable case, the i_B plots of both models are different beyond the onset of instability, but this is not relevant for the designer. For him it is important that both models indicate unstable behavior and thus show the limit of reliable operation.

Numerous simulations confirmed the expected behavior:

- The probability for instability during switching is reduced with reduced switching time and vice versa.
- Instability during switching-on becomes more probably for a capacitive and less probably for an inductive load, as the penetration depth into the region of d.c. instability is increased or reduced, respectively. For switching-off the opposite behavior is observed.

4 Experimental Results

In [2], [3] the transistor output characteristics and the onset of instability were measured for $V_{BE} = const.$ and $I_E = const.$,

³Here, the base current is preferred since instabilities are easier to detect than in the plot of the collector current.

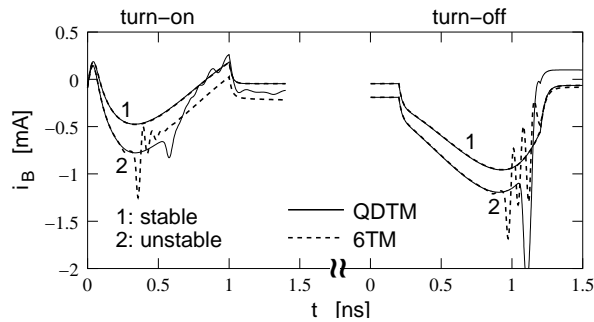


Fig. 5: Transient response of the base current in a common-base configuration – comparison of 6TM and QDTM. The supply voltages V_0 for the stable (curve 1) and unstable transient (curve 2) are 8.2 V and 8.8 V, respectively.

respectively, and compared with the QDTM simulation results. In all cases good agreement was obtained. Due to the results in Figs. 2 and 3, good agreement with measurements can also be stated for the 6TM simulation. Next, the 6TM simulation results for the d.c. characteristics of a differential stage and for the switching operation of a single transistor are verified by measurements.

4.1 D.C. Characteristics of a Differential Stage

Fig. 6 shows the measured collector currents I_{C1} , I_{C2} of a differential stage vs. V_{CB} for $R_L = 1$ k Ω . For comparison the measured characteristics of a common-base configuration at $I_E = \text{const.}$ and the resulting limiting curve (dotted line) are inserted.

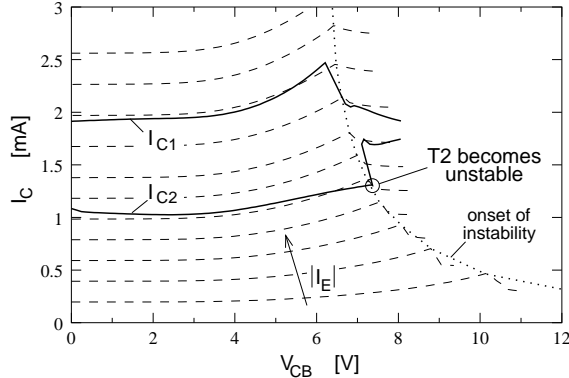


Fig. 6: Measured output characteristics of a differential stage with $R_L = 1$ k Ω , $I_0 = 3$ mA and $\Delta V_I = 20$ mV (solid lines), compared to the output characteristics of a common-base configuration at $I_E = \text{const.}$ (dashed lines).

Due to the chosen load resistance and source current, the transistor T2 with the lower emitter and collector current first reaches the critical base current $I_{Bcrit} (\approx I_B^*)$, i.e. its $I_C(V_{CB})$ -characteristic reaches the limiting curve first, and thus becomes unstable. As a consequence, the collector current of this transistor (I_{C2}) is increased while that of the other transistor (I_{C1}) is reduced. This agrees with the simulation results in Fig. 4.

4.2 Switching Operation

Fig. 7a,b shows the measured base currents of a SIC and a non-SIC transistor, respectively, for stable and unstable turn-on transients. Deviating from the simulation conditions

of Fig. 5, the driving source has now an increased rise time of $t_s \approx 2$ ns and an impedance of 200 Ω only, and the load resistance is increased to $R_L = 1$ k Ω . Despite this different conditions, the basic response of i_B looks similar to the simulated one in Fig. 5 (left-hand side). A comparison of the

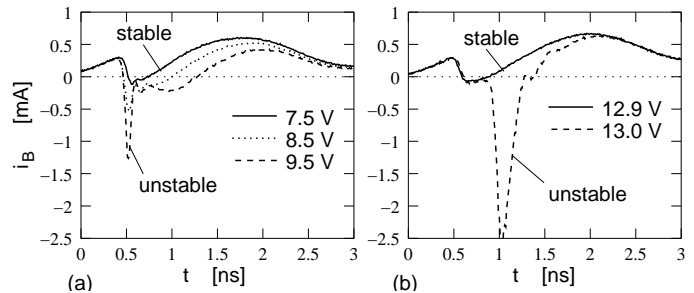


Fig. 7: Measured base current during the turn-on transient of a transistor in common-base configuration showing the change from stable to unstable operation by increasing the collector supply voltage V_0 . (a) with SIC, (b) without SIC.

results in Fig. 7a and b confirms the statement in [3]: The change from a stable transient to an unstable transient in the deep breakdown region is much more abrupt in the case of non-SIC compared to SIC transistors. (In Fig. 7b there is only a difference of 0.1 V in V_0 between both transients.) This is because in non-SIC transistors a vertical instability occurs immediately after pinch-in while in SIC transistors this effect is delayed by the current dependence of the multiplication factor M combined with the increasing influence of the emitter resistance. All these effects are considered in an extended model [4] but not in the simulations of Section 4.

5 Conclusions

In conclusion, a 6-transistor model has been presented which proved to be well suited to consider avalanche-breakdown effects in the simulation of Si bipolar circuits, even under transient conditions. Thus, the limit of reliable operation can be clearly detected. The model is physics-based and scalable for arbitrary transistor geometries.

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