Test Structures and a new approach for fast and accurate extraction of specific NPN parameters.

Qualified test structures and principle approaches for physics based parameter extraction

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Introduction

If you know all

- transistor layout measures, vertical transistor geometry and transistor configurations,
- absolute, geometry independent (NF, VAF, VAR ... ) and specific parameters (is_a, is_p, cj_a, cj_p, re_a, rb_sh, rb_l, ...)
- correct parameter scaling rules

\[
\text{IS} = \text{is}_a \times \text{AREA} + \text{is}_p \times \text{PERIE}, \\
\text{CJ} = \text{cj}_a \times \text{AREA} + \text{cj}_p \times \text{PERIE}, \\
\text{tf0} = \text{tf0} \times (1 + \text{aw}_1 \times \text{WE} + \text{aw}_2 \times \text{WE}^2) \times (1 + \text{al}_1 \times \text{LE} + \text{al}_2 \times \text{LE}^2) \quad \text{or} \quad \text{tf0} = \text{tf0}_a \times (1 + \text{a}_1 \times \text{PERIE} / \text{AREA})
\]

you can calculate parameter set for arbitrary device geometry’s using parameter set calculation scripts or tools like TRADICA [1]

How can I extract fastest model parameters for extensive transistor libraries without performing a lot of single transistor parameter extractions ?

Perform direct extraction of specific parameters !!
Introduction:

- Parameter extraction is much easier when external transistor components can be extracted accurately on simple test structures. Than parameter extraction must only be performed and optimized on the intrinsic transistor parameters.

- Important external parameters are here REX, RBX, RBL, RBI, RCX, CEOX, CJEP, CJEAL, CCOX, CJCX, CJCI, CSOX, CJSI, CJSI

- It will be very advantageous when measured characteristics from different device geometry’s can be processed directly in such a way that these measured characteristics are transformed into area specific and perimeter specific characteristics **before** beginning parameter extraction. If this data transformation is possible:
  - “Transformed” specific data set should already represents best fit to measured characteristics from all measured characteristics from different device geometry’s.
  - Parameter extraction must only be performed on two data sets: Area-specific and perimeter specific data sets.
Physics based subcircuit building
(external subcircuit components)

Fig. 3: SiGe NPN Cross-Section.
SGP Subcircuit Model: NPN Transistor

Physics based SGP transistor subcircuit model:

Base resistance under spacer and Mono-SiGe

Parasitic Substrate Transistor QP

Main Transistor QI

Fig. 1: Subcircuit Model for SGP-Model Parameter Extraction.
HICUM Model: NPN Transistor

**Fig. 2:** Subcircuit model implemented in HICUM.
Technological Cross Section of a Vertical PNP Transistor

Fig. 4: VPNP Cross-Section.

**Basic Requirements:**

- Fast complementary bipolar transistor
- High breakdown voltage
- Relative high current density
- Triple-well isolation
3-Transistor-Subcircuit Model for a Vertical PNP

SGP Circuit Deck

.SUBCKT VPNP 1=C 2=B 3=E 4=S 5=NP
RE 3 33 10
RBEX 2 22 10
RCEX 1 11 10
RNP 5 55 11
Q1 11 22 33 33 MAIN AREA=1
Q2 55 11 22 22 PAR1 AREA=1
Q3 4 55 11 11 PAR2 AREA=1
.MODEL MAIN PNP
+ IS = 1E-16
+ ...
.MODEL PAR1 NPN
+ IS = 1E-17
+ ...
.MODEL PAR2 PNP
+ IS = 1E-15
+ ...
.ENDS

Figure 5: Equivalent Three-Transistor Subcircuit Model used for VPNP-Transistor Modeling
Test structure planning should be based on a geometry and configuration tables.

The following test structures are required:

- DC test structures for I(V) characteristics
- C(V) test structures for junction capacitance characterization.
- S-parameter test structures for AC characterization.
- Resistor test structures for NPN resistance parameter extraction.
DC Test Structures for Single Transistor
I(V)-Characterization

- Measurement of all important DC characteristics of NPN’s at single transistors with different device length and width
  - 4-5 different device length
  - 4-5 different emitter width
  - Different transistor configurations

Figure: Layout of a typical single transistor test structure for DC measurements
Improved DC Test Structures for Single Transistor I(V)-Characterization

- Using “On-Chip-Force-Sense Test Structures” eliminates pad contact and wiring resistances in I(V)-characteristics.
- Important for power device characterization
- Accurate emitter resistance measurement at low emitter resistance are possible using “Modified Reflyback Method” [2]
C(V) Test Structures for NPN Junction and Oxide Capacitance Extraction

- Accurate junction and oxide capacitance characterization is possible if well designed multi transistor test structures are available.
- Accurate designed OPEN test structures are mandatory for on wafer calibration of the precision LCR Meter.
- Different WE and LE geometry’s allows an precise separation of internal and external capacitance contributions.
- Oxide overlap capacitance’s can be calculated using 2D capacitance calculation equations:

\[
c_{OX} = \varepsilon_0 \varepsilon_{ox} \left[ 1.15 \frac{W}{h} + 2.8 \left( \frac{t}{h} \right)^{0.222} \right]
\]

\[
C_j = C_{meas} - 0.5 \cdot PERI \cdot C_{OX}
\]
Measurement of all C(V) junction capacitance characteristics of NPN’s at multi transistor arrays for:

- 4-5 different device length and (e.g. CBE, CBEBBC)
- 4-5 different emitter width (e.g. CBEBBC)
- a long and short transistor of all transistor configurations

Typical transistor configurations:
C-E-B
C-B-E
C-B-E-B
C-B-E-C
C-B-E-B-C
C-B-E-B-E-B-C

Typical device length flutes:
1 • we_{min}:
1, 2, 3, 6, 10 le_{min}
2 • we_{min}:
1, 2, 3, 6, 10 le_{min}

Typical device width flute:
10 • le_{min}:
0.8/1.0/1.2/1.5/2.0/3.0/ • we_{min}

Figure: Right structure: Layout of a typical multi transistor arrays for junction capacitance and low injection I(V)-measurements. On the left side the gadget calibration structure is shown. A correctly designed OPEN test structure is strictly required for correct calibration of precision capacitance measurement bridge before measuring the device array. So inter-digital and coupling capacitance from transistor wiring can be stripped of.
C(V) Test Structures for NPN Junction and Oxide Capacitance Extraction

CBC Perimeter structure of typical NPN transistors is complicated: Using width flutes of long transistors (LE>10LE_{min}) allows accurate determination of length specific total external base capacitance c_{jc,per}.
C(V) Test Structures for NPN Junction and Oxide Capacitance Extraction

Results: Measured (red) BE and BC junction capacitance’s and recalculated (blue) BE and BC junction capacitance’s for a lot of different geometry’s

Figure: Measured (red) and recalculated (blue) B7HFC base-emitter (CBE) capacitance’s from different device geometry’s and configurations. For recalculation the extracted specific CBE capacitance values cje_a, cje_p ceox_p ceox_edge were used. Measurement temperature was 25°C.

Figure: Measured (red) and recalculated (blue) B7HFC base-collector (CBC) capacitance’s from different device geometry’s and configurations. For recalculation the extracted specific CBE capacitance values cjc_a, cjc_p, cjc_edge, ccox_p ccox_edge were used. Measurement temperature was 25°C.
C(V) Test Structures for Collector-Substrate Junction and Trench Capacitance Extraction

- Long buried layer structures (BLCAP) are designed. Length le_b is fix. Design variable is wi_bl.
- Several buried layer structures beginning from minimum buried layer width are designed. 3 to 5 different P/A-ratios are required.
- Between two bl strips always a substrate contact strip must be established to have good substrate contact.
- Spacing w_{pw} between trench/bl and substrate pwell can be varied.
- OPEN Structure must exclude metallization on top of the bl areas to avoid therein additional CS-capacitance which is not present in the BLCAP structures.
Total base resistance is one of the key parameters for modern High Frequency NPN’s.

- important to achieve good input impedance matching.
- limits Noise figure $\text{NF}_{\text{min}}$.
- limits $F_{\text{max}}$.

Accurate measurement and modeling of base resistance is particular important!

Base resistance calculation for arbitrary emitter geometry:

$$R_{bb} = R_{bx} + R_{bx} \cdot \Phi(V_{bc}) + R_{bi} \cdot \psi(we_{\text{eff}}, le_{\text{eff}}, V_{be}, V_{bc})$$

$$R_{bx} = r_{\text{link}} \cdot \frac{1}{2n_{E} \cdot (we_{\text{eff}} + le_{\text{eff}})}$$

$$R_{bi} = r_{\text{pinch}} \cdot \frac{gi \cdot we_{\text{eff}}}{n_{E} \cdot le_{\text{eff}}}$$

$$gi = \frac{1}{12} \left( \frac{1}{12} - \frac{1}{28.6} \right) \frac{we_{\text{eff}}}{le_{\text{eff}}}$$
**Basic measurement idea**

**Principal Measurement Idea:** Measuring the lateral $I_{B12}/V_{B12}$ characteristic between two base nodes of ring transistors with double base contacts over base-emitter and base-collector bias.

\[
I_{B12} = \frac{V_{B1} - V_{B2}}{2 \cdot R_{link} + R_{pinch}}
\]

\[
V_{B1} - V_{B2} = 10mV
\]
Layout of appropriate test structures for DC base resistance measurements

- Enclosed structure to ensure current flow under emitter:

Principal layout structure of typical ring transistors. Layout parameters are \( w_e \) and \( l_{b\text{con}} \).
Correction for current spreading and calculation of normalized terminal currents

- **Correction for current spreading in the device heads**

Subtracting terminal current of a short structure from terminal currents of a long structure enables correct current spreading correction. The total terminal currents are calculated by:

\[
I_E = I_E^h + 2 \cdot l b_{con} \cdot i_E \\
I_{B1} = I_{B1}^h + 2 \cdot l b_{con} \cdot i_{B1} \\
I_{B2} = I_{B2}^h + 2 \cdot l b_{con} \cdot i_{B2} \\
I_C = I_C^h + 2 \cdot l b_{con} \cdot i_C
\]

Total internal base current is given by:

\[
I_B = I_{B1} + I_{B2} \\
= I_{B1}^h + I_{B2}^h + 2 \cdot l b_{con} \cdot (i_{B1} + i_{B2})
\]
Correction for current spreading and calculation of normalized terminal currents

**Calculation of length specific device currents** $i_E, i_{B1}, i_{B2}, i_C$ and $i_{B12}$

By using two structures with different length $l_{b_{con}}$, the corner and head current rates can be canceled and length specific terminal currents can be calculated.

\[ i_E = \frac{I_E^l - I_E^s}{\Delta l_{b_{con}}} \]
\[ i_{B1} = \frac{I_{B1}^l - I_{B1}^s}{\Delta l_{b_{con}}} \]
\[ i_{B2} = \frac{I_{B2}^l - I_{B2}^s}{\Delta l_{b_{con}}} \]
\[ i_C = \frac{I_C^l - I_C^s}{\Delta l_{b_{con}}} \]

\[ i_B = i_{B1} + i_{B2} = -i_E - i_C \]

where:

\[ \Delta l_{b_{con}} = 2 \cdot (l_{b_{con}}^l - l_{b_{con}}^s) \]

⇒ Lateral base current from node B1 to node B2 per μm length:

\[ i_{B12} = 0.5 \cdot (i_{B2} - i_{B1} - i_B) = 0.5 \cdot (i_{B2} - i_{B1} + i_E + i_C) \]

\[ i_B = -i_E - i_C \]
Results and Measurement Conditions

Figure 1: Bias dependence of the base pinch resistance (in Ω/square, red curves) for RF-NPN’s in B7HF. These base resistance parameters are extracted over base emitter bias $V_{BE}$ = +1.0V to -1.0V for five different base collector voltages $V_{BC}$ = -0.5V, 0.0V, +0.5V, 1.0V, 1.5V. Wafer temperature during measurement was T= 25°C.

Inputs:
- $V_E = +1.0 \ldots -0.9V$ (1st sweep)
- $V_{B1} = -10mV$
- $V_{B2} = +10mV$
- $V_C = -0.5V, 0.0V, +0.5V \ldots +V_{cmax}$ (2nd sweep)
- $V_S = V_C$

Outputs:
- $I_E$
- $I_{B1}$
- $I_{B2}$
- $I_C$
- $I_S$

Applied to six different devices:
Test Structures for Fast and Direct Extraction of External Base and External Collector Series Resistance Parameters

- Simple NPN resistor structures can be derived from transistor layouts with CBEBC configuration (1)
- CBEBC transistor layout PCELL with scalable emitter width WE and length LE is modified in such a way that no emitter window will be processed (2)!
- Chains off N serial switched devices are realized on test chip.
- Chains with several WE- and LE-geometry’s are realized.

\[
R_{CX12} = \frac{V_{C12}}{N \cdot I_{C12}} \quad R_{BEX12} = \frac{V_{B12}}{N \cdot I_{B12}}
\]

Legend:
- Oxide
- Nitride p-doped
- Nitride n-doped
- Tungsten plug
- BPSG
- Poly
- Metal stack

RBX & RCX RESISTORS

Only EPI is between Emitter and buried layer (HV-NPN)

CBEBC-Transistor
Test Structures for Fast and Direct Extraction of External Base and External Collector Series Resistance Parameters

- Extract $R_{CEX,meas}$ from measured $I_{12}(V_{12})$-characteristics $R_{12} = V_{12}/I_{12}$
- Calculate $R_{CEX,calc}$ using simple equation approaches for total buried layer and collector contact resistance calculation.
- Sheet resistances, length specific contact and edge corrections can easily be extracted fitting these calculation equations $R_{CEX,calc}$ to measured resistance values $R_{CEX,meas}$ by optimizing to specific resistance values.
- Pre-condition: Several highly different collector geometry's are required.

$$
R_{con} = \frac{rh\_con \cdot rl\_con}{rl\_con + le\_con \cdot rh\_con}
$$

$$
R_{12l} = rsh\_bl \cdot \frac{wl\_bl\_12}{le\_con}
$$

$$
R_{12h} = rsh\_bl \cdot \frac{wl\_bl\_12}{2 \cdot d\_con} + R_{edge}
$$

$$
R_{ges} = 2 \cdot R_{con} + \frac{R_{12l} \cdot R_{12h}}{R_{12l} + R_{12h}}
$$

To be optimized
Test Structures for Fast and Direct Extraction of External Base and External Collector Series Resistance Parameters

- Extract $R_{BEX,meas}$ from measured $I_{12}(V_{12})$-characteristics $R_{12} = V_{12}/I_{12}$
- Calculate $R_{BEX,calc}$ using simple equation approaches for total base poly and base contact resistance calculation.
- Sheet resistances, length specific contact and edge corrections are extracted fitting these calculation equations $R_{BEX,calc}$ to measured resistance values $R_{BEX,meas}$ by optimizing to specific resistance values.
- Pre-condition: Several highly different base-poly geometry’s are required.

\[
R_{con} = \frac{r_{h} \cdot d_{con}}{r_{l} + l_{con} \cdot r_{h} \cdot d_{con}}
\]

\[
R_{sal,h} = \frac{r_{sh} \cdot w_{i} \cdot d_{sal}}{l_{con}} + 0.5 \cdot r_{sal,edge}
\]

\[
R_{sal} = \frac{R_{sal,1} \cdot R_{sal,1}}{R_{sal,1} + R_{sal}}
\]

\[
R_{pm} = \frac{r_{l} \cdot d_{pm}}{l_{con} + 2 \cdot d_{con}}
\]

\[
R_{12} = \frac{r_{sh} \cdot w_{i} \cdot d_{sal}}{l_{con} + 2 \cdot d_{con}}
\]

\[
R_{ges} = 2 \cdot R_{con} + 2 \cdot R_{sal} + 2 \cdot R_{pm} + R_{12}
\]
For point collector measurement structure. Current is forced from terminal C1 to C4. Voltage is sensed at port C2, C3 and C4

\[ R_{\text{con}} = \frac{r_{\text{h con}} \cdot r_{\text{l con}}}{r_{\text{l con}} + l_{\text{e con}} \cdot r_{\text{h con}}} \]

\[ R_{12,h} = r_{\text{sh bl}} \cdot \frac{w_{\text{i bl12}}}{2 \cdot d_{\text{con}}} + R_{\text{edge}} \]

\[ R_{12,f} = r_{\text{sh bl}} \cdot \frac{w_{\text{i bl12}}}{l_{\text{e con}}} \]

\[ R_{12} = \frac{R_{12,f} \cdot R_{12,h}}{R_{12,f} + R_{12,h}} \]

\[ R_{23} = r_{\text{sh bl}} \cdot \frac{w_{\text{i bl23}}}{l_{\text{e con}} + 2 \cdot d_{\text{con}}} \]

\[ R_{cc} = r_{\text{sh bl}} \cdot \frac{w_{\text{i con}}}{l_{\text{e con}} + 2 \cdot d_{\text{con}}} \]

\[ V_{C2} = (1 \cdot R_{\text{con}} + 1 \cdot R_{12} + 0.5 \cdot R_{cc}) \cdot I_{14} \]

\[ V_{C3} = (1 \cdot R_{\text{con}} + 1 \cdot R_{12} + 1.5 \cdot R_{cc} + R_{23}) \cdot I_{14} \]

\[ V_{C4} = (2 \cdot R_{\text{con}} + 2 \cdot R_{12} + 2 \cdot R_{cc} + R_{23}) \cdot I_{14} \]

To be optimized
Fore Point Collector Measurement Structure for Extraction of Collector Series Resistance Parameters

- Cross section of a For Point Collector Resistance structure. Current is forced from terminal C1 to C4. Voltage is sensed at port C2, C3 and C4

- Measurement settings:

  Inputs:
  \[ V_{C1}=0.0 \text{V} \quad I_{C2}=0.0 \text{A} \quad I_{C3}=0.0 \text{A} \quad I_{C4}=0.5 \ldots 5 \text{mA} \]

  Outputs:
  \[ I_{C1} \quad V_{C2} \quad V_{C3} \quad V_{C4} \]

- Current densities must be chosen so that self-heating in the device structure is negligible.

Legend:
- Oxide
- Nitride
- Tungsten plug
- BPSG
- Poly
- Metal stack
- p-doped
- n-doped
New Approach for Direct Extraction of Geometry-Specific NPN-Parameters

Principal Idea:

- Measuring DC- and C(V)-characteristics from a devices ensemble with different emitter geometry’s (≥3-5 different emitter length LE and ≥ 4-5 different emitter width WE).

- Transformation of measured characteristics from device X (here called Y_X(V) ) into area and perimeter specific characteristics e.g.

  \[
  Y_X(V_i) = x_a(V_i) \cdot \text{AREA}_X + x_p(V_i) \cdot \text{PERI}_X + X_{X,off}
  \]  

  \[
  \frac{Y_X(V_i) - X_{X,off}}{\text{AREA}_X} = x_a(V_i) + x_p(V_i) \cdot \frac{\text{PERI}_X}{\text{AREA}_X}
  \]  

- Performing multi linear regression on (2) for each bias point V_i. Slope leads to perimeter specific data set x_p(V_i) and intercept point leads to area specific data x_a(V_i).

- Perform parameter extraction only on the transformed data plots x_a(V) and x_p(V). These data sets are representing specific characteristics e.g. CJ_A(V_j), CJ_P(V_j), IC(V_{BE},V_{BC}), IBE(V_{BE}) IBC(V_{BC}), ICS(V_{CS}), IS(V_{BE}), ...

  \Rightarrow Only\ area\ and\ perimeter\ specific\ parameters\ are\ extracted
New Approach for Direct Extraction of Geometry-Specific NPN-Parameters

Example: Extraction of Junction capacitance parameters:

\[ C_j = c_{j, \text{area}} \cdot \text{AREA}_i + c_{j, \text{peri}} \cdot \text{PERI}_i + \text{COX} \]

\[ \frac{C_j - \text{COX}}{\text{AREA}_i} = c_{j, \text{area}} + c_{j, \text{peri}} \frac{\text{PERI}_i}{\text{AREA}_i} \]

Parameter extraction is performed only on these two characteristics:

Results:
- \( c_{j_a}, v_{j_a}, m_{j_a} \)
- \( c_{j_p}, v_{j_p}, m_{j_p} \)
New Approach for Direct Extraction of Geometry-Specific NPN-Parameters

Figure: “Measured” and calculated area and perimeter specific collector current. For calculation the extracted specific transfer current values is_a, is_p, nf_a, nf_p VAF and VAR were used. Measurement temperature was 25°C.

Figure: “Measured” and calculated area and perimeter specific base current. For calculation the extracted specific base current values ibe_a, ibe_p, nbe_a, nbe_p were used. Measurement temperature was 25°C.
Figure: “Measured” and calculated **specific** base-emitter area and perimeter (CBE) capacitance’s for B8HF. For calculation the extracted specific CBE capacitance values $c_{je\_a}$, $v_{je\_a}$, $m_{je\_a}$ and $c_{je\_p}$, $v_{je\_p}$, $m_{je\_p}$, $c_{eo\_p}$ $c_{eo\_edge}$ were used. Measurement temperature was 25°C.
**New Approach for Direct Extraction of Geometry-Specific NPN-Parameters**

### Advantages:
- Best fit to measured data is implicitly given.
- Required measurement data processing is easy to implement.
- Single transistor parameter extraction is needed only for very few edge devices to extract geometry independent parameters.
- Only the specific device characteristics are taken for parameter extraction.
- Much lower effort for parameter extraction because there is no need for extensive single transistor parameter extraction.

### Requirements:
- Scalability and scaling rules for device characteristics.
- Device characteristics must be measured for all devices at the same voltage or current bias points.
- Availability of enough device geometry’s.
- Availability of highly different device geometry’s.
- Accurate measurement data with little measurement noise.
Summary

- All of the required external NPN parameters can be extracted with few efforts using intelligent test structures.

- Carefully designed multi-transistor capacitance measurement structures enables very easy and accurate extraction of all specific junction capacitance parameters without performing cold s-parameter measurements.

- Using the presented simple test structures in inline measurement setups (PCM) will lead to higher accuracy in determining important NPN parameters and will give you excellent parameter statistics.

- Reducing measured data from a lot of different device geometry’s as per description directly into area, perimeter and sheet specific characteristics saves
  - plenty of parameter extraction work,
  - gives you automatically best fit to measurement data base.
References

[1] M. Schroeter. „TRADICA. An integrated modeling tool linking process and circuit
design“. Model Parameter Generation and Sizing of Integrated Bipolar Transistors.