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Bipolar vs. MOS

“Using SiGe in a CMOS World”

Bipolar Arbeitskreis

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Contents BJT vs. MOST

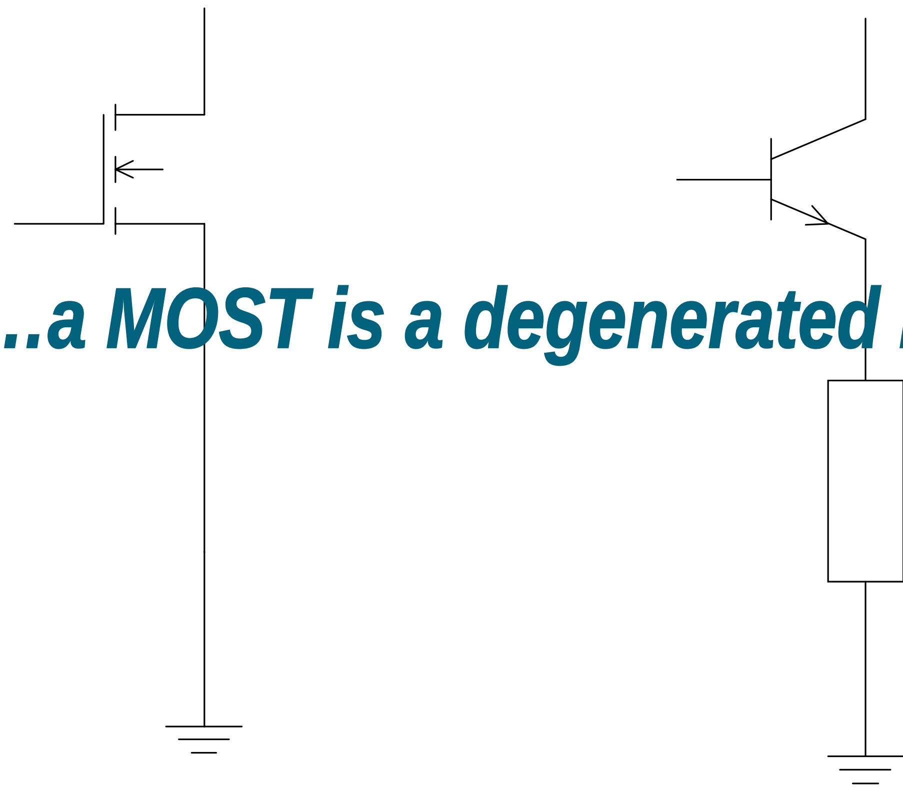
Tables: „Balance sheets“ (RF biased)

Equations: Gain, speed, noise

Curves: transit frequency, noise figure, breakdown voltage

Application: 2.4GHz transceiver – BiCMOS „redefined“

Provocative...



...a MOST is a degenerated BJT...

Basics

MOS:

* surface device
* majority carriers
* voltage driven
* drift current (= faster...)
* saturation region
* linear/triode region
* square-law I-V characteristics
  (linear I-V is also possible)
* low transconductance (≈ 7x ID -M.I.)
* high (capacitive) input impedance (0.1~1pF)
* no DC input current

Bipolar (SiGe):

* bulk device
* minority carriers
* current driven
* diffusion current (+ drift)
* forward active region
* saturation region - not for the fainthearted!
* exponential I-V characteristics
* high transconductance (≈ 40x IC)
* low input impedance (1~10kΩ)
* base current

BJT vs. MOS: Table (1)

Param.	Description	Related Block Spec	BJT vs. MOS	Remarks	
				BJT (S35)	CMOS (RF-CMOS 0.18u, 0.13u, ...)
vn_1/f	Flicker (low frequency) Noise	sensitivity	+++++	Bulk device	Surface device – becomes worse for smaller device geometries
Voffset	Input offset voltage	resolution, sensitivity	+++++	~ 0.1mV - due to higher gm, VBE determined by doping	1~2mV, VTH determined by geometry and doping
VA *	Early voltage -> CS Zout -> (LF) V/V gain	gain	++++	SiGe has very high Early voltage (100V)	Gets worse with smaller geometries
gm	Transconductance (V/I) gain	gain, speed, current consumption	+++	Exponential V/I curve gm≈40*IC	Square-low V/I curve: gm≈7*ID (max. 30*ID – weak inversion)
vnth_in	Input Thermal Noise	sensitivity (range)	+++	Due to higher gm	
Vmax *	Max. Operating voltage	output power	+++	BVCEO < 2.0V (HS), 4.5V (HV) BVCES < 7V (HS), 10V (HV)	VDS < 1.8V, 1.3V, …
Zout	Output impedance (driving capability)	current consumption, output power	+++	Zout ≈ 1/gm is much smaller	
ft *	Transit frequency	speed, current consumption	++	~ gm	~ gm, MOS can reach similar ft however, requires higher IDS and VDS
VminRF *	Min. Operating voltage for RF applications	speed, output power	++		VDS > VCE for high speed

* SiGe specific advantage

BJT vs. MOS: Table (2)

Param.	Description	Related Block Spec	BJT vs. MOS	Remarks	
				BJT (S35)	CMOS (RF-CMOS 0.18u, 0.13u, ...)
ESD	Electrostatic Discharge Performance	QA	++	More robust	Requires substantial additional circuitry
Zmatch	Impedance & Noise Matching	current consumption, BOM	+	Inherent bipolar impedances are closer to 50-ohm	Can be overcome with additional (external) components.
Area	Device area	price	+/-		
IIP3	Linearity	selectivity	+/-	Exponential V/I – can be overcome using circuit techniques + HF mainly dominated by parasitics which mitigate the effect	Square-law V/I
Vmin	Min. Operating voltage for non-RF applications	current consumption	- -	VBE (0.8V) > VTH (0.5V)	Low VTH options
Iin	DC Input Current	leakage, input impedance	- -	Base current ~ IC/100	No gate current
Zon	Switch ON-impedance	complexity	- - - -	Should not be used as switch (saturation region)	Linear region ideal for RF switches

BJT vs. MOS: Basic equations

MOS: | **Bipolar:**

Current::

$$I_D = \frac{\mu C_{ox}}{2n} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \frac{V_{DS}}{VA \cdot L})$$

$$I_C = I_S \cdot e^{\frac{V_{BE}}{U_T}} \cdot (1 + \frac{V_{CE}}{VA})$$

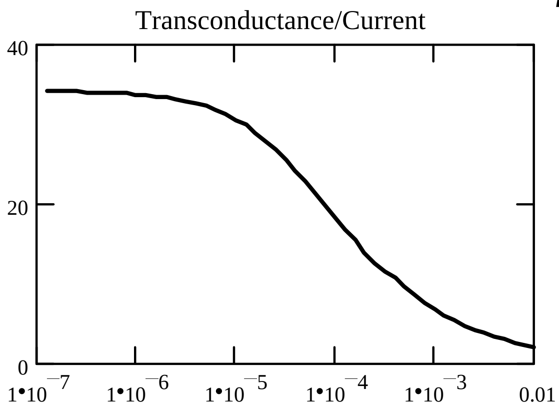
Transconductance:

$$g_m = \frac{2 I_D}{V_{GS} - V_T}$$

$$g_m = \frac{I_C}{U_T}$$

Moderate and weak inversion:

$$g_m = \frac{I_D}{n \cdot U_T \sqrt{1 + \frac{I_D}{\mu C_{ox} \cdot \frac{W}{L} 2 \cdot U_T^{\,2}}}}$$



Weak inversion factor: (1.1~1.3)

$$n = 1 + \frac{C_d}{C_{ox}}$$

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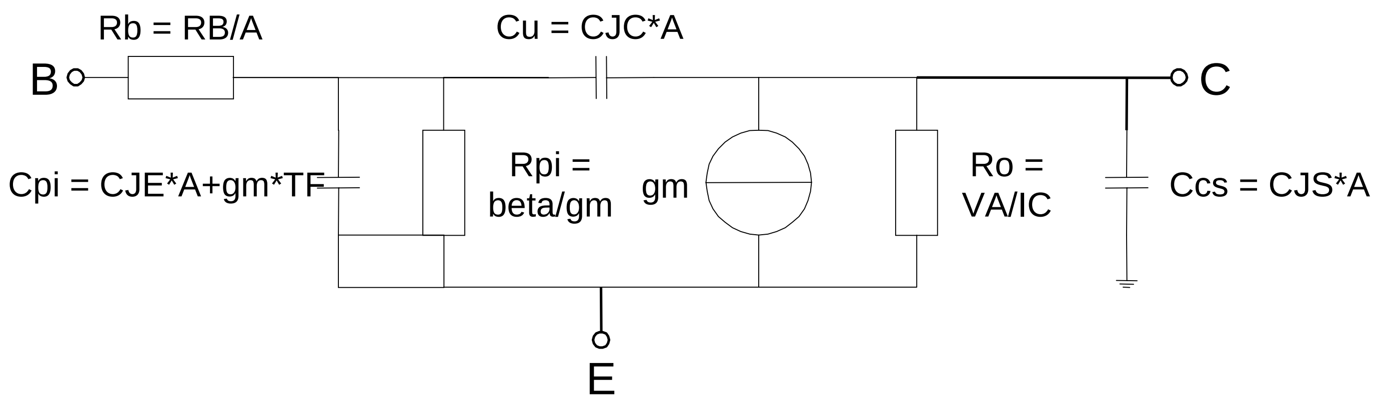
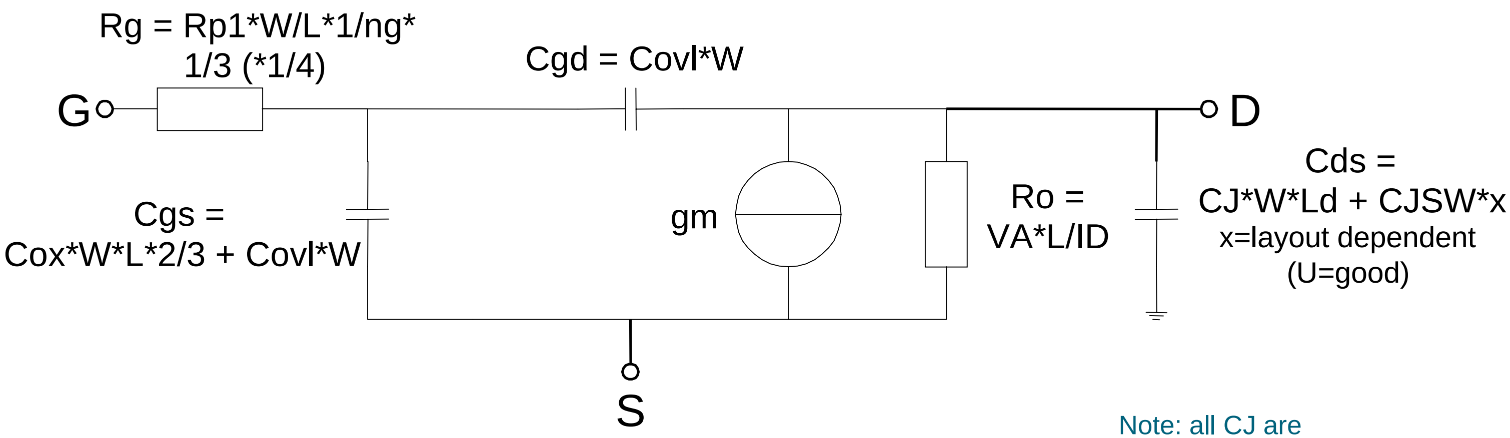
BJT vs. MOS: Small signal models

Bipolar:



MOS:



Observe: contrary effect of area on input resistance

Note: all CJ are voltage dependent

BJT vs. MOS: Speed performance equations

MOS:

Unity current gain frequency:

$$f_T = \frac{gm}{2\pi \cdot (C_{gs} + C_{gd})}$$

$$\Rightarrow f_T \propto \frac{1}{a + W * b}$$

for fixed VGS

Unity power gain frequency:

$$f_{\max} \approx \sqrt{\frac{f_T}{8\pi \cdot R_G \cdot C_{gd}}}$$

$$\Rightarrow f_{\max} \propto \sqrt{\frac{1}{a * W^2 L + b * W^3 L}}$$

for fixed VGS

Bipolar:

$$f_T = \frac{gm}{2\pi \cdot (C_\pi + C_\mu)}$$

$\Rightarrow f_T$ dependent on A for small I_C

$$f_{\max} \approx \sqrt{\frac{f_T}{8\pi \cdot R_B \cdot C_\mu}}$$

$\Rightarrow f_{max}$ dependent on A for small I_C

BJT vs. MOS: Equivalent input noise - DC

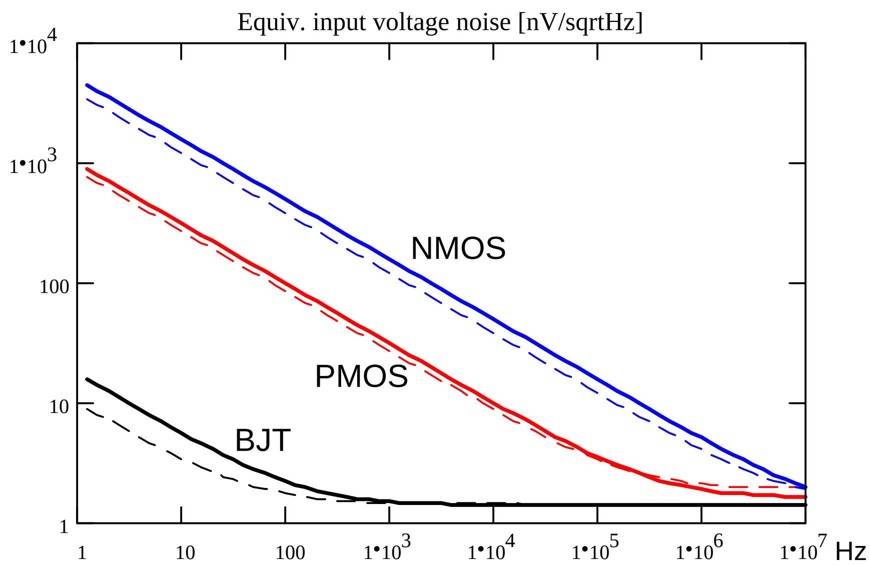
MOS:

Thermal:

$$v_{n,T}^{\ 2} = 4kT(R_G + \frac{2}{3g_m})$$

Flicker:

$$v_{n,f}^{\ 2} = \frac{KF \cdot I_D^{\ AF}}{L^2 \cdot C_{ox} \cdot f \cdot g_m^{\ 2}}$$



Bipolar:

$$v_{n,T}^{\ 2} = 4kT(R_B + \frac{1}{2g_m})$$

source

$$v_{n,f}^{\ 2} = i_{n,f}^{\ 2} \cdot R_S^{\ 2}$$

$$= (\frac{KF \cdot I_B^{\ AF}}{f} + 2 \cdot q \cdot I_B) \cdot R_S^{\ 2}$$

BJT vs. MOS: Equivalent input noise - RF

For f > fT/100:

Introduce $\beta(f) \approx \frac{f_T}{f}$

correlated

MOS:

$$v_{n,T}^{2} = 4kT(R_G + \frac{2}{3g_m}) \qquad i_{n,T}^{2} = 4kT\frac{\frac{2}{3}\cdot g_m}{\beta(f)^2}$$

= Induced gate noise $i_{,g}^2$

correlated

Bipolar:

$$v_{n,T}^{2} = 4kT(R_B + \frac{1}{2g_m}) \qquad i_{n,T}^{2} = 2\cdot q\cdot(I_B + \frac{I_C}{\beta(f)^2})$$

$$= \frac{4kT\cdot g_m}{2}\left(\frac{1}{\beta} + \frac{1}{\beta(f)^2}\right)$$

BJT vs. MOS: Noise Figure

Noise Factor: *F = SNRout/SNRin ≅ Total (equiv.) noise / Noise due to RS only*

Noise Figure: *NF = 10 log (F) [dB]*

First order approximation:

$$F = 1 + \frac{(v_{n,T} + i_{n,T} \cdot R_S)^2}{4kT \cdot R_S}$$

*Note: to account for correlation v_n and i_n*R_S are first added and then squared = debatable*

Optimum NF reached with noise matching when:

$$R_{S,opt} = \frac{v_n}{i_n}$$

-> Tradeoff between IC/D, area, and RS

$R_{S,opt}$ is not necessarily the same as R_S needed for impedance matching (optimum power transfer);

BJT: 100Ω range - simultaneous power and noise matching

MOST: kΩ range – more difficult to achieve at high frequencies

SiGe has advantages due to low rbb and high f_T (β_{AC})

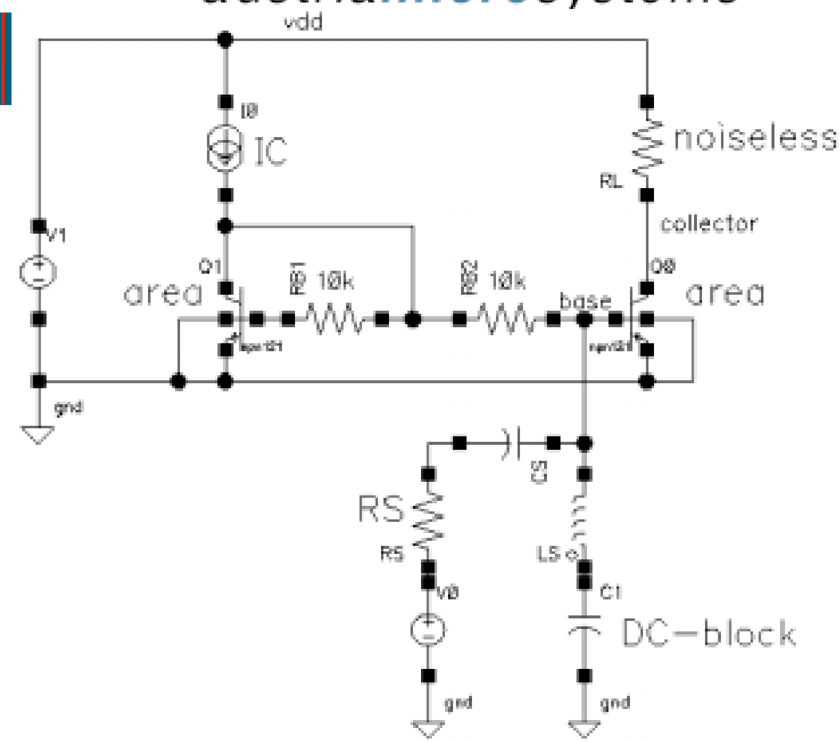
Noise Figure S35

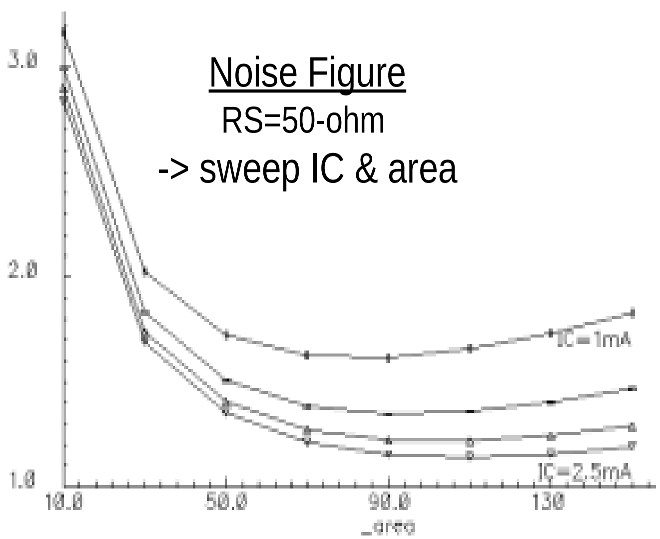
NF requires optimum for

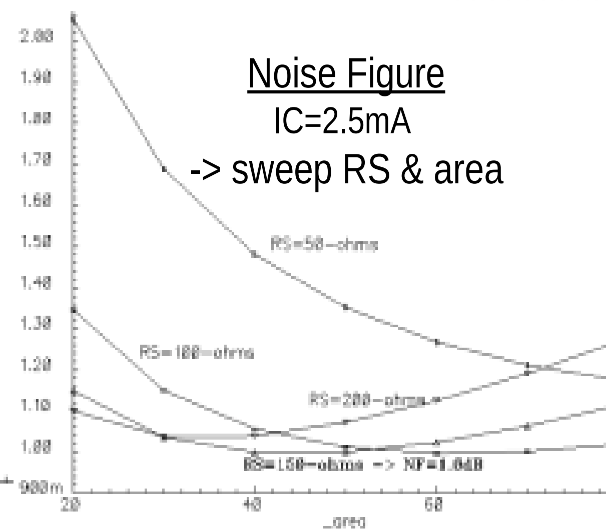
- device area,
- bias current,
- source impedance:
  - not necessarily 50-ohms
  - not purely “real”.

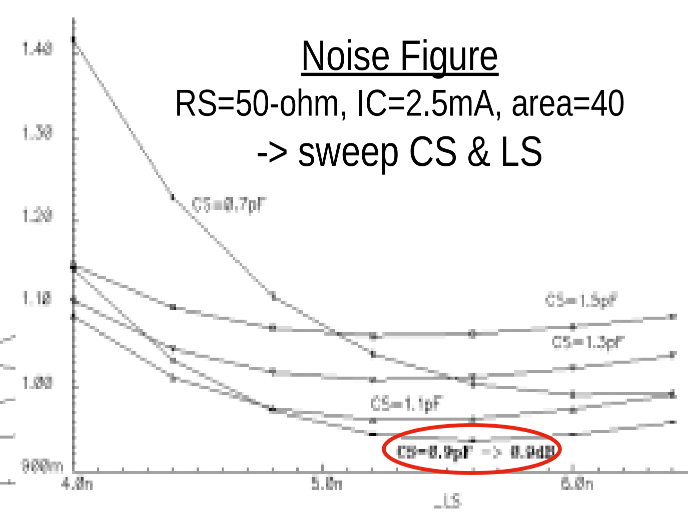
Sweep input matching

-> NFmin=0.9dB @2.4GHz @2.5mA

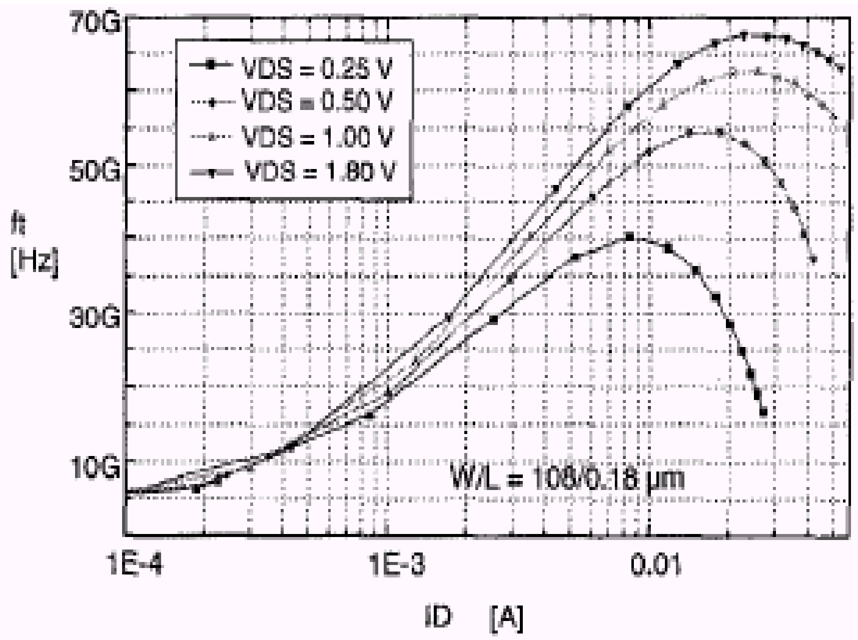








0.18um CMOS - RF



. 11: Measured fT for the regular Vt high performance device.

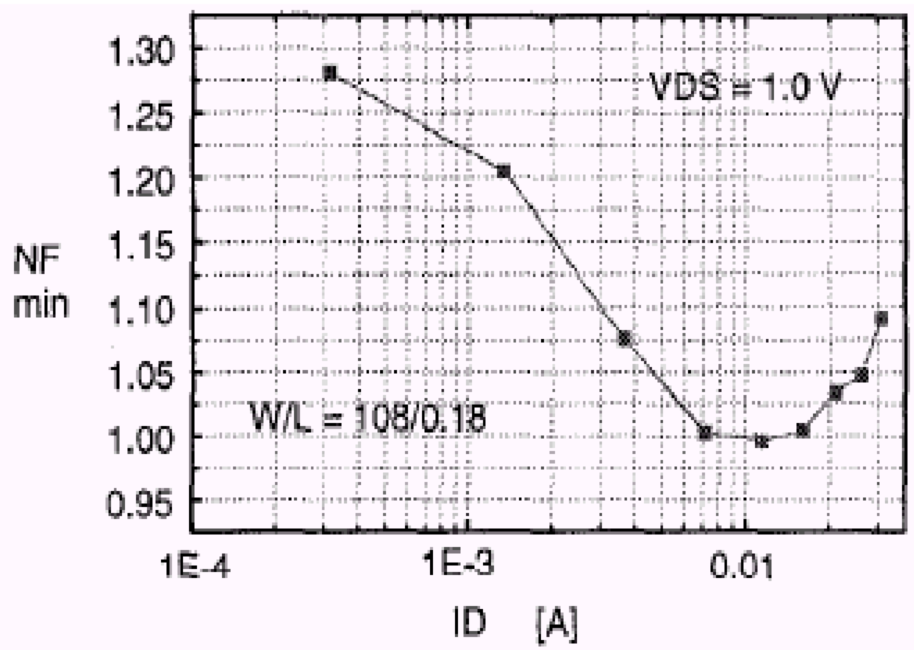
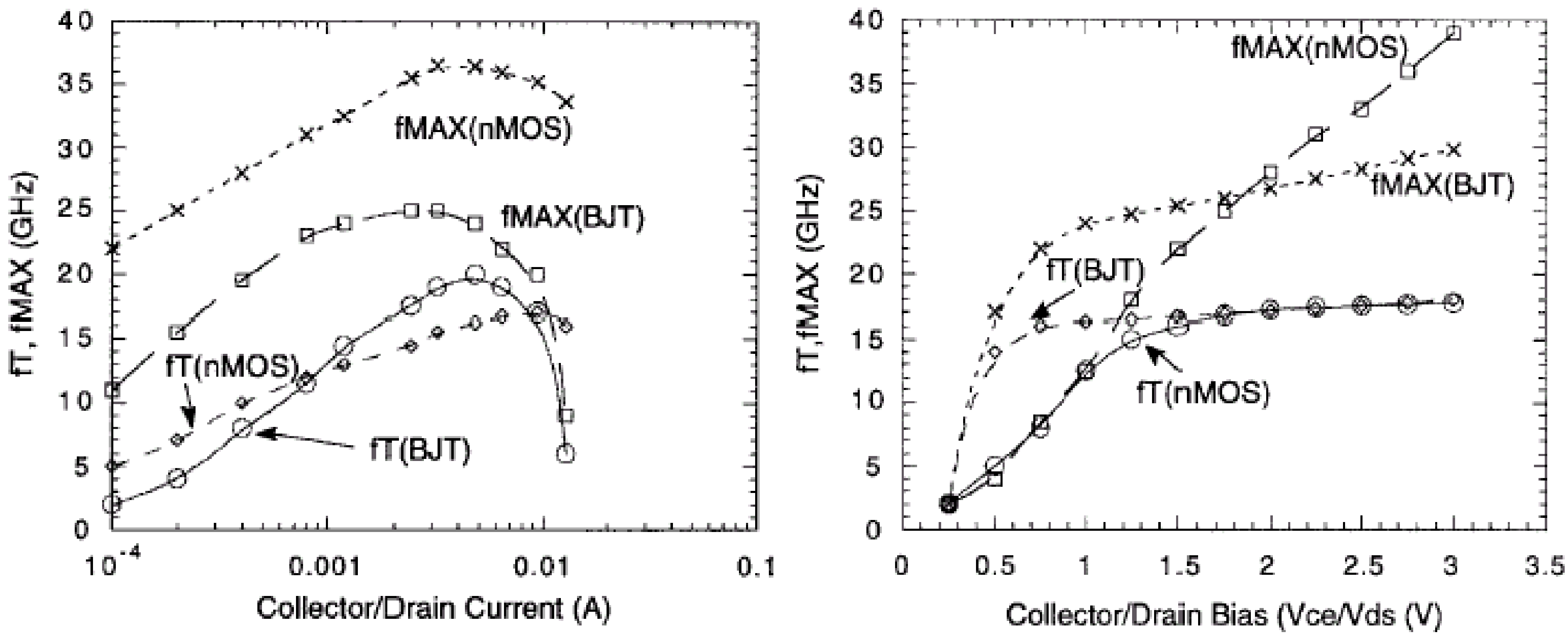


Fig. 12: Minimum noise figure @ 2GHz for the regular Vt device.

‘System on a Chip’ Technology Platform for 0.18um Digital, Mixed Signal & eDRAM Applications
- Infineon & IBM, IEDM99.

fT dependency on VCE, VDS

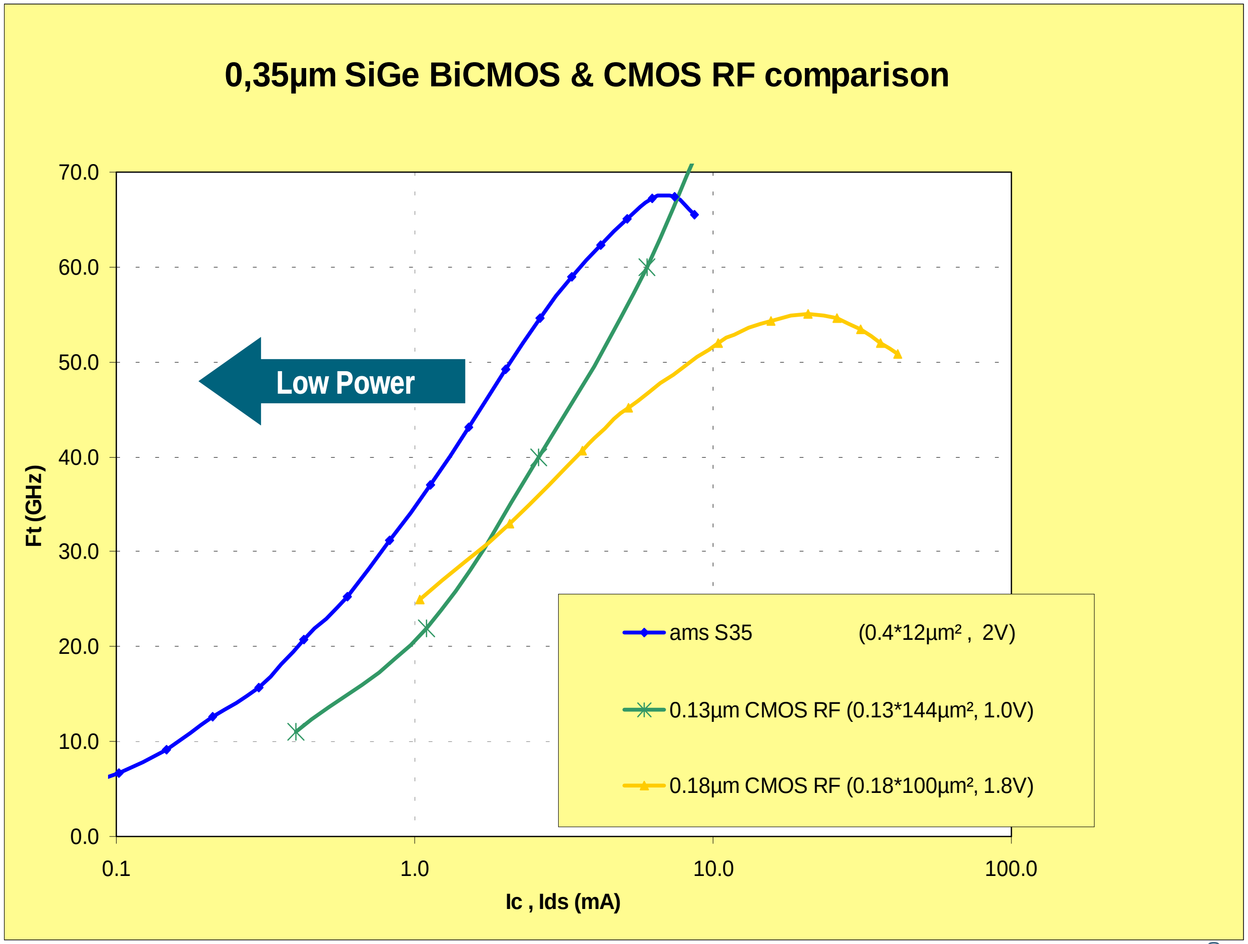
0.5um BiCMOS process (not AMS):



[Voinigescu95, Larson97]

0.35µm SiGe vs. 0.18um / 0.13um CMOS

- 1/3 of CMOS RF current consumption



Breakdown as function of fT; SiGe vs. CMOS

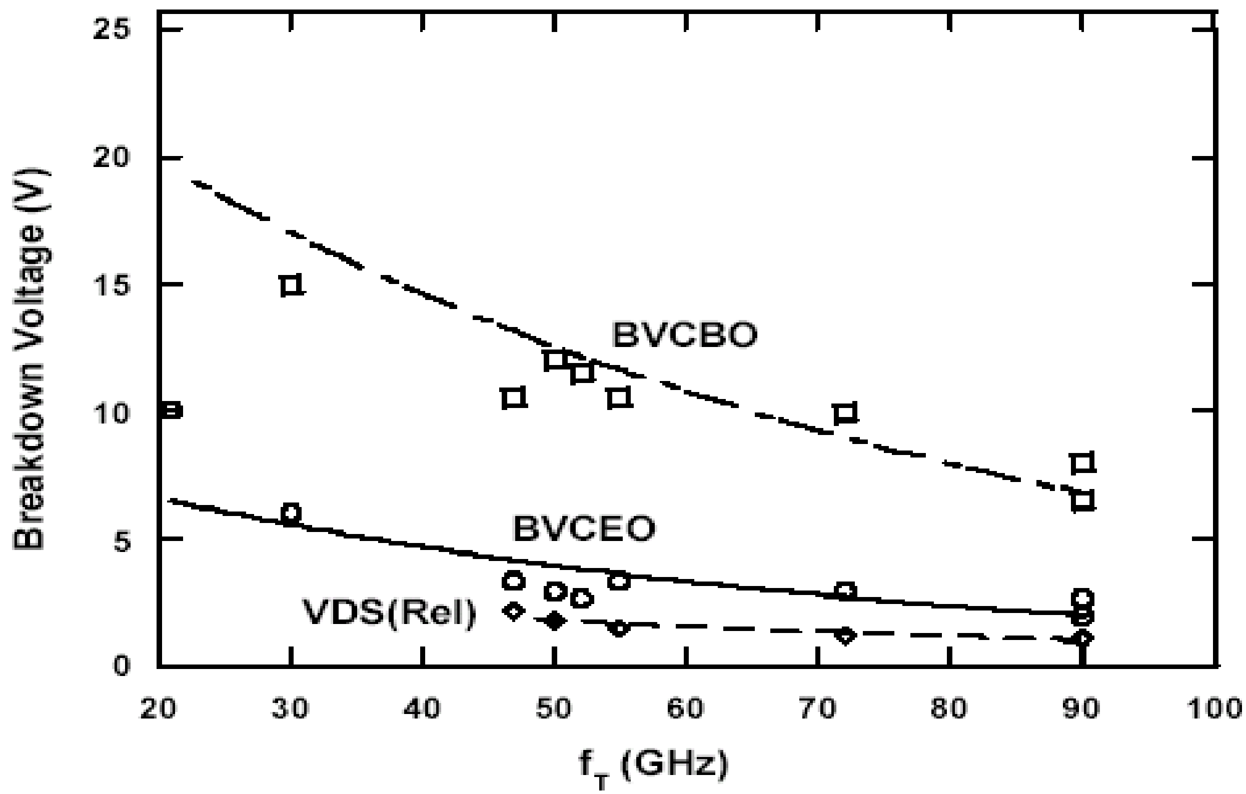


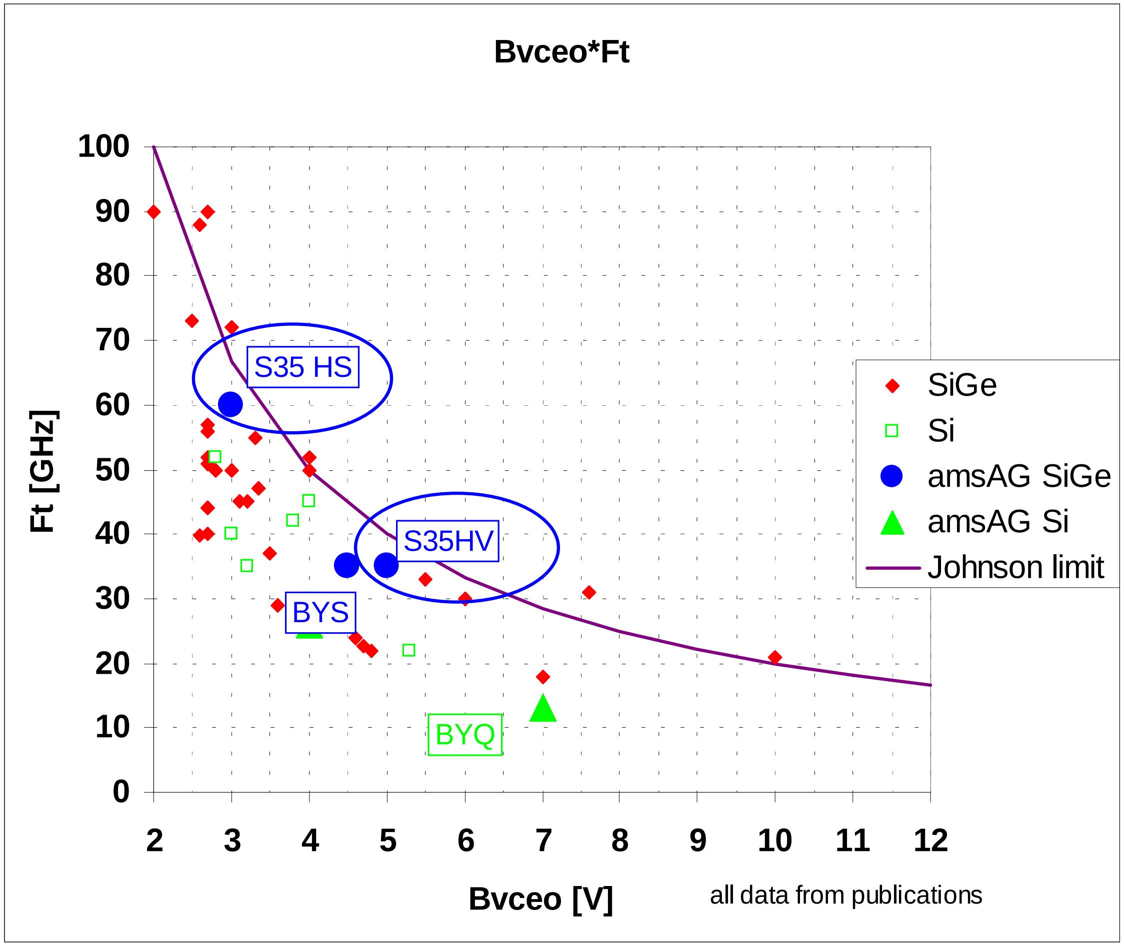
Figure 3: Comparison of voltage limitations of MOSFETS and HBTs as a function of f_T.. The Si/SiGe HBT BVCEO and BVCBO maintain a roughly 1:3 relationship from 20 to 90 GHz.

ICSI 2003, Santa Fe

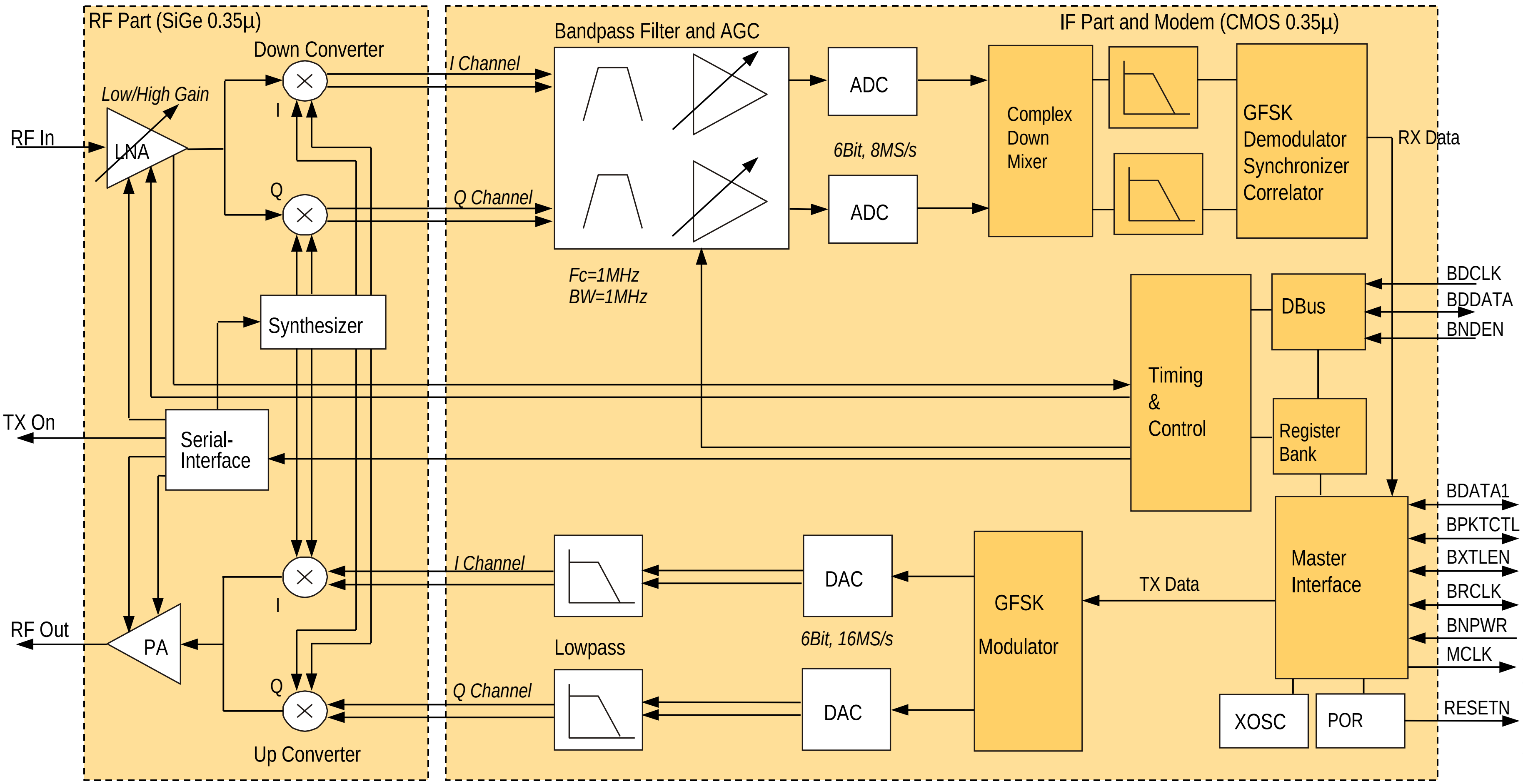
S35 HV and HS transistors

- High Voltage (S35HV) and High-Speed (S35HS) HBT's on the same IC

- HV or HS only reduces mask count by "-1"

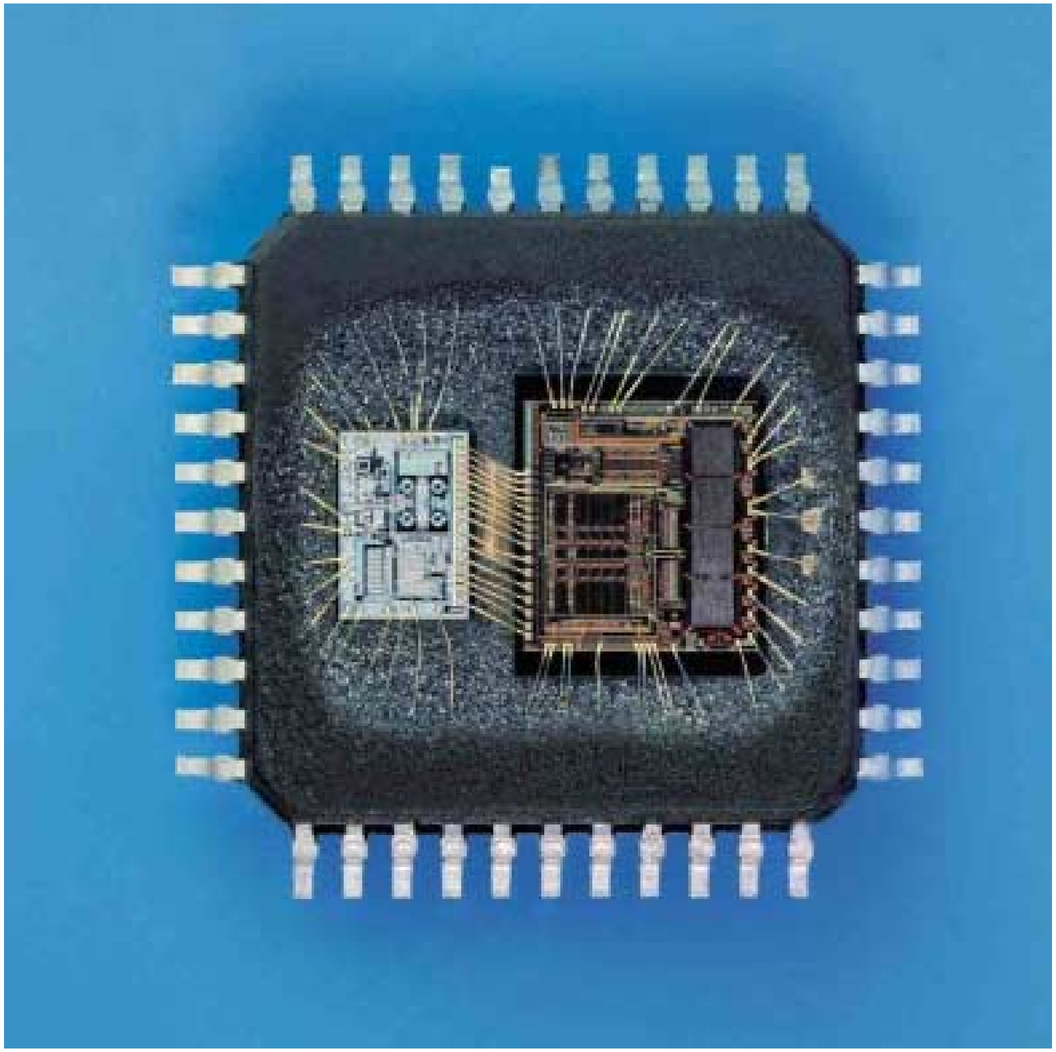


BJT *plus* MOS: 2.4GHz Transceiver Architecture



ams' BT radio

2.4GHz Transceiver in a Multi Chip Package



2 ICs in one package:

0.8µm SiGe-BiCMOS
(S35 redesign on-going)
+
0.35µm CMOS

Conclusion: SiGe vs. RF-CMOS w.r.t. a 2.4GHz radio

SiGe (0.35um):

+ lower noise
  (-90dBm vs. *-80dBm*)
  ⇒ longer distance
  ⇒ higher quality of operation

+ lower current consumption
  (peak current)
  (25mA @-85dBm
  or 30mA @-90dBm
  vs. *40mA @-80dBm*)
  ⇒ longer battery life

CMOS (0.18um):

+ allows higher system integration
  ⇒ cheaper system

References / Recommended Reading

[1] Foundation of rf CMOS and SiGe BiCMOS technologies - J.S. Dunn, *IBM J. Res. & Dev*., Vol. 47, No. 2/3, March/May 2003, p.101~138.

[2] SiGe HBT Technology: A New Contender for Si-Based RF and Microwave Circuit Applications - John D. Cressler, *IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES*, May 1998, p.572~589.

[3] Transistor Noise in SiGe HBT RF Technology - Niu, Gressler, e.a., *Journal of Solid-State Circuits*, Sept. 2001, p.1424 ~ 1427.

[4] Sub-Micron Silicon RF IC Technologies - D.K. Lovelace, e.a, *1998 IEEE MTT-S Digest*, p.1859~1862.