austriamicrosystems

VBIC - Simulator Implementation and Benchmarking

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BIP-AK

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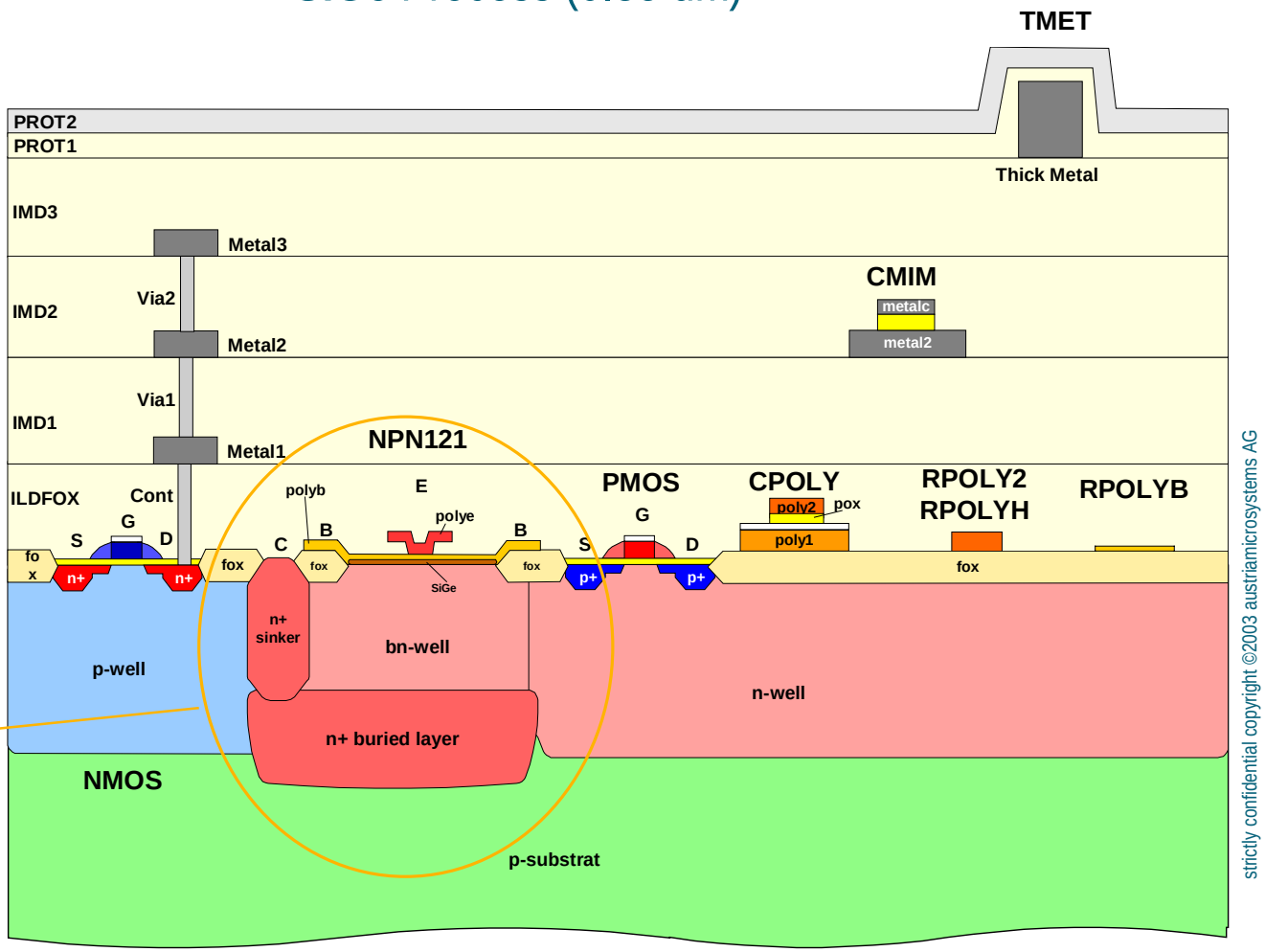
A leap ahead in mixed signal

Process cross section

- **Bipolar** transistors
- **MOS** transistors
- **MOS** varactors
- **Poly** resistors
- **Capacitors** (PiP,MiM)
- **Inductors**
  (M3, thick metal)

SiGe Process (0.35 um)



VBIC model

Bipolar model availability (2001)

Support of 2 design environments (Cadence, ADS, Mentor)
and 2 different simulators

Simulator	VBIC (1.15)		MEXTRAM		HICUM	
	Available	Robust/ accurate	Available	Robust/ accurate	Available	Robust /accurate
1)Spectre	Yes	Yes	Yes	?	No	X
2) ADS	Yes	Yes	Yes	?	No	X
3) ELDO	Yes	No	Yes	?	Yes	?
4) HSPICE	Yes	No	Yes	?	Yes	?
5) PSPICE	No	X	No	X	No	X
6) Saber	No	X	No	X	No	X
7) Smash	Yes	?	No	X	No	X
9) Smart-spice	Yes	?	Yes	X	Yes	X

Robustness/accuracy tested by austriamicrosystems

Bipolar model availability (2003)

Support of 3 design environments (Cadence, ADS, Mentor) and 6 different simulators

Simulator	VBIC (1.15)		MEXTRAM		HICUM	
	Available	Robust/ accurate	Available	Robust/ accurate	Available	Robust /accurate
1)Spectre	Yes	Yes	Yes	?	Yes	?
2) ADS	Yes	Yes	Yes	?	Yes	?
3) ELDO	Yes	Yes	Yes	?	Yes	?
4) HSPICE	Yes	Yes	Yes	?	Yes	?
5) PSPICE	No	X	No	X	No	X
6) Saber	No	X	No	X	No	X
7) Smash	Yes	Yes	No	X	No	X
9) Smart-spice	Yes	Yes	Yes	X	No	X

Support of bipolar compact model: tradeoff between accuracy and availability

Bipolar model implementation at austriamicrosystems

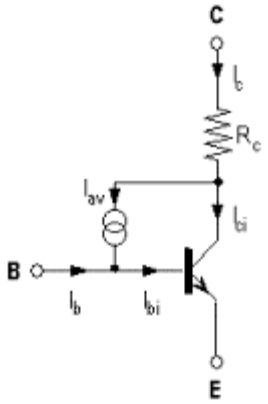
Simulator	Qualified Version (Level)	Supported since	Processes
Agilent-ADS	ADS 2003A (vbic)	1999	BYR,BYX,S35
ELDO	5.6 (Level 21)	2002	BYR,BYX,S35
Hspice	2003.3 (Level 4)	2003	BYR,BYX,S35
SmartSpice	2.0.8.C (Level 5)	2002	BYR,BYX,S35
Smash	4.3.5 (Level 2)	2001	BYR,BYX,S35
Spectre	4.6 (vbic)	1999	BYR,BYX,S35

The qualification is always linked to a specific simulator version.
Usage of another simulator version is at own risk.

VBIC - The starting point

0.8 um SiGe BiCMOS process (1998):

effect of weak avalanche current (VCE=3V)



$$I_{AV} = \left(\frac{-U_{bc\_smo}}{BVCB}\right)^{NAV} \cdot I_C$$

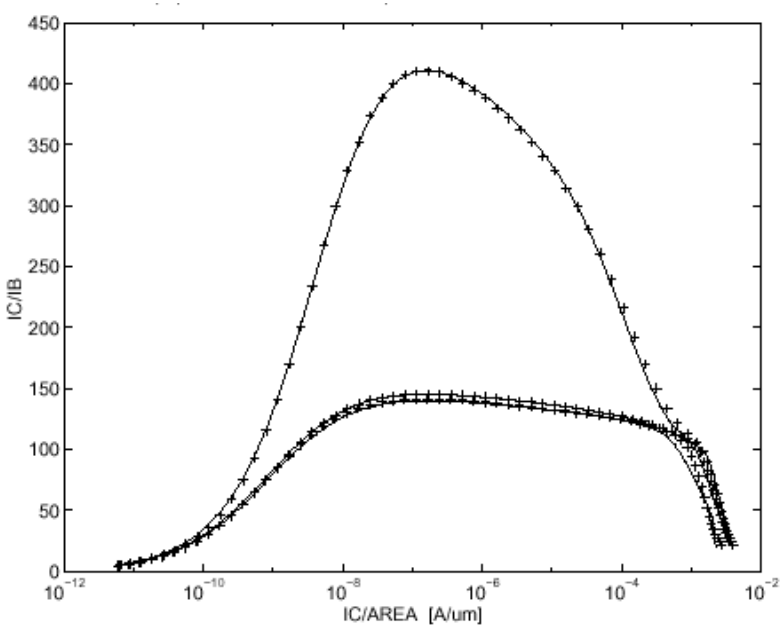
$$\varepsilon = 0.0001$$

$$U_{bc\_smo} = 0.5\left(U_{bc} - \sqrt{U_{bc}^2 + \varepsilon^2}\right)$$

Solutions:

1) Gummel Poon model + subcircuit (supported until 2003)

2) New compact model: VBIC



VBIC model benchmarking - public release

Parameter Set: Public release (Colin Mc Andrew)

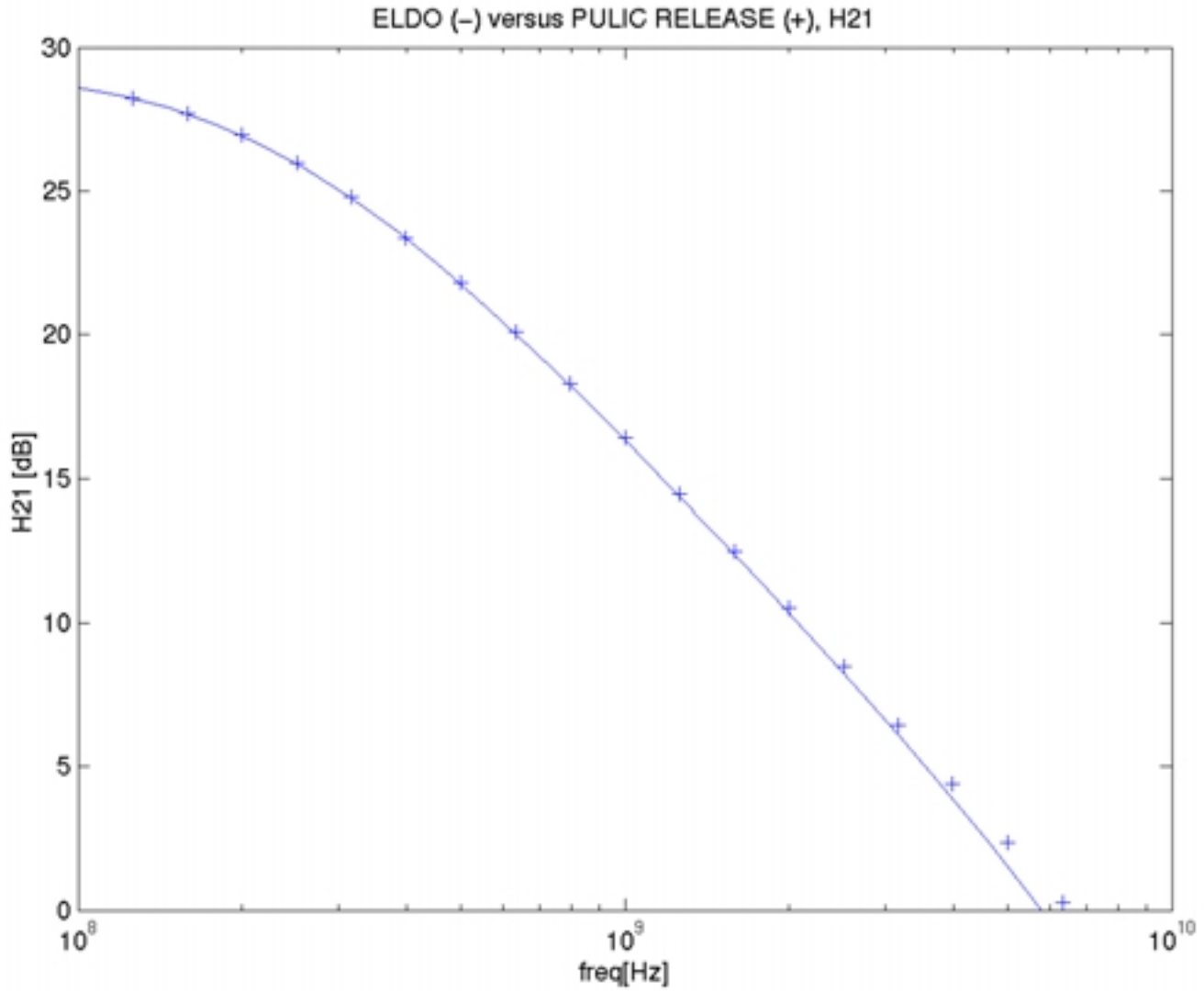
Tests carried out:

FG, Forward Gummel (T=-50, 27, 50, 150 deg.)
RG, Reverse Gummel
H21 (FT)

Results of benchmark simulator (FORTRAN)
are compared to simulator under test.

Criteria: relative error < 0.5 %

Example benchmark (ELDO 5.6)



VBIC benchmarking problems

Spectre:

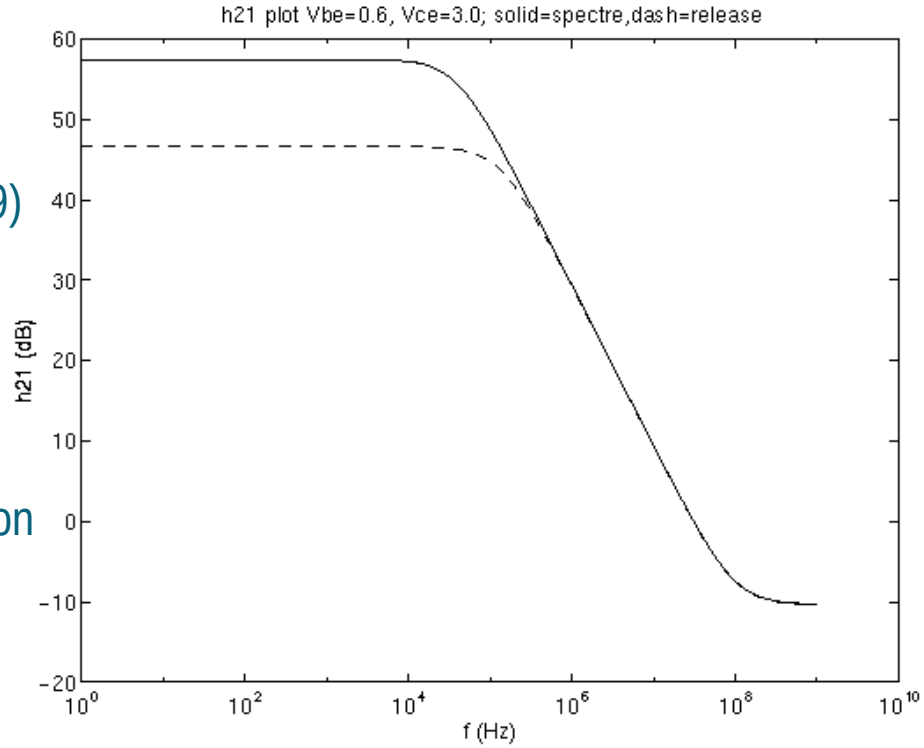
First VBIC bipolar parameter set extracted at ams: 11/1998

First tested version of VBIC in Spectre: 4.4.3 (1999)

20-01-1999:
AC implementation wrong (error in h21 > 10dB)

8-6-2000:
Monte Carlo implementation for IS gives no variation

fixed in 4.4.3.100.98

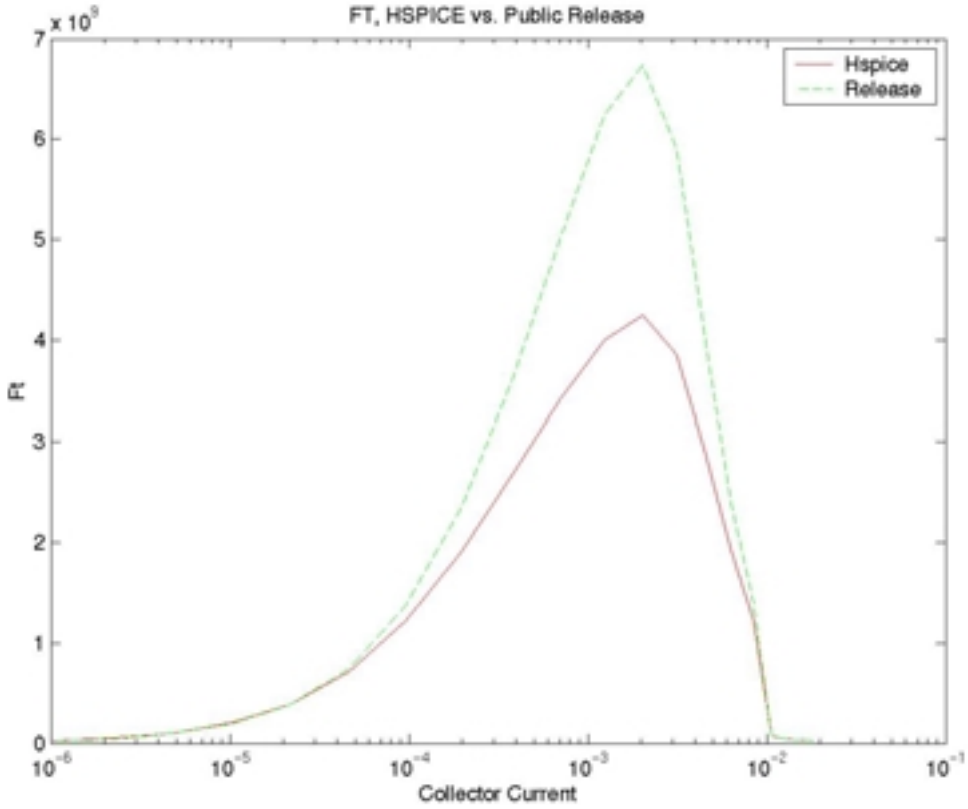


VBIC benchmarking problems

HSPICE 2000.4:

FT (h21) wrong for public release test

AREA parameter not supported ! (resolved for HSPICE 2003.3)



VBIC benchmarking problems

ELDO 5.3 (7/2000): errors in h21

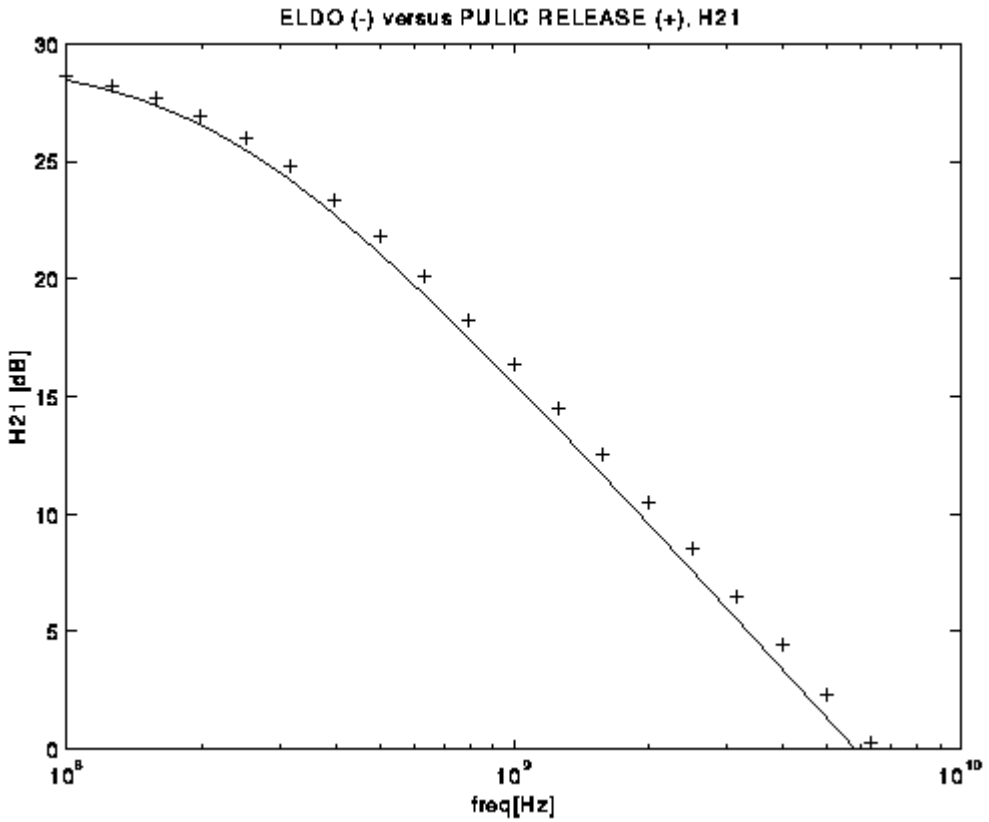
resolved for ELDO 5.6 (1/2002)

ELDO 6.2:
Warning issued:

“Level 21 replaced by Level8, version 1.15”

But: Version=1.2 selected by simulator

Solution:
Explicitely set level=8, version=1.15, in model file !



VBIC process benchmarking

— **Scalable model** parameters extracted by Zoltan Huszka (MATLAB routines)

— Comparison of extraction results to results of **golden reference simulator** (Spectre)

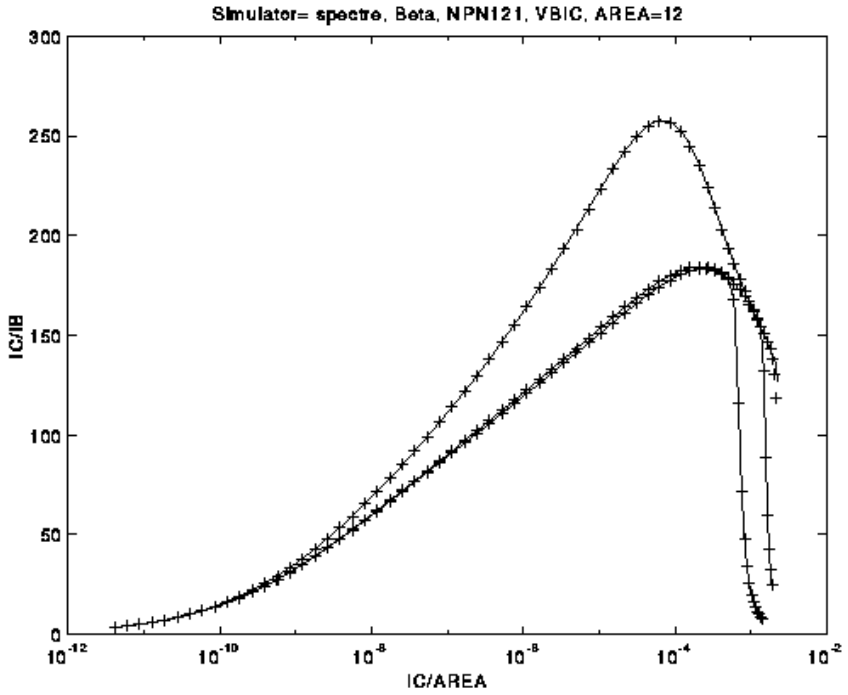
— Benchmarks are carried out for **any process parameter update** and the following devices: npn121, npn111, npn132, npn232, npn243, npn254

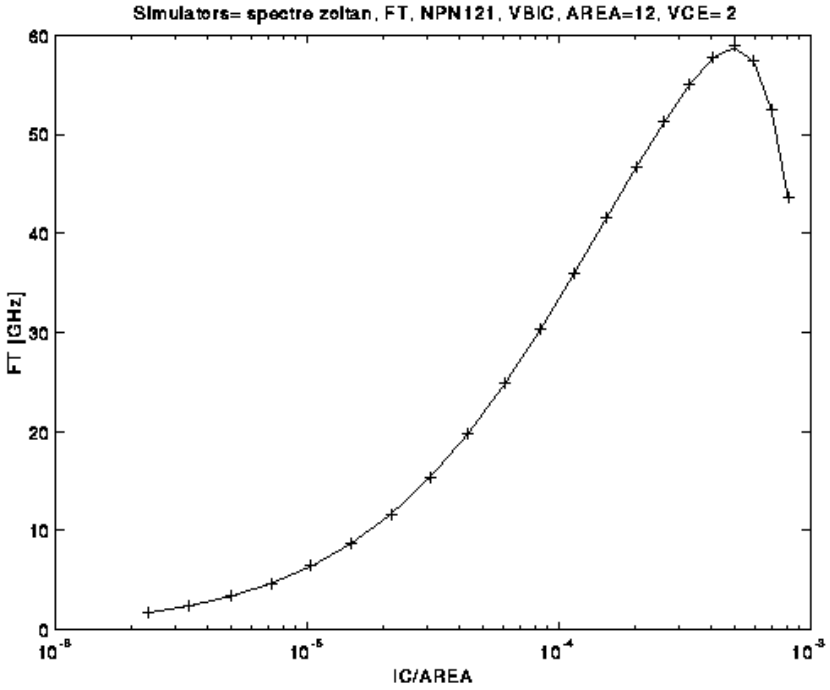
— **Benchmarks:**

FG (Forward Gummel), AREA=0.8, 12, 24
FT, AREA=0.8, 12
Worst Case Corner (FT and FG), AREA=0.8, 12

Example - S35 process: 84 benchmark simulations

VBIC process benchmarking (Beta and FT)





VBIC Worst Case Corner Modeling

Device performance variation is described by SPICE models

– **RF - MOS transistors (BSIM3V3)**

wp (fast NMOS, fast PMOS)
ws (slow NMOS, slow PMOS)
wo (fast NMOS, slow PMOS)
wz (slow NMOS, fast PMOS) + typical

– **RF - Bipolar (VBIC, SGP)**

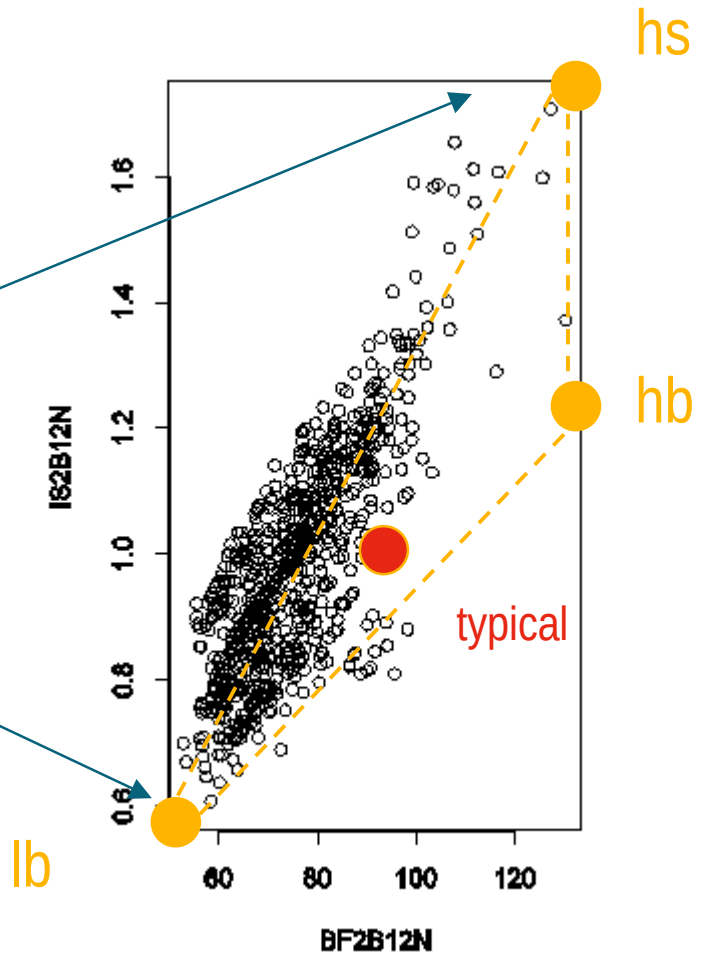
hs (high speed, high beta)
lb (low speed, low beta)
hb (low speed, high beta) + typical

– **RF - Resistors/Capacitors**

wp (worst power), ws (worst speed) + typical

– **RF - Inductors**

lq (low q-factor), hq (high q-factor) + typical



VBIC Worst Case Corner Modeling

Maximization of IC, Current Gain (IC/IB), FT

Example: VBIC model

$$I_C = IS\left(\exp\left(\frac{vbe}{NF \cdot V_t}\right)-1\right)+\cdots$$

$$I_B = IBEI\left(\exp\left(\frac{vbe}{NEI \cdot V_t}\right)-1\right)+\cdots$$

~IS/BF

SPICE parameter limits

MAP parameter limits

VBIC

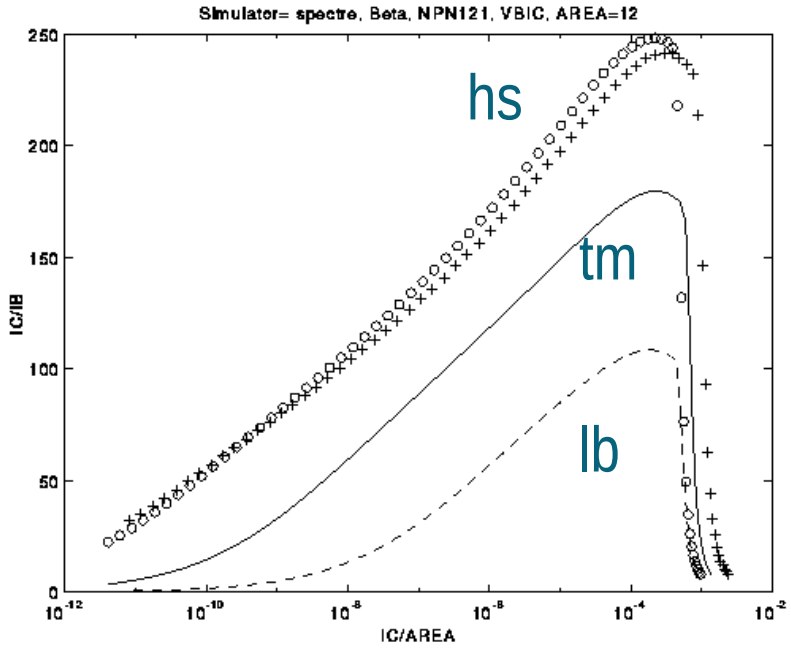
MAP

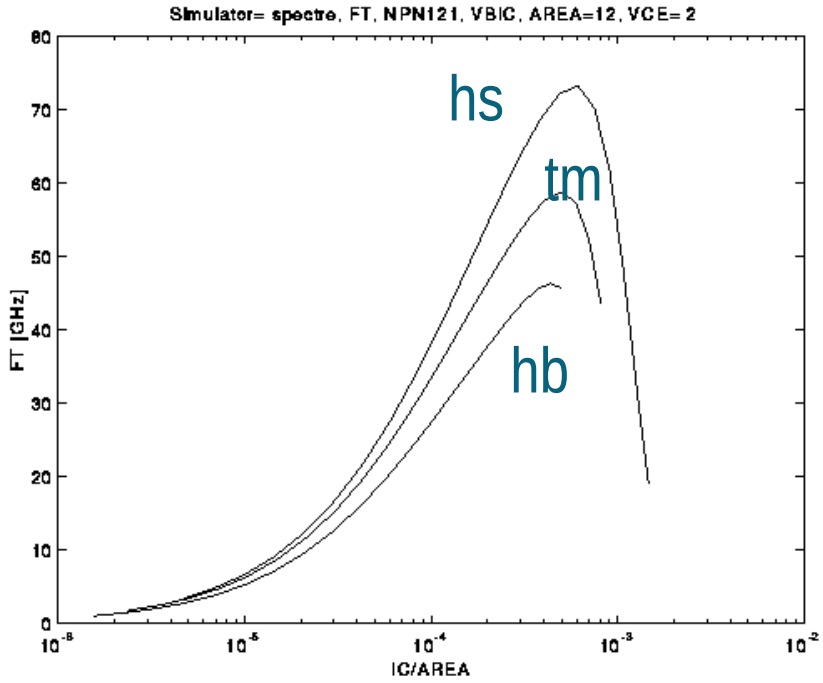
Parameter	LB	HB	HS	MAP-PAR
IS	min	tm	max	IS2B3N
IBEI*	lb	hb	hs	BF2B3N/IS2B3N
IBEN	max	min	min	IS2B3N
VEF	max	min	max	2*VAF2BN
IKF	min	tm	max	ICHB2BN
RE	max	max	min	RE2BN
RBI	max	max	min	RBDC1BN
RBX	max	max	min	RBDC1BN
RCX	max	max	min	RC2B3N
RCI	max	max	min	RC2B3N
CJE	max	max	min	CJE
CJC	max	max	min	CJB
CJEP	max	max	min	CJB
CJCP	max	max	min	CJN
TF	max	tm	min	FT2BN
AVC2*	max	min	min	BVCBO2BN

Corner Simulation - Bipolar Transistors

BF
min typ max
100 170 240

FT
min typ max
50 60 75





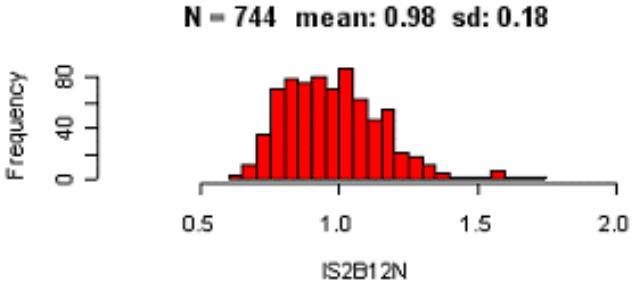
CJE, TF, BF

VBIC - Monte Carlo and Mismatch

Process simulation (Monte Carlo):

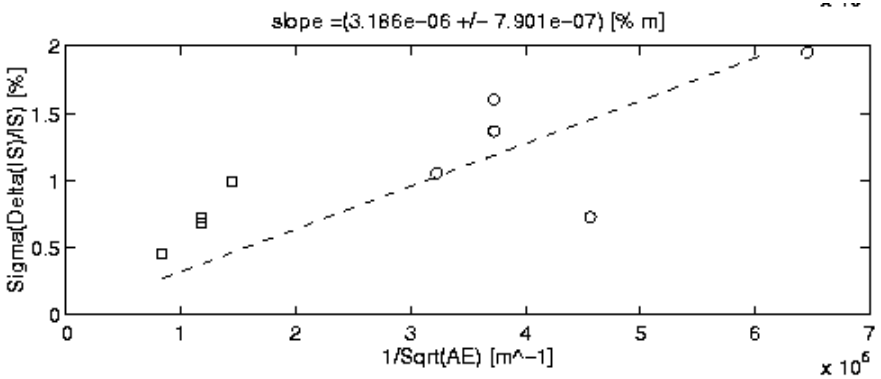
Process variation (uniform distribution) of:

IS, IBEI, IBEN, RBI, RE,RC, CJE, CJC, CJ



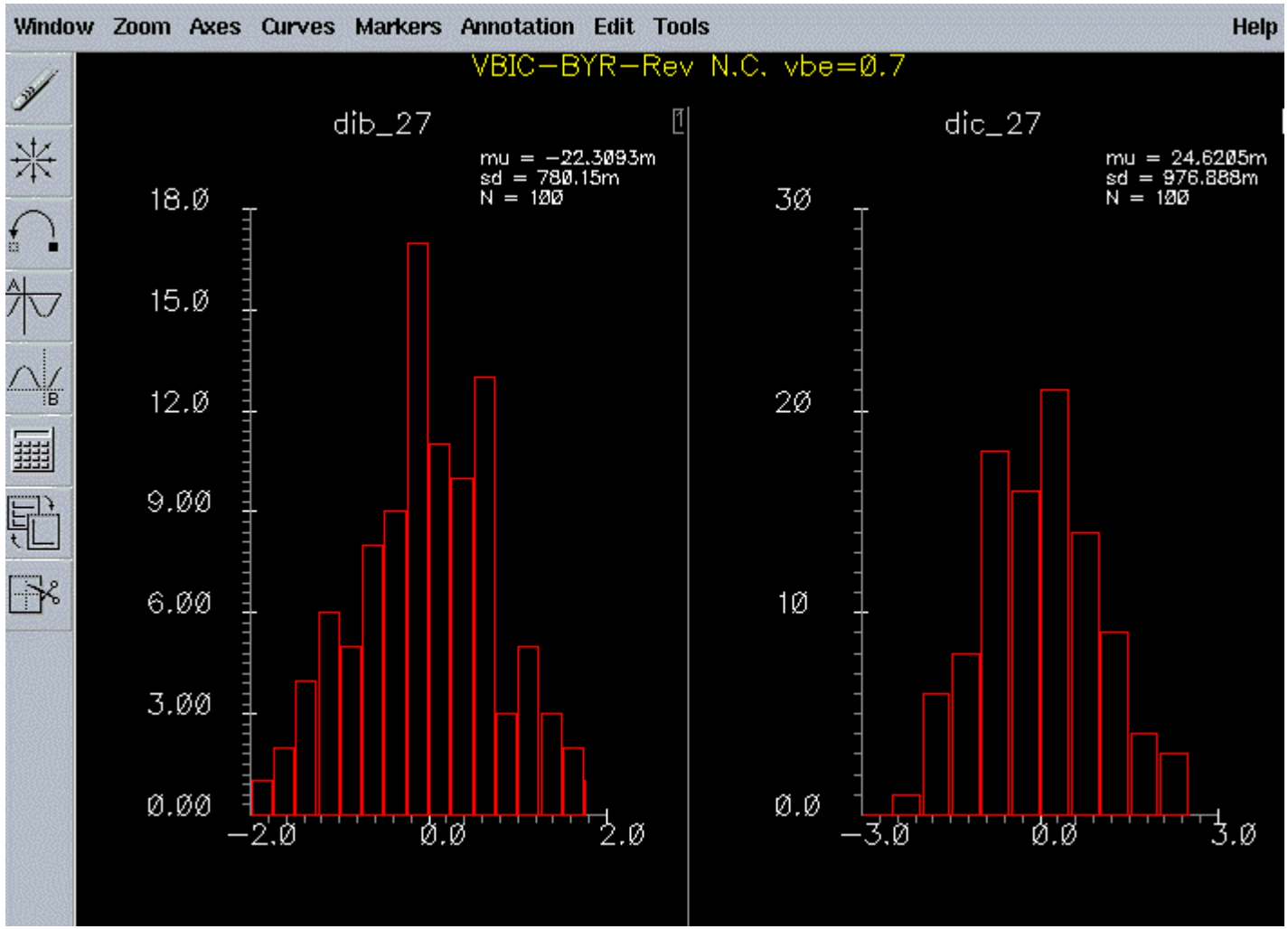
Mismatch (Gaussian distribution) of:

IS, IBEI, IBEN



$$\sigma(\Delta IS / IS) = A_{IS} / \sqrt{AREA}$$

VBIC Mismatch Simulation



Conclusion

- VBIC advantages : availability (most simulators and extraction tools)
- VBIC 1.15 is implemented correctly for most of the simulators
- Simulator benchmark of bipolar device models is critical and elaborate
- Missing features (scalable models, mismatch etc.) must still be implemented using sub-circuits.
- Vision: standardisation
  Interesting project: ADMS/ZSPICE by L. Lemaitre
  Verilog-AMS - Code Generation (ADMS) - Benchmarking(ZSPICE)

  http://sourgeforce.net/projects/mot-adms