A leap ahead in mixed signal
- **Bipolar** transistors
- **MOS** transistors
- **MOS** varactors
- **Poly** resistors
- **Capacitors** (PiP, MiM)
- **Inductors** (M3, thick metal)

**SiGe Process (0.35 um)**

**VBIC model**
Support of 2 design environments (Cadence, ADS, Mentor) and 2 different simulators

<table>
<thead>
<tr>
<th>Simulator</th>
<th>VBIC (1.15)</th>
<th></th>
<th>MEXTRAM</th>
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<th>HICUM</th>
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Robustness/accuracy tested by austriamicrosystems
Support of 3 design environments (Cadence, ADS, Mentor) and 6 different simulators

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<td>9) Smart-spice</td>
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Support of bipolar compact model: tradeoff between accuracy and availability
The qualification is always linked to a specific simulator version. Usage of another simulator version is at own risk.
0.8 um SiGe BiCMOS process (1998):
effect of weak avalanche current (VCE=3V)

Solutions:
1) Gummel Poon model + subcircuit (supported until 2003)
2) New compact model: VBIC
**Parameter Set:** Public release (Colin Mc Andrew)

Tests carried out:

FG, Forward Gummel (T=-50, 27, 50, 150 deg.)
RG, Reverse Gummel
H21 (FT)

Results of benchmark simulator (FORTRAN) are compared to simulator under test.

Criteria: relative error < 0.5 %
Example benchmark (ELDO 5.6)

ELDO (-) versus PULIC RELEASE (+), H21

- H21 [dB]
- freq [Hz]

The graph shows the comparison of H21 between ELDO (-) and PULIC RELEASE (+) across different frequencies.
Spectre:

First VBIC bipolar parameter set extracted at ams: 11/1998

First tested version of VBIC in Spectre: 4.4.3 (1999)

20-01-1999:
AC implementation wrong (error in h21 > 10dB)

8-6-2000:
Monte Carlo implementation for IS gives no variation
fixed in 4.4.3.100.98
**HSPICE 2000.4:**
FT (h21) wrong for public release test

**AREA** parameter not supported! (resolved for HSPICE 2003.3)
**ELDO** 5.3 (7/2000): errors in h21 resolved for ELDO 5.6 (1/2002)

ELDO 6.2:
Warning issued:

“Level 21 replaced by Level8, version 1.15”

But: Version=1.2 selected by simulator

Solution:
Explicitely set level=8, version=1.15, in model file!
— **Scalable model** parameters extracted by Zoltan Huszka (MATLAB routines)

— Comparison of extraction results to results of **golden reference simulator** (Spectre)

— Benchmarks are carried out for **any process parameter update** and the following devices: npn121, npn111, npn132, npn232, npn243, npn254

— **Benchmarks:**
  
  FG (Forward Gummel), AREA=0.8, 12, 24  
  FT, AREA=0.8, 12  
  Worst Case Corner (FT and FG), AREA=0.8, 12

Example - S35 process: 84 benchmark simulations
VBIC Worst Case Corner Modeling

Device performance variation is described by SPICE models

- **RF - MOS transistors (BSIM3V3)**
  - wp (fast NMOS, fast PMOS)
  - ws (slow NMOS, slow PMOS)
  - wo (fast NMOS, slow PMOS)
  - wz (slow NMOS, fast PMOS) + typical

- **RF - Bipolar (VBIC, SGP)**
  - hs (high speed, high beta)
  - lb (low speed, low beta)
  - hb (low speed, high beta) + typical

- **RF - Resistors/Capacitors**
  - wp (worst power), ws (worst speed) + typical

- **RF - Inductors**
  - lq (low q-factor), hq (high q-factor) + typical
Maximization of IC, Current Gain (IC/IB), FT

Example: VBIC model

\[ I_c = IS \left( \exp \left( \frac{vbe}{NF \cdot V_t} \right) - 1 \right) + \ldots \]

\[ I_b = IBEI \left( \exp \left( \frac{vbe}{NEI \cdot V_t} \right) - 1 \right) + \ldots \]

~IS/BI

SPICE parameter limits

MAP parameter limits

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<th>HB</th>
<th>HS</th>
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Corner Simulation - Bipolar Transistors

**BF**
- min: 100
- typ: 170
- max: 240

**FT**
- min: 50
- typ: 60
- max: 75

CJE, TF, BF
Process simulation (Monte Carlo):
Process variation (uniform distribution) of:
IS, IBEI, IBEN, RBI, RE, RC, CJE, CJC, CJ
Mismatch (Gaussian distribution) of:
IS, IBEI, IBEN

\[ \sigma(\Delta IS / IS) = A_{IS} \sqrt{\text{AREA}} \]
VBIC Mismatch Simulation

Window, Zoom, Axes, Curves, Markers, Annotation, Edit, Tools

VBIC-BYR-Rev N.C. vbe=0.7

\[ d1b_{27} \]
\[ \mu = -22.3093m \]
\[ \sigma = 786.13m \]
\[ N = 100 \]

\[ d1c_{27} \]
\[ \mu = 24.5205m \]
\[ \sigma = 976.389m \]
\[ N = 100 \]
Conclusion

- VBIC advantages: availability (most simulators and extraction tools)
- VBIC 1.15 is implemented correctly for most of the simulators
- Simulator benchmark of bipolar device models is critical and elaborate
- Missing features (scalable models, mismatch etc.) must still be implemented using sub-circuits.
- Vision: standardisation
  Interesting project: ADMS/ZSPICE by L. Lemaitre
  Verilog-AMS - Code Generation (ADMS) - Benchmarking(ZSPICE)
  
  http://sourceforge.net/projects/mot-adms