



Simple Emitter and Collector Scaling Approach with VBIC for Low-cost SiGe:C HBT's

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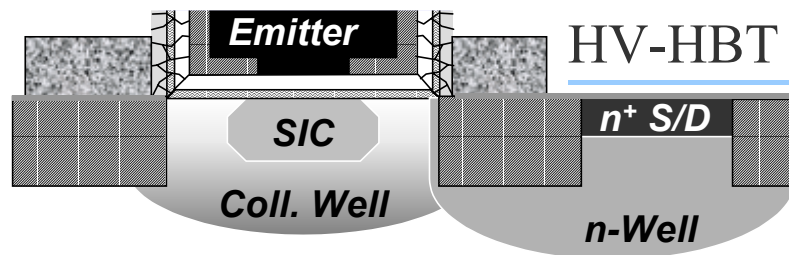
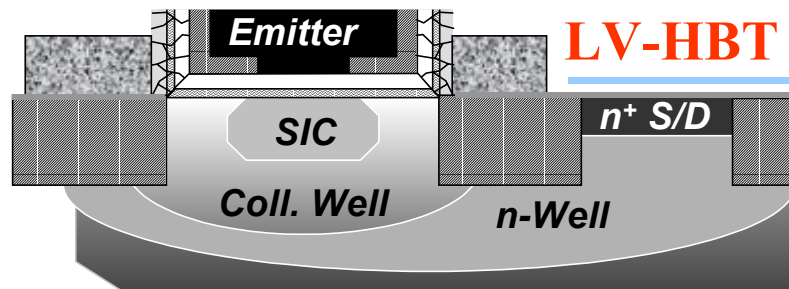
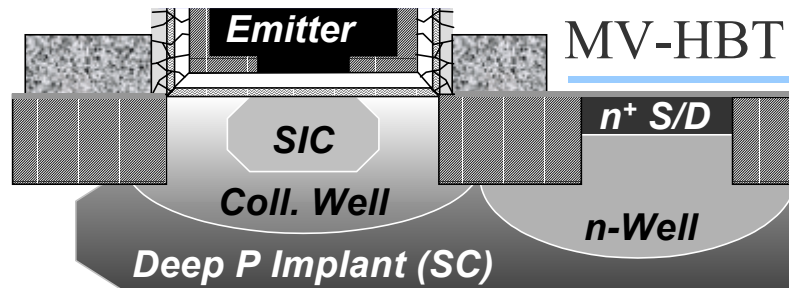
Bipolar Arbeitskreis

Unterpremstätten

October 23-24, 2003

- Technology and layout for scaling
- Test structures - general approach
- Scaling equations - implementation in IC-CAP
- Measurement setup
- Results
- Conclusion

SiGe:C Technology - HBT features



- 19 mask BiCMOS process
- Gate poly used for the external base
- CMP applied for separating the emitter from the external base
- 3 types of HBTs by different superpositions of the MOS n-well and isolation (SC) implants with the HBT collector well and SIC implants:

	BV_{CEO}	f_T
<u>MV-HBT</u>	4V	50GHz
<u>LV-HBT</u>	2.4V	75GHz
<u>HV-HBT</u>	>7V	30GHz

Details: D. Knoll et al., IEDM Tech. Dig., p.783, Dec. 2002.

Layout for scaling



Scaling approach is demonstrated for the **LV device**

Design Kit:

3 values can be accessed in PCell

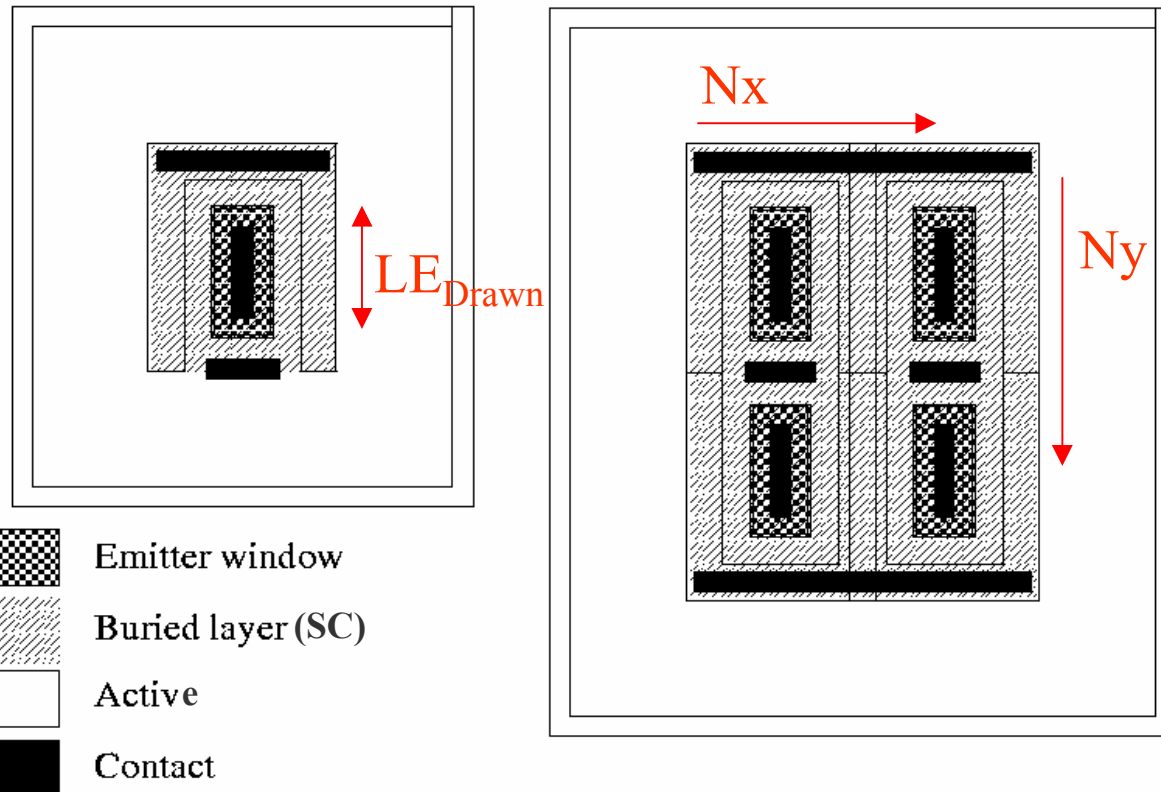
- Drawn emitter length (LE_{Drawn})

Number of emitters by

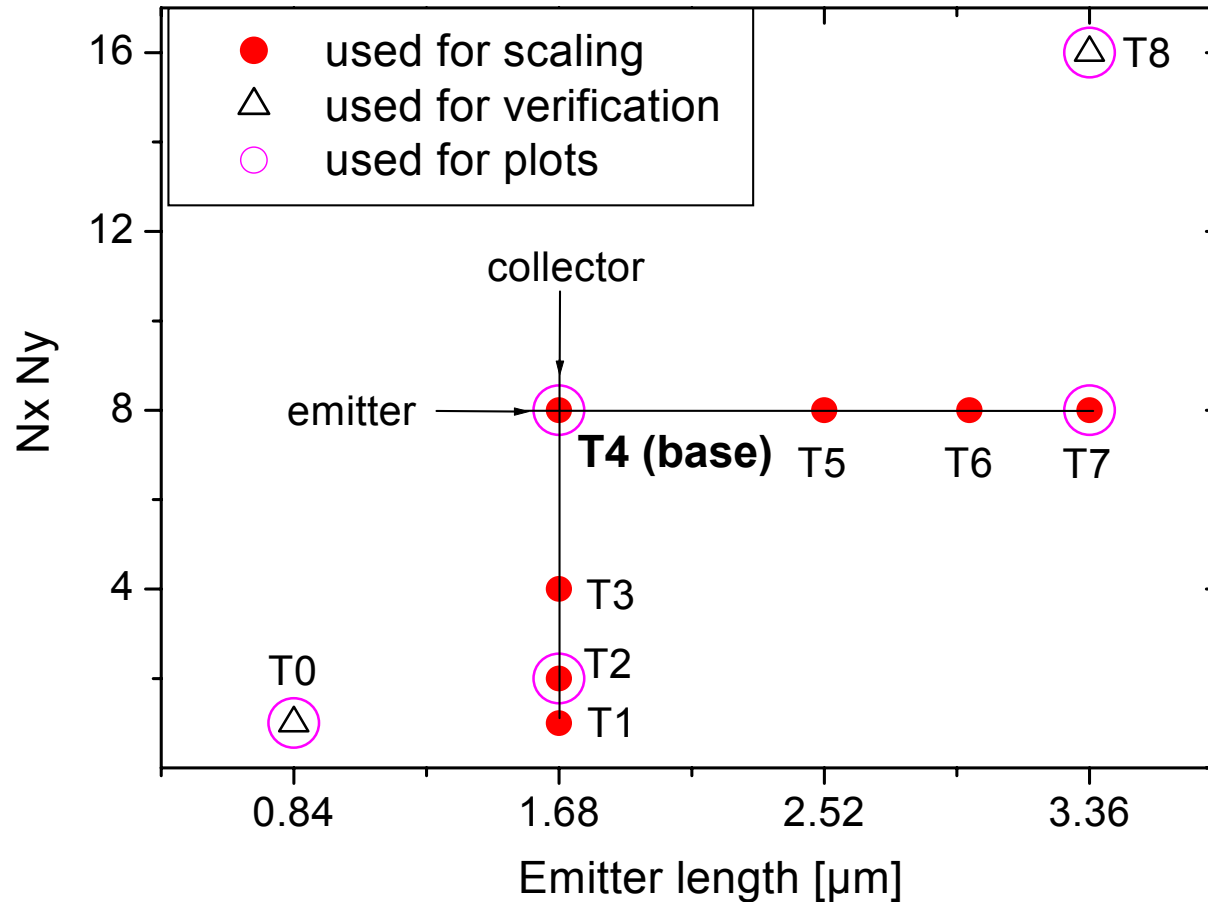
- No. of columns (N_x): 1 .. 8
- No. of rows (N_y): 1, 2

Scaling with

emitter and collector area



Test-structures used for scaling



LE_{Drawn} scaling : 4

N_x, N_y scaling : 4

verification : 2

total : 9

Not optimum choice !!!

Scaling approach for model parameter



1. Determine parameters of basic transistor (PAR_B) including temperature behavior and 1/f noise

Only one full parameter extraction and optimization !

2. Combining data from different geometries in one IC-CAP setup

3. Determine model parameter for scaled model (PAR_S) by optimization on curves from different geometries

Scaled model parameters (PAR_S) are function of basic parameters (PAR_B) and scaling factors (F_{PAR_SKF})

Scaling equations

$A_E = f(LE_{\text{Real}})$, $P_E = f(LE_{\text{Real}})$ real emitter area and perimeter,

$A_C = f(LE_{\text{Real}}, N_x, N_y)$, $P_C = f(LE_{\text{Real}}, N_x, N_y)$ real collector area and perimeter

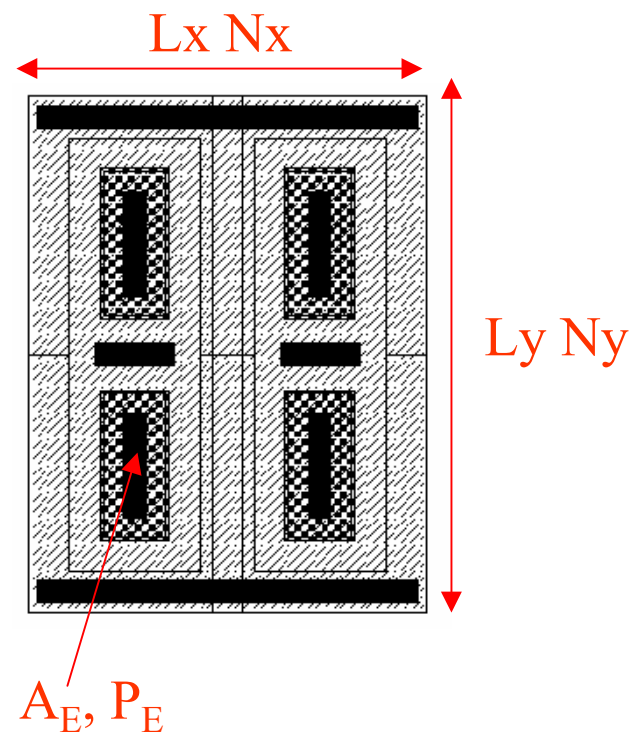
$$A_C = L_x N_x L_y N_y$$

$$P_C = 2(L_x N_x + L_y N_y)$$

$$L_y = f(LE_{\text{Real}}) \quad L_x = \text{const}$$

Values are normalized to the base device

For the base device: $CJE_S = CJE_B$



Scaling with emitter area/perimeter

$$CJE_S = CJE_B \left((1 - F_{CBE_SKF}) A_E + F_{CBE_SKF} P_E \right) N_X N_Y$$

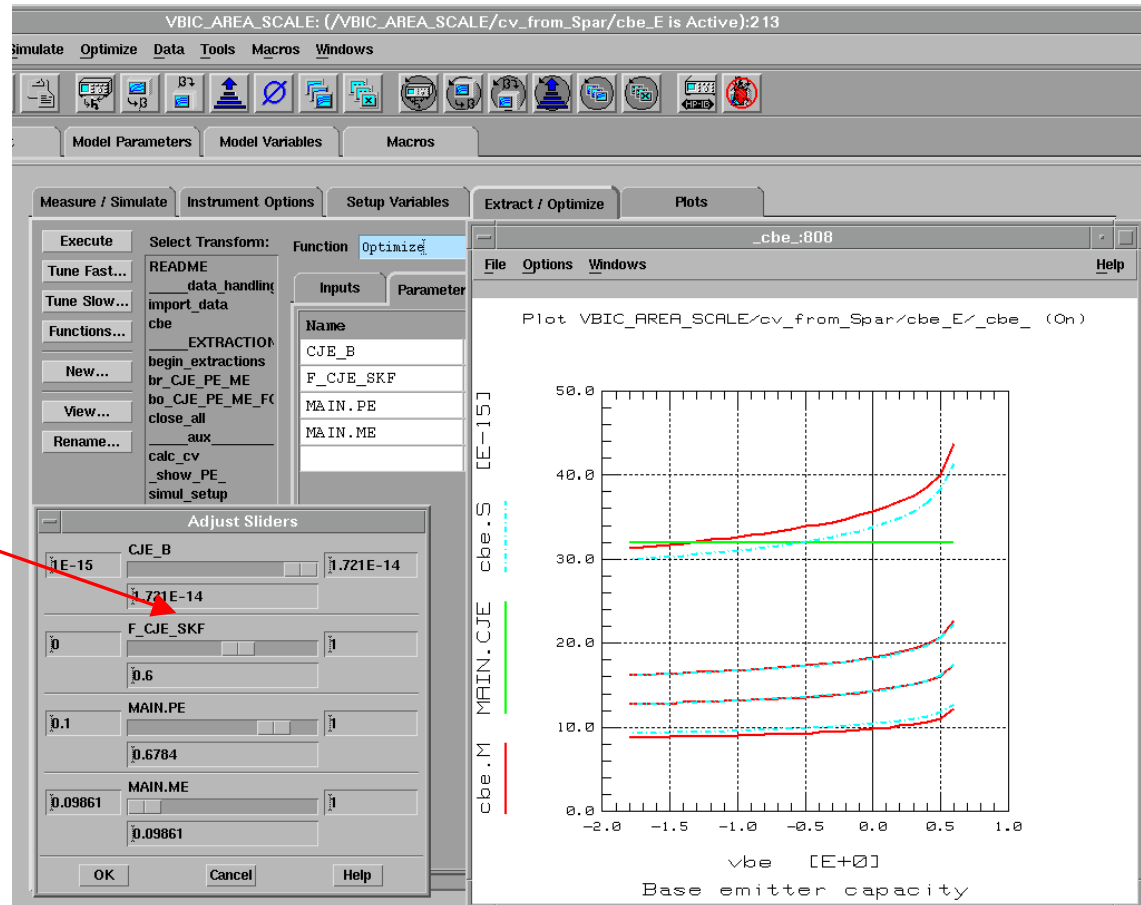
Similar: CJC, IS, IKF,
 IBEI, IBEN, RE, RBI, RCI
 CJEP (base area)

$F_{CBE_SKF} = 0.2$ fit
 in this example

$ITF = f(A_E)$

i.e. no scaling factor

same for other currents



Collector scaling and fitting

2. Scaling with collector area

$$CJCP_S = CJCP_B \left((1 - F_{CJCP_SKF}) A_C + F_{CJCP_SKF} P_C \right)$$

Similar: RCX, IBEIP, IBENP, RS

3. Scaling with fitting factor

$$RTH_S = \frac{RTH_B}{\sqrt{A_E}} \frac{1}{(N_x N_y)^{RTH_SKF}} \quad 0.5 < RTH_SKF < 1$$

Similar: AVC2, RBX (2)

Total 18 scaling factors

Measurement setup

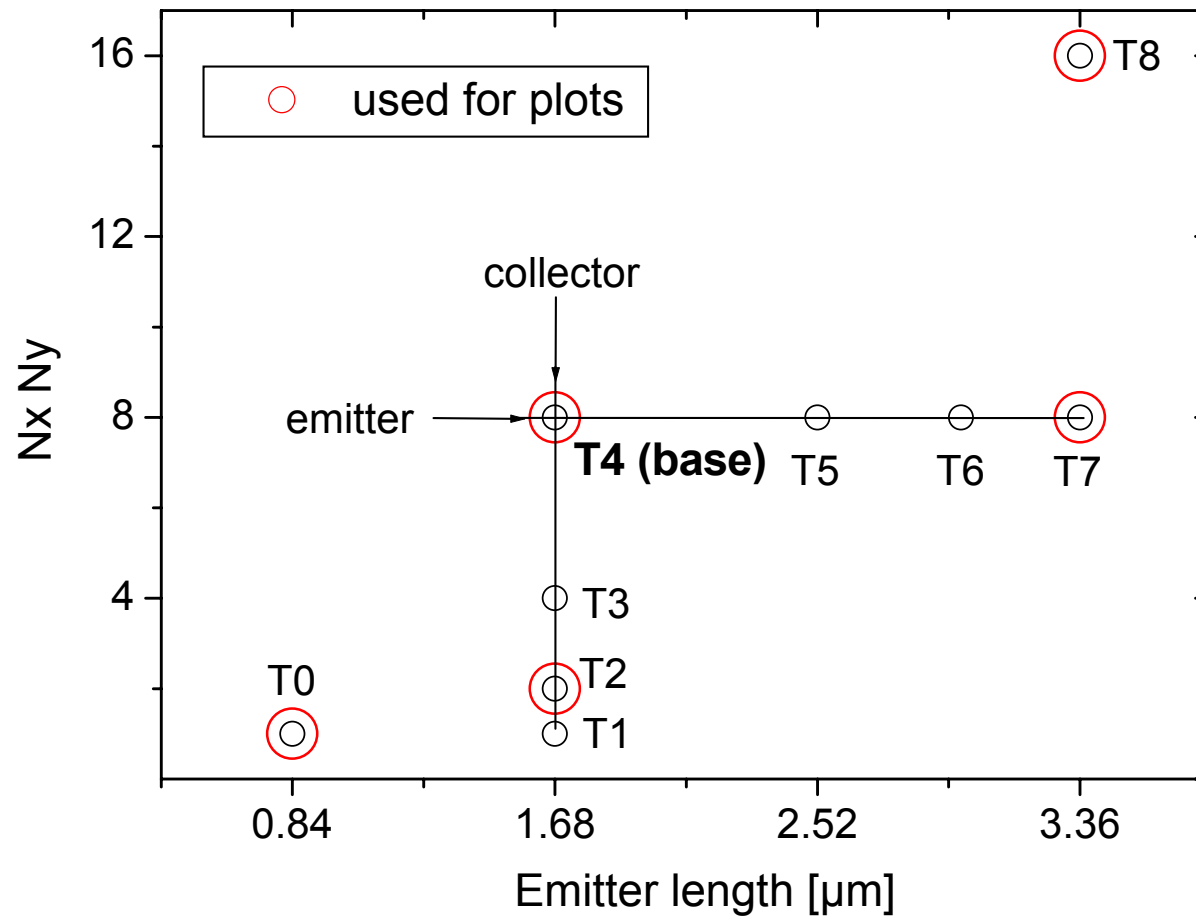


Single setup for DC and RF measurements

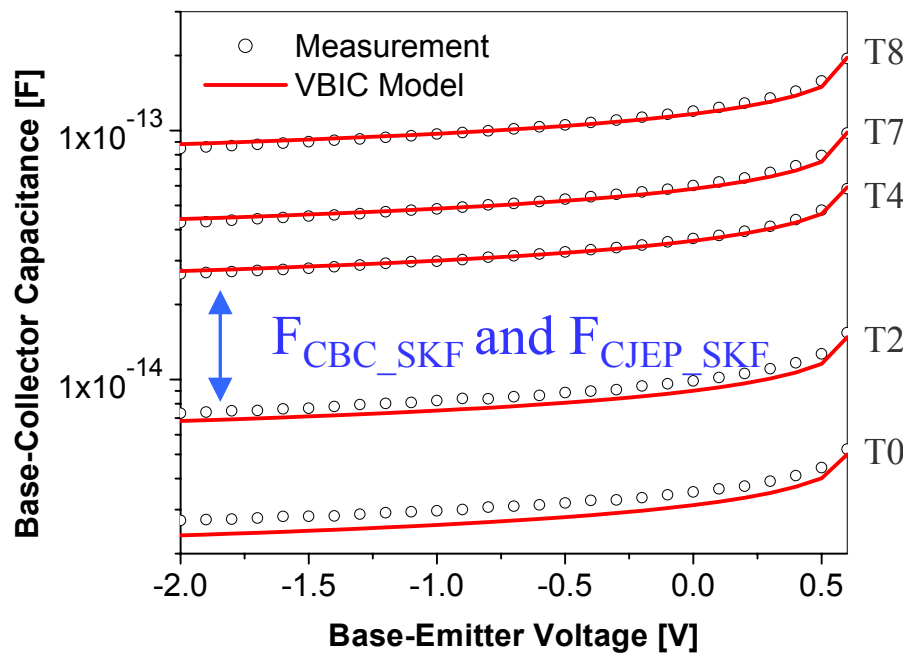


- DC-measurements (4142B)
Kelvin probes
- CV measurements (4284A)
- RF measurements (PNA E8364A)
45 MHz - 50 GHz
- Temperature range: -55 °C - 200 °C

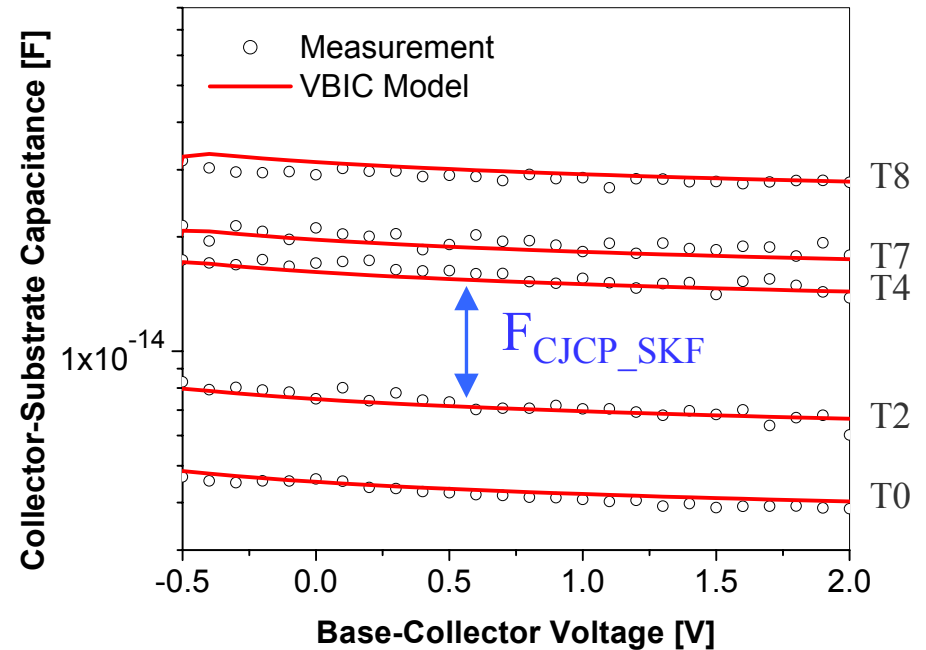
Results: 5 devices are plotted



Results: CV Scaling



Base-Collector capacitance

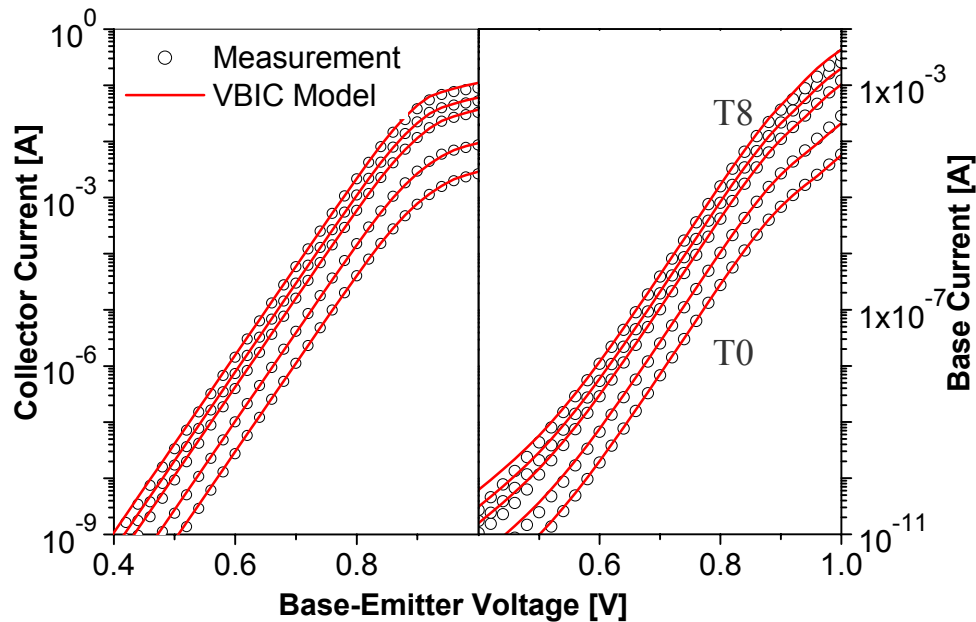


Collector-Substrate capacitance

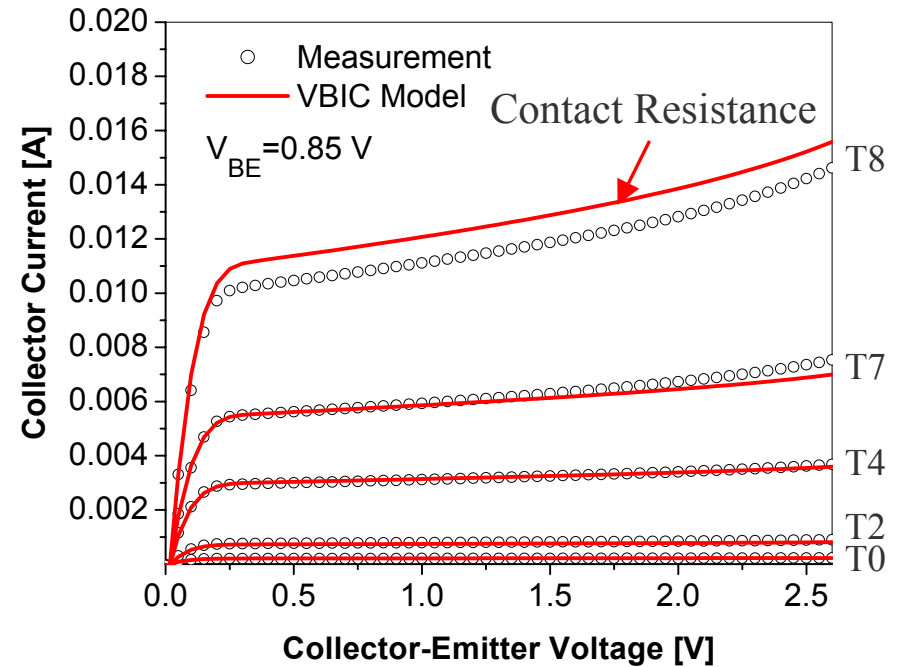
Results: DC Scaling



In all figures curves from transistors with different geometries are plotted

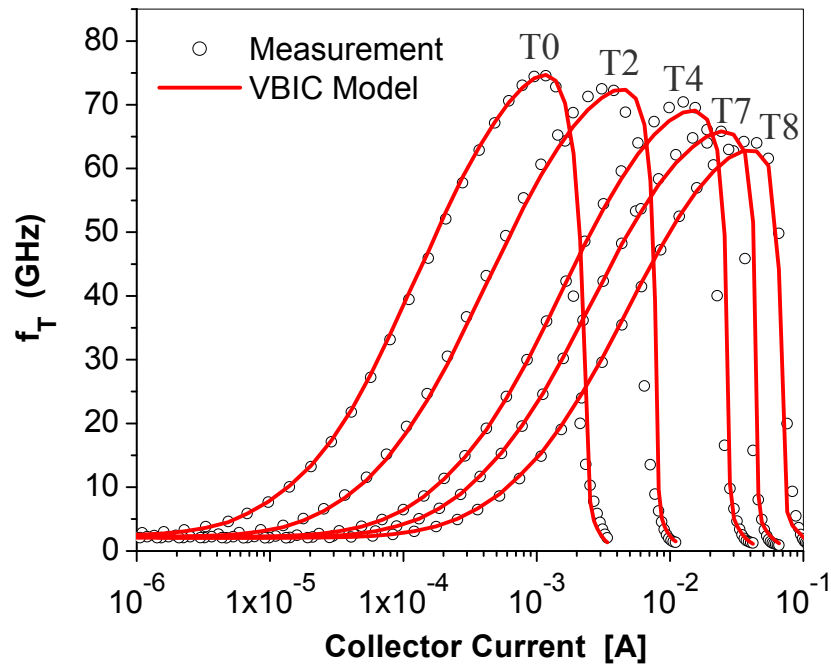


Gummel plot @ $V_{CB} = 0V$

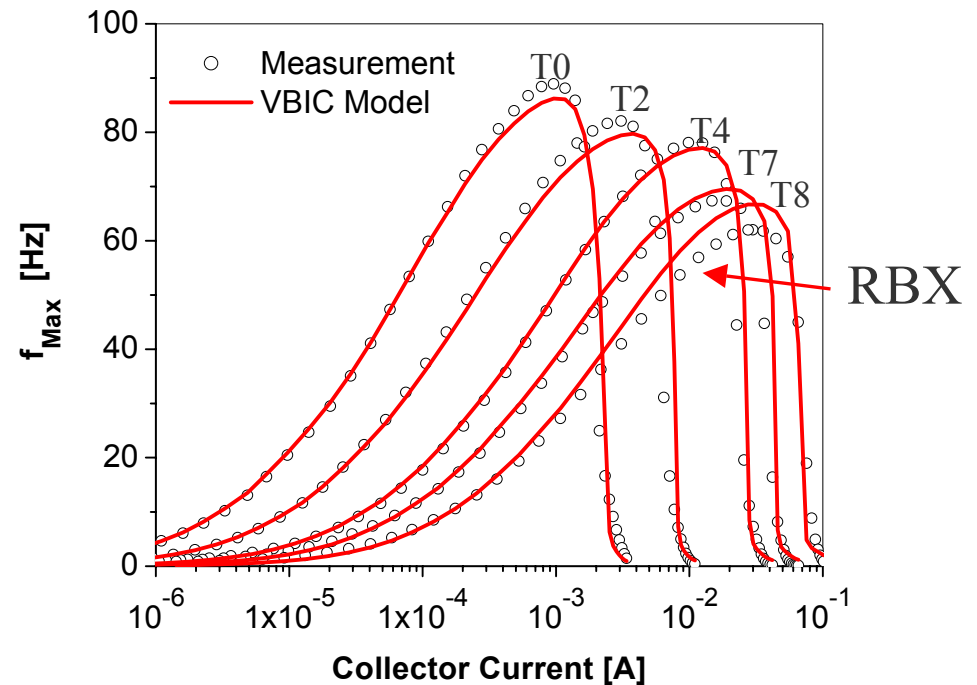


Output characteristics
@ $V_{BE} = \text{const.}$

Results: RF Scaling



f_T extracted at 5GHz,
VCE 1.5V



f_{Max} extracted at 24GHz,
VCE 1.5V

Conclusion



- Simple scaling approach implemented in IC-CAP
- Emitter length variation only over a limited range
- Special layout for multi emitter structures
- Test structures generated with Pcells
- We use only RF-Pads, no special test structures
- DC and RF model accuracy better than 10%