CODESTAR

Compact modelling of on-chip passive structures at high frequencies.

Ehrenfried Seebacher
2003-10-24

CODESTAR Partner

Partner	Funding KEuro
IMEC	623
Philips	528
TU Gent (RUG)	244
TU Eindhoven (TU/e)	397
UNI Bucharest (LMN)	178
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Total	2.604

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IST-2001-34058

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Main Goal:
Development of a code dedicated for the electromagnetic simulation of passive on-chip structures resulting in a small signal network.

- **Analysis of the test structure with the electromagnetic feel solver**
- **Systematic reduction of the net list.**
- **Resulting model will be inserted into the CAD tool.**
- **Validation of the CODESTAR code with fabrication and characterisation of test structures.**
- **Matching of the CODESTAR simulation and the measurements is the measure of the project.**

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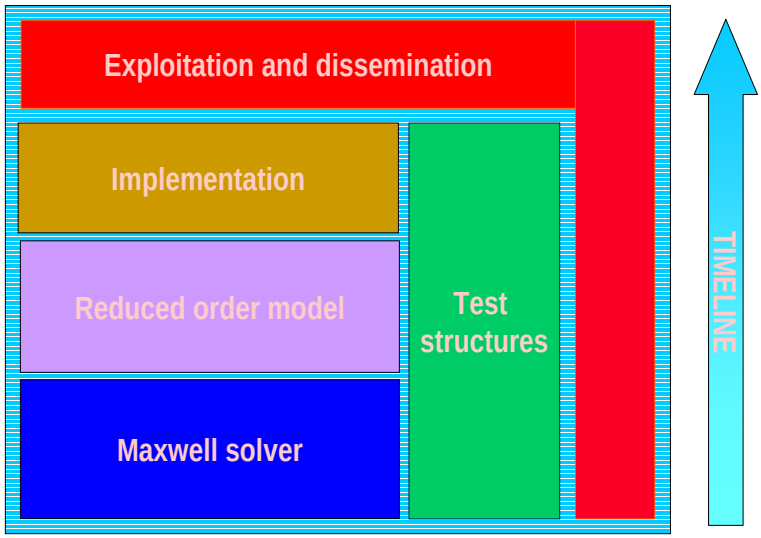
Workpackages/overview



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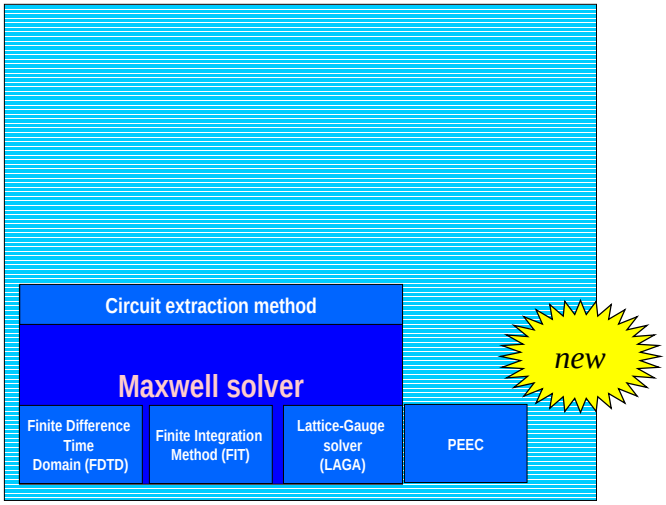
Workpackage 1



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Workpackage 2

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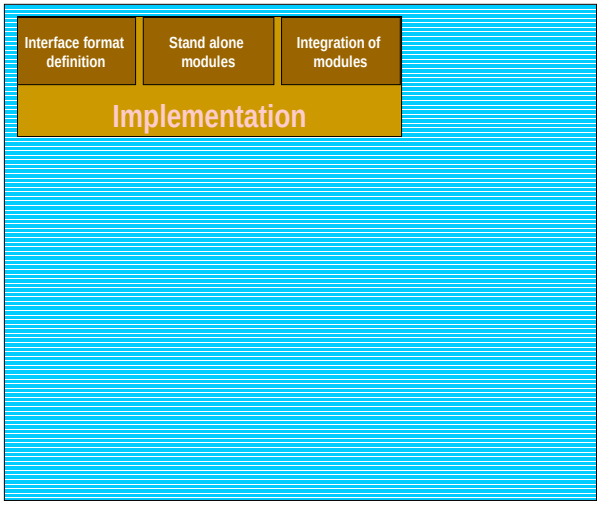
Workpackage 3



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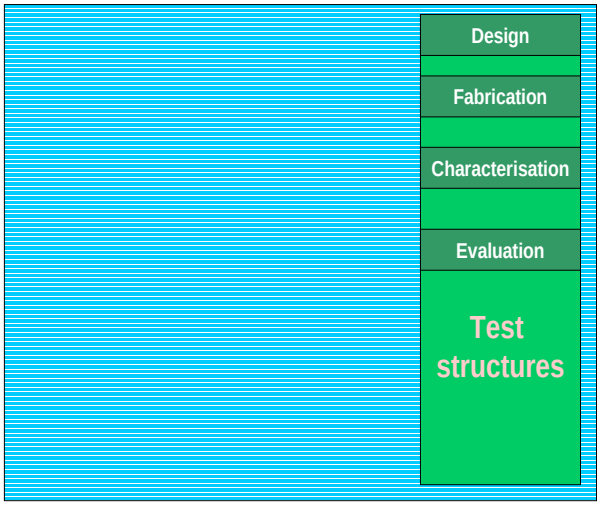
Workpackage 4



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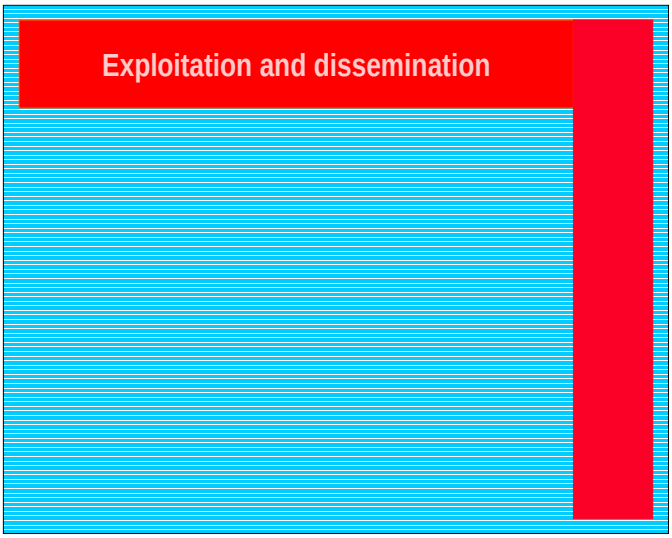
Workpackage 5



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Deliverables 1/4

Del. no.	Deliverable name	WP no.	Lead participant	Estimated person-months	Del. Type *	Security **	Delivery (proj. month)	
D0	Periodic reporting and final report	0	IMEC	6	R	Pub.	End August of each year	☑ 18-09-02 (21-03-03) 31.09.03
D1	Report of end-users requirements	4	AMS	7	R	Pub.	End March 2002	☑ In time
D2	Website	0	IMEC	1	O	Int/Pub.	End March 2002	☑ In time
D3	Project Presentation	0	IMEC	1	R	Pub.	End March 2002	☑ In time
D4	Report on interface format to the CAD environment	3	IMEC	6	R	Pub.	End May 2002	☑ In time
D5	Report on existing and new order reduction methods	2	PHILIPS	10	R	Int.	End June 2002	☑ 1 month delay

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Deliverables 2/4

Del. no.	Deliverable name	WP no.	Lead participant	Estimated person-months	Del. Type *	Security **	Delivery (proj. month)	
D6	Report on the selection of test cases	4	AMS	15	R	IST	End March 2003	☑ 2 months delay
D7	Report on the usability and adaptation of FDTD to solve the field-problem	1	TU/e	8	R	Int.	End May 2003	☑ In time
D8	Report on the usability and adaptation of FIT to solve the field-problem	1	LMN	6	R	Int.	End May 2003	☑ In time
D9	Report on the usability of the lattice-gauge (LG) solver	1	IMEC	9	R	Int.	End May 2003	☑ In time
D10	Report on circuit extraction in existing Maxwell solvers	1	Tu/E	29	R	Int.	End May 2003	☑ In time

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Deliverables 3/4

Del. no.	Deliverable name	WP no.	Lead participant	Estimated person-months	Del. Type *	Security **	Delivery (proj. month)	
D11	Demonstrator of order reduction modules	2	PHILIPS	33	D	Int.	End May 2003	☑ In time
D12	Prototype of stand-alone software modules	3	IMEC	28	D	Int.	End December 2003	On schedule
D13	Report on the characterisation of test structures	4	AMS	20	R	Int	End March 2004	
D14	Report on the characterisation (sub-) 100nm CMOS back-end patterns	4	IMEC	6	R	Int	End May 2004	
D15	Final Demonstrator of CAD tool	3	IMEC	17	D	Int.	End May 2004	

Deliverables 4/4

Del. no.	Deliverable name	WP no.	Lead participant	Estimated person-months	Del. Type *	Security **	Delivery (proj. month)
D16	Report on the benchmarking of currently available tools	4	AMS	20	R	Int.	End June 2004
D17	Report on the acceptance of the new simulation tools outside the consortium	5	IMEC	4	R	Int.	End August 2004
D18	Dissemination and use plan	5	IMEC	5	R	Int.	End August 2004

2. CODESTAR Review Meeting

Work Package 4

Ehrenfried Seebacher

WP4 Overview

Objective:

Design, fabricate and characterise test-structures in order to benchmark the tools.

WP4.1 Industrial requirements.

WP4.2 Design, Implementation and fabrication of test case.

WP4.3 Characterisation.

WP4.4 Evaluation of test case with existing tools

WP4.1 Industrial requirements

D1 Report of end-user requrenments

Standard Structures:

- Test structures of passive devices
- Interconnect test structures

- used for RF design.
- based on suggestions by RF designer in close co-operation with the characterisation and process engineers.

Challenging Structures:

- Test structures of RF pads
- Test structures of RF cells
- Test structures for Substrate Coupling Analysis

- Should illustrate the ultimate complexity a field solver can handle.
- based on suggestions by RF designer

CAD Tool Enhancements and End User Requirements

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WP4.2 (D6) Design, Implementation and fabrication of test case

Installation of a test-structure implementation plan for standard and challenging structures:

- Determine responsibilities
  - ams internal and IMEC
- Allocate resources.
  - Layout resources.
  - Design resources.
- Fix tape-in and fab out schedule
- Target date for measurement resources and equipment availability.

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Standard Structures **WP4.2**

Test-structure implementation plan Capacitors, Resistors

Device	Process	Resp.	Layout	Test-chip Name	Meas. Available
Capacitors PIP/MIM	0.35um CMOS PIP	ams K. Molnar	available	14868	yes
	0.35um BiCMOS MIM	ams K. Molnar	available	12727	yes
Resistors Rpoly2 RpolyH	0.35um CMOS	ams K. Molnar	available	12718 12719	yes

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Standard Structures **WP4.2**

Test-structure implementation plan Inductors

Device	Process	Resp.	Layout	Test-chip Name	Meas. Available
Inductors	0.35um BiCMOS/SiGe thick metal	ams K.Molnar	available	12735	Yes
	0.35um CMOS 4 metal	ams K. Molnar	available	12734	Yes
	Cu-BCB on glass	IMEC G. Carchon	available		yes
	Cu-BCB on Si	IMEC G. Carchon	available		yes

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Standard Structures **WP4.2**

Test-structure implementation plan Interconnect

Device	Process	Resp.	Layout	Testchip Name	Meas. Available
Interconnect	0.35um BiCMOS	ams Z.Huszka,	tbd	tbd	tbd
	0.35um CMOS	ams Z.Huszka,	tbd	tbd	tbd
	Al-Lowk	IMEC M. Stucchi	Available	Giga	Yes
	Cu-Lowk	IMEC M. Stucchi	Available	DD80	Yes

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Challenging Structures **WP4.2**

Test-structure implementation plan RF-Pads, LC-Cells, SCA structures

Device	Process	Resp.	Layout	Testchip Name	Meas. Available (planned)
RF-Pads	0.8um BiCMOS	ams K.Molnar, M.Mayerhofer	available	APESD08V1 LCESD08V1	No
	0.35um CMOS BiCMOS	ams K.Molnar, M.Mayerhofer	available	APESD35V2 LCESD35V2	Yes
LC-Cells	0.35um CMOS	ams K. Molnar	available	12738	No
SCA Structures	0.35um CMOS	Ams G.Rappitsch,	available	Storm	No

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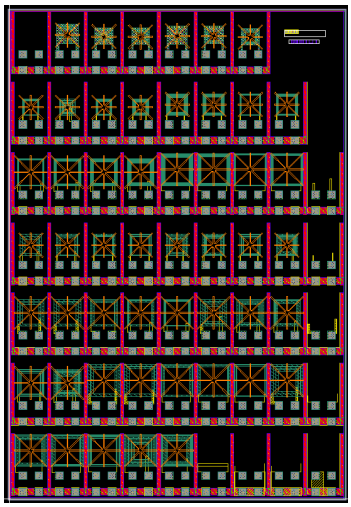
WP4.2

Selection of the test-structure for the CODESTAR benchmark:

- End-user requirements
- Physical effects.
- Based on a huge number of test-chips.
- High accurate measurement possible.
- Theoretical background.
- TCAD simulations.



Overview of test-chip layout – Spirals TM

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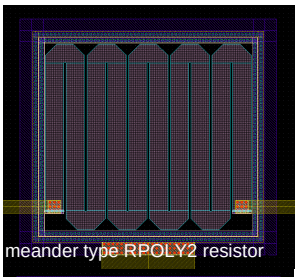
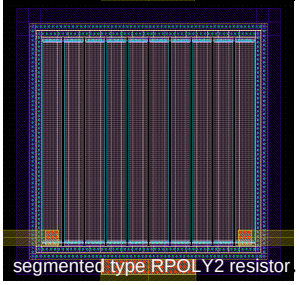
Selection of the test-structures

Resistors (Standard Structures)

- Two rpoly resistors are selected:

- meander type (bends) having high resistance
- segmented type (finger) having high resistance and increased cut-off frequency.
  - RP2, RPH layouts available.
  - Measurements are available.
  - Redesign recommended
    (no substrate contact,
    dummy device correction)


meander type RPOLY2 resistor


segmented type RPOLY2 resistor

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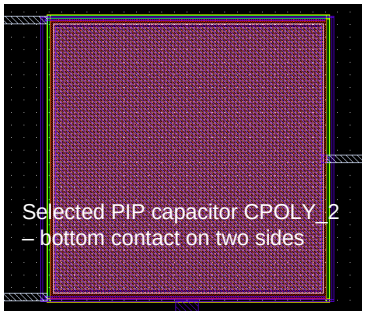
Selection of the test-structures

Capacitors (Standard Structures)

- Two PIP and one MIM capacitor are selected for CODESTAR:

- 2 PIP capacitors having different contacting schemes.
- 1 large MIM capacitor
  - Measurement is avaialable
  - Redesign recommended
    - RF-layout new (de-embedding)


Selected PIP capacitor CPOLY_2
– bottom contact on two sides

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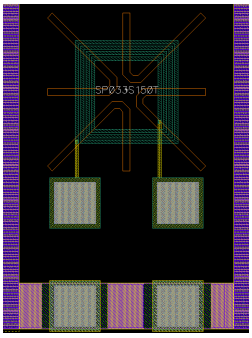
Selection of the test-structures

Spiral Inductors

(Standard Structures)

Three thick metal inductors are proposed for CODESTAR:

- Spiral I: small valued inductance with a low number of turns.
  - **The effect of stray inductance and cap is large.**
- Spiral II: large inductance
  - **with increased substrate interaction and decreasing Q.**
- Spiral III: inductance with a resonance frequency below 6GHz
  - Layout and s-parameter data up to 6 GHz are available.
  - No Redesign required



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Selection of the test-structures

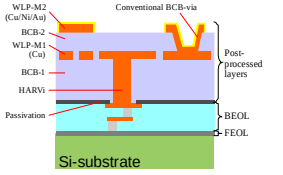
Wafer Level Packaging (WLP) integrated Inductors

(Standard Structures)

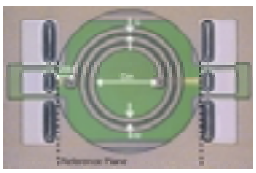
Four high Q inductors on WLP with Cu and low-k materials are proposed for CODESTAR:

- **inductor L3 with substrate contacts present at the probe tips**
- **inductor L3 without substrate contacts at the probe-tips**
- **inductor L4 with substrate contacts, without patterned poly-silicon ground shield**
- **inductor L4 with substrate contacts, with patterned poly-silicon ground shield**

No Redesign required



BCB benzo-cyclobutene



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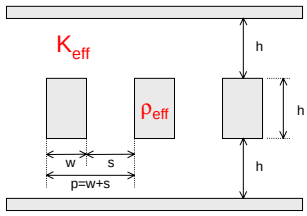
Selection of the test-structures

Interconnect test-structures
(Standard Structures)

Two high frequency structures processed on Al-SiO_2 and Cu- SiO_2 are proposed for CODESTAR:

- **microstrip and coplanar lines**
  - Signal attenuation, impedance, cross-talk.
- **2D and 3D interconnect models**
  - Dimension (w,s,p) and material change (ITSR roadmap)



2D interconnect structure

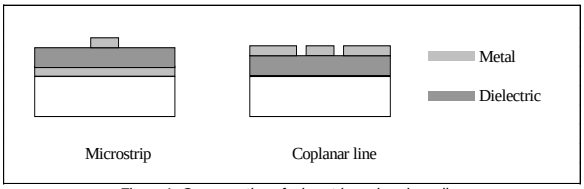
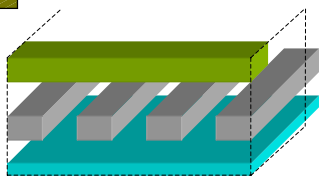


Figure 1: *Cross-section of microstrip and coplanar line*



3D interconnect structure

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Selection of the test-structures

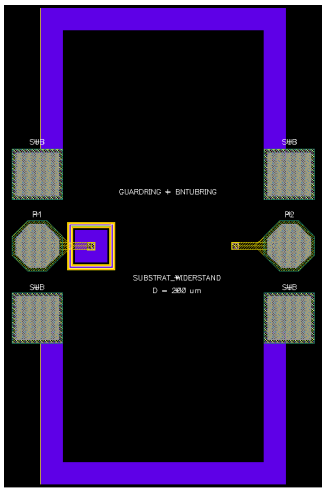
SCA STRUTURES
(Challenging Structures)

Two test-structures have been selected for CODESTAR validation purposes:

- **SCA1** : p+ guard ring symmetric with 200 um and 50um coupling distance and 16.4 um guard ring width.
- **SCA2** : p+/n+/sinker/buried-layer guard ring with 200 um and 50um coupling distance and 16.4 um p+ guard ring width and 2.3 um n+ guard ring width.

Impedance =f (guard ring, distance)

- Redesign is necessary



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Selection of the test-structures

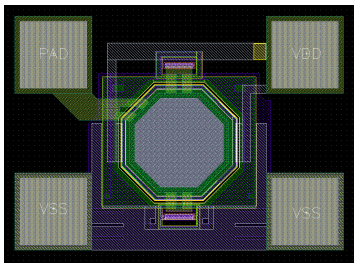
RF pads
(Challenging Structures)

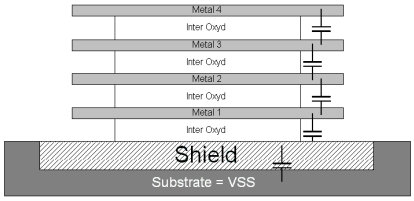
Two pads have been selected for CODESTAR validation purposes:

- Pad1: full metal pad stack ensures good bonding conditions.
- Pad2: top metal and metal 3 gives low capacitances for RF applications.

RF-pad capability:

- Signal processing (low cap)
- ESD, bonding (high cap)
  - Diode, metal stack





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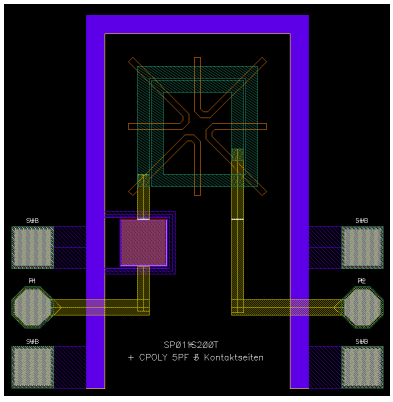
Selection of the test-structures

LC, LL- cells
(Challenging Structures)

Two LC and LL- cells have been selected for CODESTAR validation purposes:

- LC-cell: Inductor with PIP or MIM.
- LL-cell: distance variation.



Bip-AK - Oct. 23.2003
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CODESTAR Test-chip

- **Devices have been produces on different runs and test-chips.**
- **GSG structures necessary for 40GHz measurements.**
- **Not all necessary de-embadding structures (up to 20GHz) are available.**
- **Some redesigns are useful.**

S35 MPW
11.Aug-16.Nov

CODESTAR Test-chip:
Includes all selected structures with open-short-thru de-embedding
double poly, MiM cap and thick metal process

CODESTAR Test-chip

Three CODESTAR test-chips are proposed for the benchmark:

- **SiGe BiCMOS 0.35um process 2P, MIM, 4M, TM**
- **Layout finished, tape out 16.Nov.**
- **Accurate measurements are guaranteed**
  - open, short, thru de-embedding on the wafer
- **Technology file verification on the wafer.**

CODESTAR Test-chip

Three CODESTAR test-chips are proposed for the benchmark:

- **CODESTAR1:**
  - RP2,RPH, PIP, MIM, Inductor, Pads
- **CODESTAR2:**
  - LL-cells, LC-cells, SCR
  - Inductor, guarding check
- **CODESTAR3:**
  - tech file check, oxide thickness.

WP4 Overview

Design, fabricate and characterise test structures in order to benchmark the tools.

WP4.1 Industrial requirements. ✓

WP4.2 Design, Implementation and fabrication of test case. ✓

WP4.3 Characterisation. Ongoing/16.Nov

WP4.4 Evaluation of test case with existing tools