Corporate Mission

To provide the most competitive integrated mixed signal solutions focused on speed, value, and quality.

*austriamicrosystems’* experienced team empowers customers to pursue the ideal path in combining analog and digital processing through proven and perfected product and process IP.
Our Success Is Based On...

Know How

Products

Technology
Company Profile

– 1981 Austria Micro Systems founded by American Microsystems Inc. (AMI)/Voest Alpine Joint Venture

– 1993 June AMS goes public

– 2000 July groundbreaking new Fab in Graz

– 2000 August AMS returns to private status (Permira Private Equity Fund)

– 2002 March new 200 mm Fab goes on-line

– Multinational presence: 800+ employees, 12 offices worldwide
Value Chain

- **Product Definition**
- **Design**
- **Mask Generation**
- **Wafer Production**
- **Wafer Sort**
- **Assembly**
- **Test**
- **ASSPs**
- **ASICs**
- **COT**
- **Delivery to Customer**

ASICS

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Full Service Foundry

DESIGN SUPPORT
CAD tools (HIT-Kit), analog and digital IP

PROCESS CHARACTERIZATION
Spice modeling for mixed signal, RF, HV

WAFFER PRODUCTION
(100/200 mm FAB)
Mixed Signal RF and
High-Voltage Processes

BACKEND SERVICES
Test, Assembly
### Respected Number 1 Foundry (*)

<table>
<thead>
<tr>
<th>Rank</th>
<th>CMOS</th>
<th>BiCMOS</th>
<th>SiGe</th>
<th>Bipolar</th>
<th>GaAs</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TSMC</td>
<td><em>ams</em></td>
<td><em>ams</em></td>
<td>Zetex</td>
<td>UMS</td>
</tr>
<tr>
<td>2</td>
<td><em>ams</em></td>
<td>ST Micro.</td>
<td>Atmel</td>
<td>Mitel</td>
<td>TriQuint</td>
</tr>
<tr>
<td>3</td>
<td>ST Micro.</td>
<td>Philips</td>
<td>IBM</td>
<td>Philips</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Chartered</td>
<td>Alcatel</td>
<td>Philips</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Atmel</td>
<td>Atmel</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>UMC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*) Source: Future Horizons 2002 (European Chipless & IC Design House Report)
Revenue By Regions 2002

Europe 74%

Americas 19%

Asia-Pacific 7%
Process Characterisation at austriamicrosystems
Local Modelling activities

- CMOS
- BiCMOS
- SiGe
- HV CMOS
- EEPROM
- Opto

Design Documents
SPICE Modelling
Simulator Support
Verification
A Link between Design and Manufacturing
Capabilities under one Roof

Process Characterization

Design
Test
Assembly

Mask Shop

Waferfab 100mm

Waferfab 200mm

a leap ahead in mixed signal  

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Design Documents

Basic Design & Process Information

Process Parameters Documents
- Operating conditions
- Structural & geometrical parameters
- Electrical parameters
- SPICE Models
- Figures of merit (e.g. FT, FMAX)

RF-Design Documents
- RF-Devices
- RF Modeling
- Figures of merit (e.g. Qmax)

Noise Documents
- Noise Measurements
- Noise Modeling

Matching Documents
- Matching Measurements
- Matching Modeling

Design Rule Documents
- Rules, Guidelines, Recommended Layout Structures
Simulator Integration Flow

Device Models
- Measurement
- Parameter Extraction
- Statistical Modelling

Simulator Integration
- Spectre, Eldo, ..

DESIGN
- HIT-Kit, Customer

Process Characterisation

Testchips, SLM

Statistical Process Data
- MAP-Parameters

Process
Simulator Model Generation Flow

Parameter Database
modn, modp, rpoly1, cpoly...

Generation Program

Spectre
Typical
Worst Case
Monte Carlo
Stat. Corners

Eldo

ADS

20,000 model files

30 processes
## Circuit Simulators and Models

<table>
<thead>
<tr>
<th>Simulator</th>
<th>MOS-Transistor</th>
<th>Monte Carlo &amp; Matching</th>
<th>Bip-Transistor</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>BSIM3v3 Level 53</td>
<td>AMS MOS15 level15</td>
<td>SGP</td>
</tr>
<tr>
<td>Eldo</td>
<td>4.4.1</td>
<td>4.3.5</td>
<td>4.4.1</td>
</tr>
<tr>
<td>Accusim I</td>
<td>B.3</td>
<td>A.3</td>
<td>B.3</td>
</tr>
<tr>
<td>Spectre Direct</td>
<td>4.4.3</td>
<td></td>
<td>4.4.3</td>
</tr>
<tr>
<td>Spectre</td>
<td>4.4.1</td>
<td>4.3.4</td>
<td>4.4.1</td>
</tr>
<tr>
<td>Hspice</td>
<td>97.2(level 49)</td>
<td>-</td>
<td>97.2</td>
</tr>
<tr>
<td>Saber</td>
<td>4.3</td>
<td>3.2</td>
<td>-</td>
</tr>
<tr>
<td>Smash</td>
<td>3.53(level 8)</td>
<td>3.4</td>
<td>-</td>
</tr>
<tr>
<td>Pspice</td>
<td>A/D v. 8.0</td>
<td>-</td>
<td>A/D v. 8.0</td>
</tr>
<tr>
<td>Agilent-ADS</td>
<td>1.01</td>
<td>-</td>
<td>1.01</td>
</tr>
</tbody>
</table>

*Note: Some simulators may have additional versions or levels that are not explicitly listed.*
Compact Modeling for the CMOS Process

- BSIM3v3 for std. MOS transistor
- High voltage transistor modeled as sub-circuits
- JFET models for all diffusion resistors
- SGP model for all pnp (Vert,Lat)
- Subcircuit for the zener diode modeling
- Voltage and Temp. dependent Capacitance modeling
- Matching Parameter
Vertical PNP Transistor

- Standard Gummel Poon Model

Lateral PNP Transistor

- Sub-circuit lateral and vertical pnp Transistor
- Parameter extraction
  - Optimizer linked to Eldo
Analog modeling for capacitances

Voltage and temp. dependent modeling of the PIP and MIM capacitances

CPIP = 0.86 fF/µm²

CMIM = 1.25 fF/µm²
1/f Noise Characterisation
Noise Plots

SPICE Model

\[ S_{i_F} = \frac{1}{C_{OX} \cdot L_{eff}^2} \cdot KF \cdot f D \cdot f \]

BSIM3v3

\[ S_{ij} = \frac{1}{C_{OX} \cdot L_{eff}^2} \cdot \frac{I_D}{f_{EF}} \cdot f \cdot f \cdot f \]
Device Mismatch
Steps to the mismatch simulation:

- Suitable test chip (prevent Measurements from systematic Mismatch Influences)
- Accurate measurements (on wafer)
- Parameter extraction (non linear fits)

- Applying Pelgroms Law
- Simulation models (suitable for Monte Carlo)
Process & Device Characterization

HV CMOS Characterisation
Compact Modeling HV CMOS 50V & 90V Process

- Special sub-circuits for high voltage transistor model
- BSIM3v3 for std. MOS transistor
- VBIC for npn & SGP model for all pnp bipolar transistors
- JFET models for all diffusion resistors
- Subcircuit for the junction FET
- Parasitic diode modeling for all HV transistors and isolated transistors.
- SOAC - “Safe Operating Area Check” checks the allowed DC operating conditions
- Temp. modeling for -30-125degC
## Devices & Simulation Models

### 0.35 BiCMOS

<table>
<thead>
<tr>
<th>Device</th>
<th>Device Name</th>
<th>Model Name</th>
<th>Model Rev.</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3 Volt NMOS</td>
<td>NMOS</td>
<td>modn</td>
<td>2.0</td>
</tr>
<tr>
<td>3.3 Volt PMOS</td>
<td>PMOS</td>
<td>modp</td>
<td>2.0</td>
</tr>
<tr>
<td>high voltage NMOS (gate oxide)</td>
<td>NMOSH</td>
<td>modnh</td>
<td>2.0</td>
</tr>
<tr>
<td>vertical NPN bipolar transistors:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>single base, single collector</td>
<td>NPN111</td>
<td>npn111</td>
<td>2.0</td>
</tr>
<tr>
<td>vertical NPN bipolar transistors:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>multiple base, single collector</td>
<td>NPN121</td>
<td>npn121</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td>NPN132</td>
<td>npn132</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td>NPN143</td>
<td>npn143</td>
<td>2.0</td>
</tr>
<tr>
<td>vertical NPN bipolar transistors:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>multiple base, double collector</td>
<td>NPN232</td>
<td>npn232</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td>NPN243</td>
<td>npn243</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td>NPN254</td>
<td>npn254</td>
<td>2.0</td>
</tr>
<tr>
<td>Vertical PNP bipolar transistor</td>
<td>VERT10</td>
<td>vert10</td>
<td>2.0</td>
</tr>
<tr>
<td>Lateral PNP bipolar transistor</td>
<td>LAT2</td>
<td>lat2</td>
<td>2.0</td>
</tr>
<tr>
<td>Lateral PNP bipolar with buried layer</td>
<td>LAT2B</td>
<td>lat2b</td>
<td>tbd</td>
</tr>
<tr>
<td>Diode NDIFF / PSUB</td>
<td>SUBDIODE</td>
<td>nd</td>
<td>2.0</td>
</tr>
<tr>
<td>Diode PDIFF / NWELL</td>
<td>WELLDIODE</td>
<td>pd</td>
<td>2.0</td>
</tr>
<tr>
<td>Diode NWELL / PSUB</td>
<td>NWD</td>
<td>nwd</td>
<td>2.0</td>
</tr>
<tr>
<td>Diode BNWELL / PSUB</td>
<td>BNWD</td>
<td>bnwd</td>
<td>tbd</td>
</tr>
<tr>
<td>Zener diode</td>
<td>ZD2SM24</td>
<td>zd2sm24</td>
<td>2.0</td>
</tr>
<tr>
<td>POLY1-DIFF capacitor</td>
<td>NGATECAP</td>
<td>ngatecap</td>
<td>2.0</td>
</tr>
<tr>
<td>POLY1-SINKER capacitor</td>
<td>CSINK</td>
<td>csink</td>
<td>tbd</td>
</tr>
<tr>
<td>POLY1-SINKERM capacitor</td>
<td>CSINKM</td>
<td>csinkm</td>
<td>2.0</td>
</tr>
<tr>
<td>MOS Varactor</td>
<td>CVAR</td>
<td>cvar</td>
<td>2.0</td>
</tr>
<tr>
<td>PDIFF resistor</td>
<td>RDIFFP, RDIFFP3</td>
<td>rdiffp (model R)</td>
<td>rdiffp3 (model JFET)</td>
</tr>
<tr>
<td>NDIFF resistor</td>
<td>RDIFFN, RDIFFN3</td>
<td>rdiffn (model R)</td>
<td>rdiffn3 (model JFET)</td>
</tr>
<tr>
<td>NWELL resistor</td>
<td>RNWELL</td>
<td>rnwell</td>
<td>2.0</td>
</tr>
</tbody>
</table>
### Devices & Simulation Models

#### 0.35um BiCMOS

<table>
<thead>
<tr>
<th>Device</th>
<th>Device Name</th>
<th>Model Name</th>
<th>Model Rev.</th>
</tr>
</thead>
<tbody>
<tr>
<td>POLY2 resistor</td>
<td>RPOLY2</td>
<td>rpoly2</td>
<td>2.0</td>
</tr>
<tr>
<td>CPOLY capacitor</td>
<td>CPOLY</td>
<td>cpoly</td>
<td>2.0</td>
</tr>
</tbody>
</table>

#### RPOLYH MODULE

<table>
<thead>
<tr>
<th>Device</th>
<th>Device Name</th>
<th>Model Name</th>
<th>Model Rev.</th>
</tr>
</thead>
<tbody>
<tr>
<td>POLYH resistor</td>
<td>RPOLYH</td>
<td>rpolyh</td>
<td>2.0</td>
</tr>
</tbody>
</table>

#### 5 VOLT MODULE

<table>
<thead>
<tr>
<th>Device</th>
<th>Device Name</th>
<th>Model Name</th>
<th>Model Rev.</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 Volt NMOS</td>
<td>NMOSM</td>
<td>modnm</td>
<td>2.0</td>
</tr>
<tr>
<td>5 Volt PMOS</td>
<td>PMOSM</td>
<td>modpm</td>
<td>2.0</td>
</tr>
<tr>
<td>high voltage NMOS (mid-oxide)</td>
<td>NMOSMH</td>
<td>modnmh</td>
<td>2.0</td>
</tr>
</tbody>
</table>

#### CMIM MODULE

<table>
<thead>
<tr>
<th>Device</th>
<th>Device Name</th>
<th>Model Name</th>
<th>Model Rev.</th>
</tr>
</thead>
<tbody>
<tr>
<td>METAL2-METALC capacitor</td>
<td>CMIM</td>
<td>cmim</td>
<td>2.0</td>
</tr>
</tbody>
</table>
## 0.8um HBT BiCMOS

<table>
<thead>
<tr>
<th>Device</th>
<th>Device Name</th>
<th>Model name</th>
<th>Model Rev.</th>
</tr>
</thead>
<tbody>
<tr>
<td>vertical npn bipolar tr.</td>
<td>NPN#C#B#E</td>
<td>npn#C#B#E</td>
<td>2.0</td>
</tr>
<tr>
<td>mos varactor</td>
<td>CVAR</td>
<td>cvar</td>
<td>2.0</td>
</tr>
<tr>
<td>inductors</td>
<td>SPXXXAY</td>
<td>spxxxay</td>
<td>2.0</td>
</tr>
<tr>
<td>poly1-polyb capacitor</td>
<td>CPOLYBRF</td>
<td>cpolybrf</td>
<td>1.0</td>
</tr>
<tr>
<td>poly1 resistor</td>
<td>RPOLY1RF</td>
<td>rpoly1rf</td>
<td>1.0</td>
</tr>
<tr>
<td>polyb resistor</td>
<td>RPOLYBRF</td>
<td>rpolybrf</td>
<td>1.0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Simulator</th>
<th>Simulator</th>
<th>CAD Integration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spectre</td>
<td>Spectre 4.4.6</td>
<td>Cadence IC446</td>
</tr>
<tr>
<td>Gemini/ADS</td>
<td>HPEESOFSIM v.170 rev. 200</td>
<td>Agilent ADS v2001</td>
</tr>
</tbody>
</table>
Vertical NPN bipolar transistor

NPN121, NPN2xy, (cbe), W=0.8μm
Scalable VBIC bip. transistor models
  • state of the art model
    - HP-ADS, Spectre, Saber, (ELDO)
Scalable SGP bip. transistor models
  • improved SGP model
    - compatible for all simulators

Temperature modeling from -50 - 125(200)degC

Parameter Extraction from DC-, S-Parameter and Noise measurements
S-Parameter measurements up to 40GHz
Extraction of cutoff frequency $F_T$ and maximum oscillation frequency $F_{MAX}$ as figures of merit
RF MOS Transistor Modeling

BSIM3v3.2 & Sub-circuit

- gate res, substrate netwerk
- fixed gate length (0.35um)
- different with
- number of fingers
Varactor Sub-circuit & C-V Characteristics
Inductor Modelling

There is a library with 15 different square inductors with values ranging from 1.4 nH up to 20 nH. The layout of the inductors is fixed. All inductors are modeled with a lumped RLC equivalent circuit.

---

Here are four graphs showing the measured and simulated effective series inductance and quality factor of spiral SP025C2 as a function of frequency.

- Top left: Schematic of the inductor model.
- Top right: Graph showing the inductance (L) vs. frequency.
- Bottom left: Graph showing the resistance (R) vs. frequency.
- Bottom right: Graph showing the quality factor (Q) vs. frequency.

---

Note: The graphs show a clear difference between measured and simulated data, especially at higher frequencies.
The poly1-polyb capacitor is built up of:

- polyb (top-plate) - insulator (thin oxide) - poly1 (bottom-plate).

20 capacitors with values ranging from 0.2 pF – 10 pF and different W/L-ratios were measured and fitted. A scaleable model was generated based on these measurements.

Measured (x) and simulated (-) series capacitance (W=33.4 µm, L=33.4 µm) as a function of frequency.
Software & Measurement Equipment
S-Parameter Measurement capabilities

Measurement Equipment

- Cascade Summit Probe Station
- Parameter - Analyzer
- Network - Analyzer
- Cap-Meters

Extraction Tools

- UTMOST
- IC-Cap
- WinCal 2.3
- Matlab
- LabView
UTMOST
for active devices

IC-Cap
for active and passive devices,
interface to ADS

WinCal 2.3
for passive devices, runs on PC

Matlab
params optimizer

LabView  dc measurements (resistor, jfet, bip transistor models)
MOS AK

Infineon, Philips, EPFL, Agilent, Motorola

Bip-AK

Infineon, Philips, Alcatel, Atmel, Bosch, Motorola, IHP

TU-Graz, TU-Wien

Supervision of dissertation and diplom thesis

CODESTAR (Compact moDEling of on-chip passive Structures At high fRequencies)

Outlook

CMOS:
- BSIM3v3, BSIM4, EKV3

BiCMOS:
- VBIC, HICUM/Mextram, HF - Noise

HV-CMOS:
- BSIM3v3 Sub-circuit, AMS HV-CMOS

Opto
- Photo Diode model