

VBIC 1.20 Benchmarking

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BIP-AK

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X-FAB Key Facts

- Facilities:** Erfurt, Germany (Headquarters)
Lubbock, TX, USA
Plymouth, UK
- Capacities:** ~ 28.000 Eight Inch equiv.
wafer starts per month
- Processes:** 1.0 – 0.35 μm mixed signal CMOS and BiCMOS
special: BCD, SOI, MEMS
- Services:** Design Kits, Prototyping
- Employees:** ~ 1.000 worldwide
- Sales (2004):** \$ 177 m (€ 142,4 m)*

*unaudited



History

- > 1960s
- > Production of microelectronics begins at the former Funkwerk Erfurt

- > 1968
- > The semiconductor collective VEB Mikroelektronik Erfurt is founded to produce
- > semiconductor components

- > 1989
- > 35m MOS IC (μ P, dRAM, ..)
- > 150m Diodes and MOSFET

- > 1990 - 1999
- > The tradition-rich firm is privatized in stages
- > Beginning of the 90s two companies:
 - > => Thesys Gesellschaft fuer Mikroelektronik mbH
 - > => X-FAB Gesellschaft zur Fertigung von Wafern mbH

History

- > 1999
- > ELEX N.V. becomes majority shareholder of Thesys in 1999
- > spins off its ASIC and ASSP business into today`s Melexis GmbH

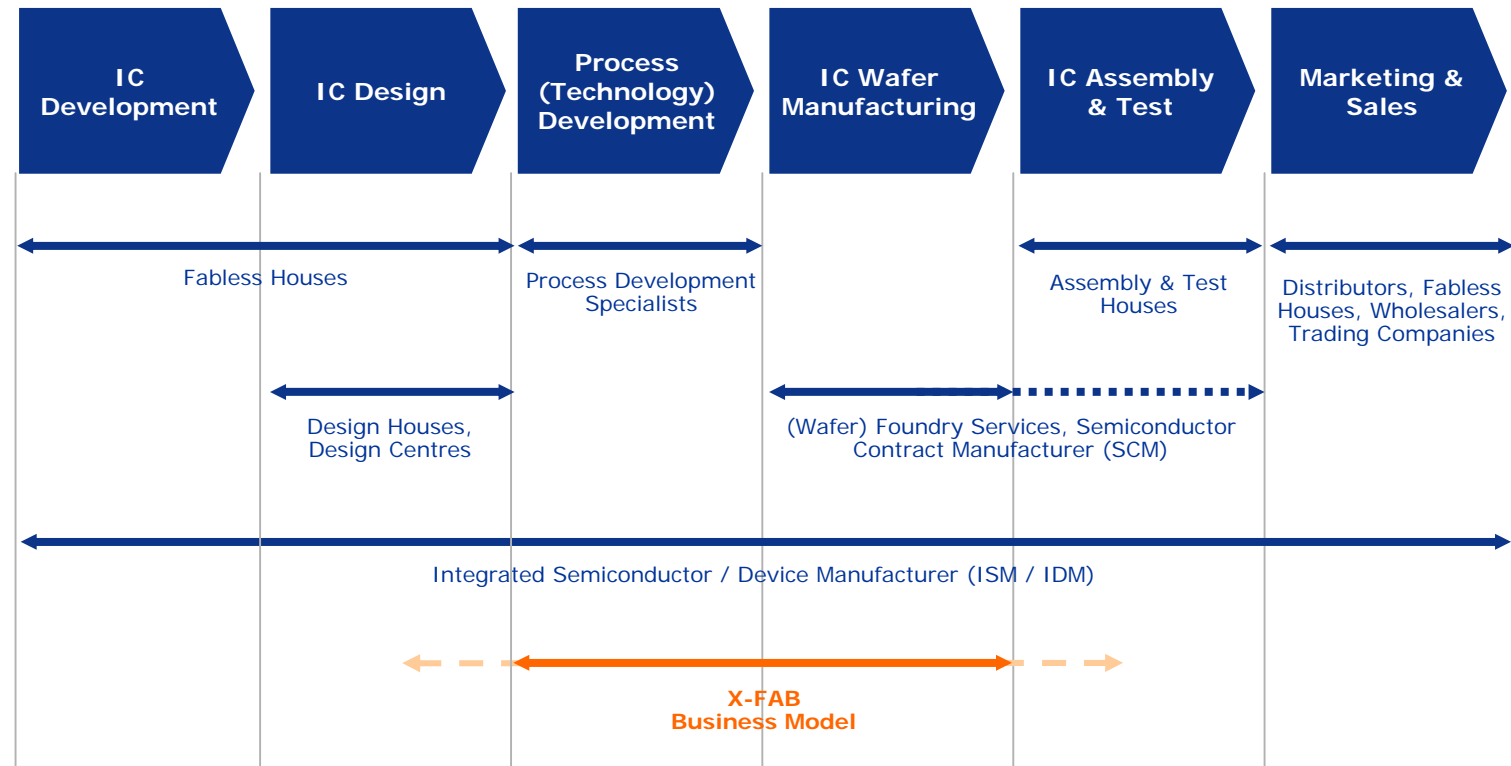
- > foundry business of Thesys Mikroelektronik
- > and X-FAB Gesellschaft zur Fertigung von Wafern mbH

- > => X-FAB Semiconductor Foundries GmbH

- > 2000
- > X-FAB Texas Inc. in Lubbock, Texas
- > becomes a subsidiary firm of X-FAB Semiconductor Foundries GmbH

- > 2001
- > X-FAB Semiconductor Foundries GmbH becomes a private limited company
- > => X-FAB Semiconductor Foundries AG
- > 2002
- > X-FAB Semiconductor Foundries acquires the Zarlink Plymouth Fab
- > The new named X-FAB UK Ltd. becomes a subsidiary of the
- > X-FAB Group

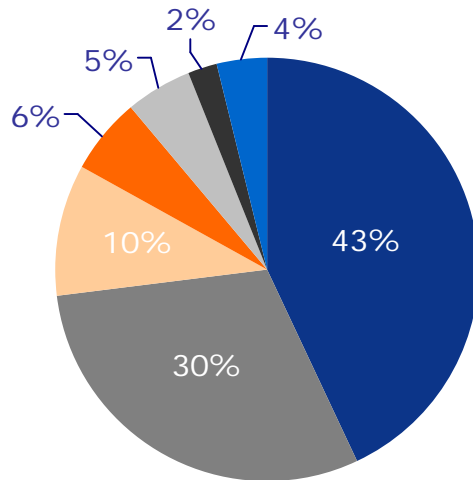
Our Business Model



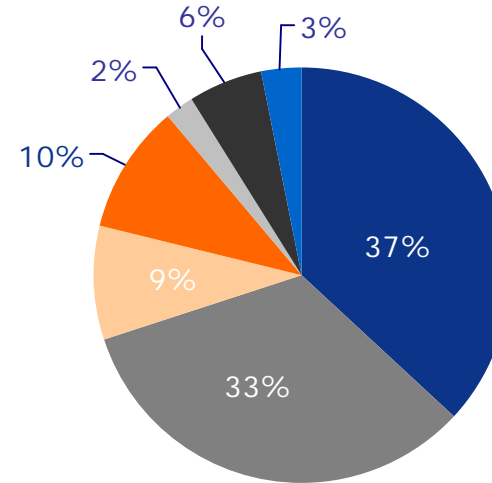
- > X-FAB is a **PURE-PLAY FOUNDRY**
 - we specialize in the manufacturing of integrated circuits for our customers
- > X-FAB does not design ICs for internal consumption

Market Segments

2003



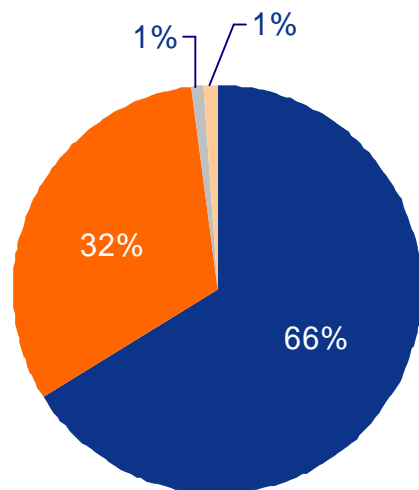
2004



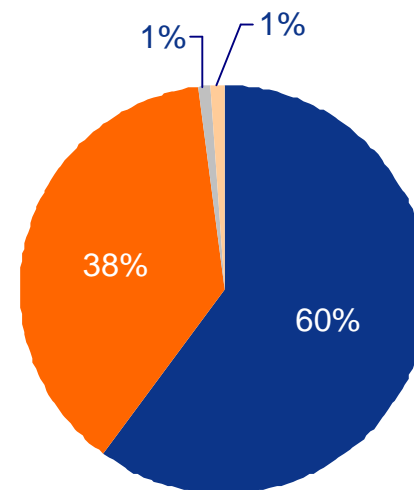
- Automotive
- Communications
- Industrial
- Consumer
- Others
- PC & Peripherals
- Medical

Sales by Customers' Origin

2003



2004



EMEA

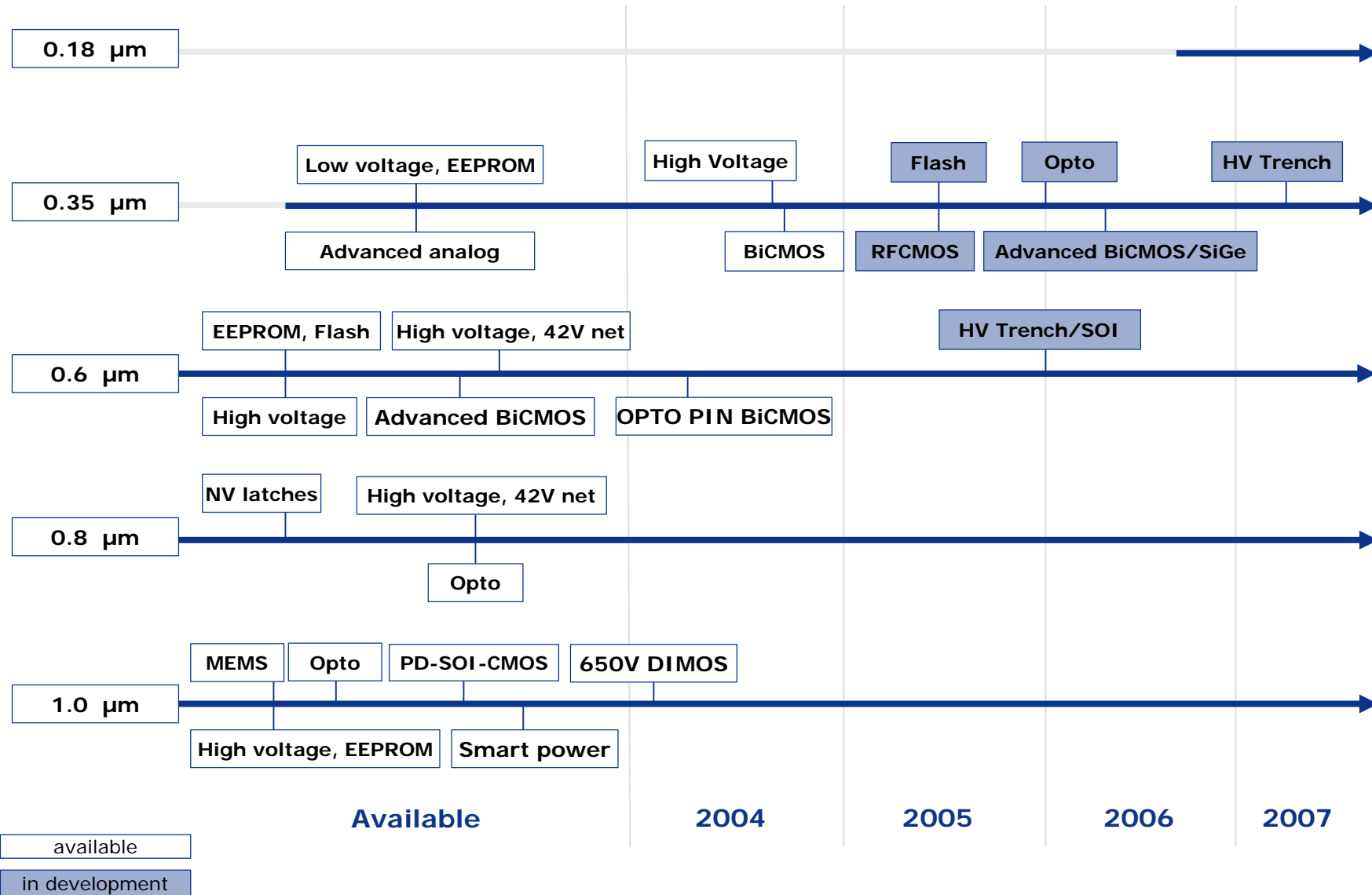
North America

Asia Pacific

Japan



Mixed-Signal Process Evolution / Roadmap



Modular Technologies

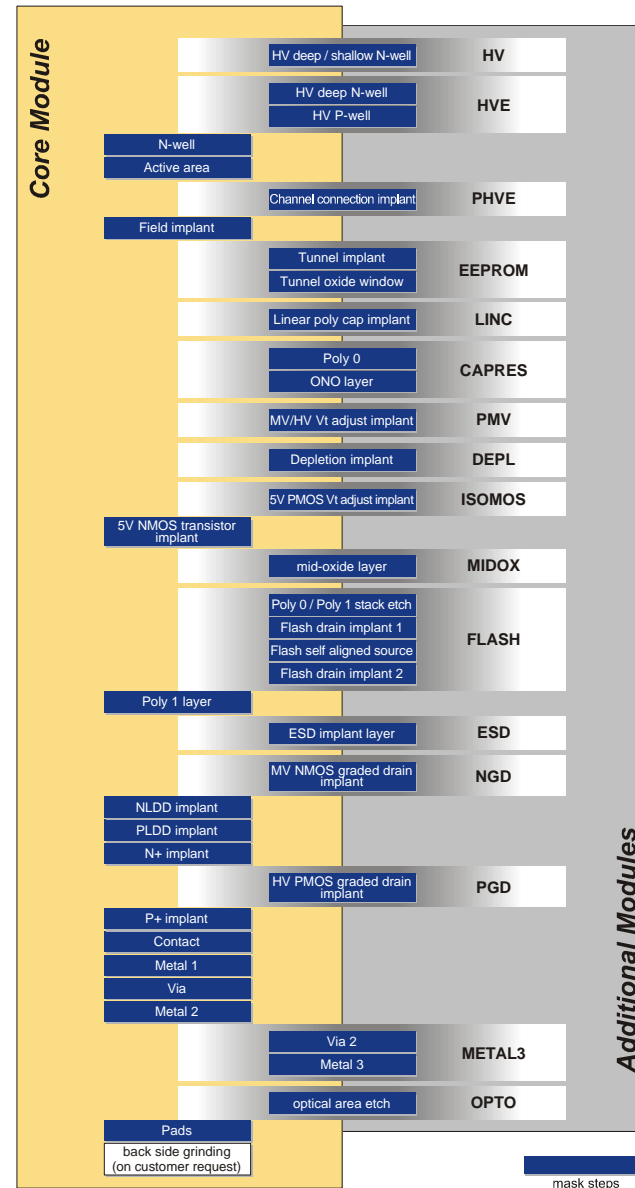
Please enter your selection!

MODULES	REQUIRES	REQUIRED BY
1: CORE <input checked="" type="checkbox"/>		all
2: CAPRES <input type="checkbox"/>		
3: LINC <input type="checkbox"/>	2	
4: MIDOX <input type="checkbox"/>		
5: PMV <input type="checkbox"/>	4	
6: NGD <input type="checkbox"/>	4	
7: EEPROM <input type="checkbox"/>	2 5 6	
8: FLASH <input type="checkbox"/>	7 14	
9: PGD <input type="checkbox"/>	5	
10: HV <input type="checkbox"/>	4	
11: HVE <input type="checkbox"/>	10	
12: PHVE <input type="checkbox"/>	11	
13: ISOMOS <input type="checkbox"/>		
14: METAL3 <input type="checkbox"/>		
15: OPTO <input type="checkbox"/>		
16: ESD <input type="checkbox"/>		
17: DEPL. <input type="checkbox"/>	4	

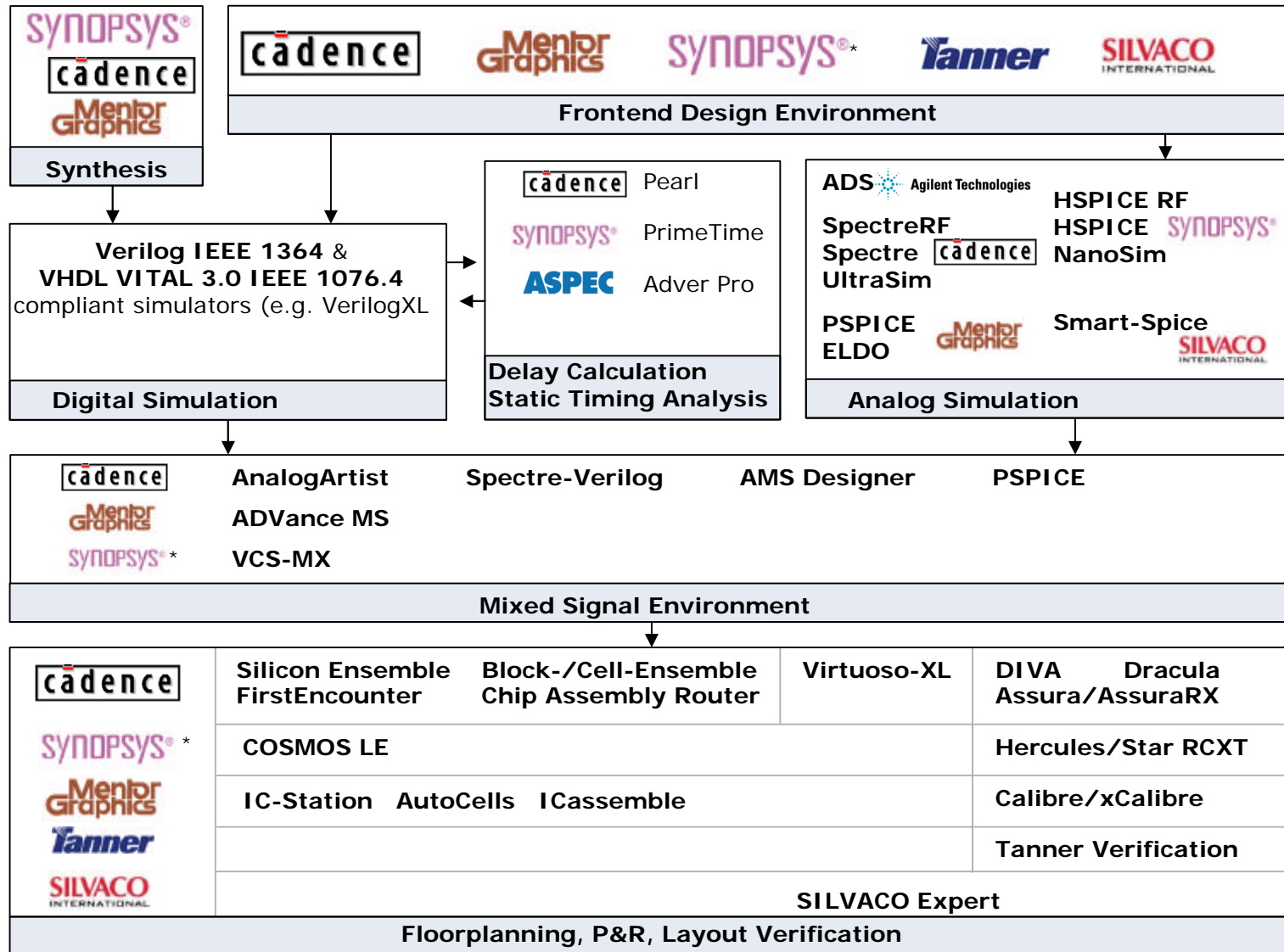
RESULTS

technology	masks	layers
name H1111	11	14

HELP OK



Supported Design Environments



*) Design Kits in development

A lecture on VBIC v1.15 was given by

Gerhard Rappitsch

“VBIC – Simulator Implementation and Benchmarking”

BIP_AK 2003

The conclusion was that VBIC v1.15 is implemented correctly for most of the simulators

Some facts will be added in the following regarding VBIC v1.20

VBIC V1.20 updates (24 September 1999)

- Base-emitter breakdown model added (**IBBE, NBBE, VBBE**)
- Reach-through model added for B-C depletion capacitance (**VRT, ART**)
- **DTEMP** local temperature difference parameter added
- **NKF** high current beta rolloff parameter added
- Temperature dependence added to IKF (**XIKF**)
- Ability to select SGP qb formulation added (**QBM**)
- Ability to separate IS for fwd and rev added (**ISRR,**)
- Fixed collector-substrate capacitance added (**CCSO**)
- Separate temperature coefficients added for RCX, RBX, RBP

- **VERS** and **VREV** (version revision) parameters added
- bug in psibi mapping with temperature fixed
- bugs in electrothermal derivatives and solver stamp fixed
- polarity of some branches reversed

Model Implementation

Simulator	Version	VBIC1.15			VBIC1.20		
		Level	VERS	VREV	Level	VERS	VREV
Spectre	5	vbic	1.15		vbic	1.2	0
ELDO	5.6	21					
ELDO	6.5	8	1.15		8	1.2	0
HSPICE	2005.3	4 (VBIC95)	-		9 (VBIC99)	-	-
Agilent-ADS	2003	vbic			-	-	-
SmartSpice	2.4	5	1.1	5	5	1.2	0
SmartSpice	2.16	4	?	?	?	?	?
PSPICE		-			-		

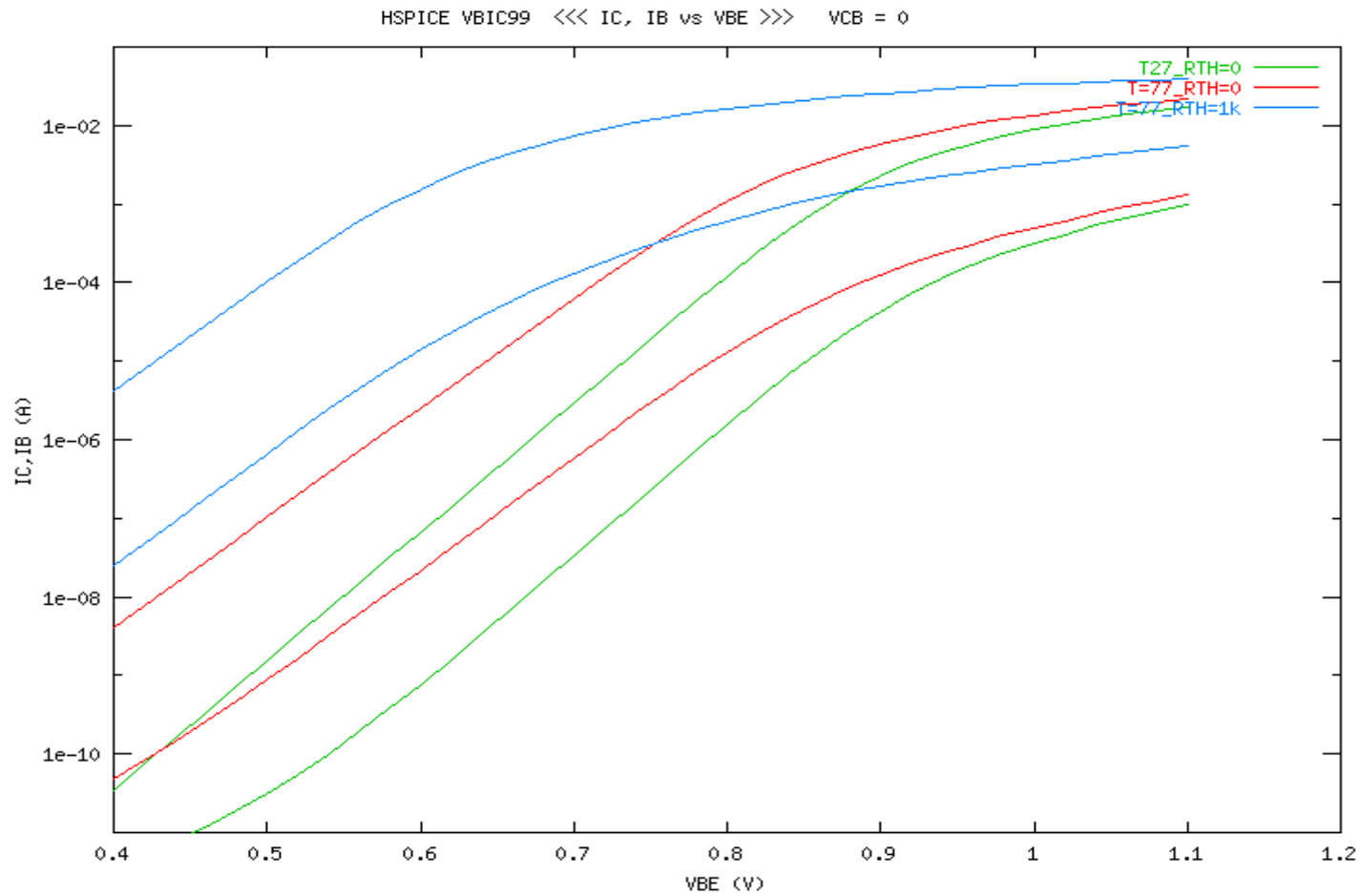
Forward Gummel
Reverse Gummel
Reverse IBvsVB
ICvsVC
H21

T=27, 77 deg C

Parameter Set:

- a) real V1.2 set
(QPM=0 => Qb equation compatible to SGP)
- b) use of V1.15 parameters only
(QBM=1 => Qb equation of V1.15)

HSPICE benchmarking problems



Simulation: HSPICE_2005.3

HSPICE benchmarking problems

Simulation results compared to Spectre v1.20: diff [%]

FG: VB=0.4.. 1.1V VCB=0

Model: b (use of V1.15 parameters only)

VERS	TEMP	RTH	HSPICE_05SP1	HSPICE_03 *	ELDO	SmartSpice	Spectre_v1.15
1.2	27	0	0	0	0	0	0
1.15	27	0	0	0	0	*	*
1.2	27	1k	0	0	0	0	0
1.15	27	1k	0	0	0	*	*
1.2	77	0	0	0	0	0	0
1.15	77	0	0	0	0	*	*
1.2	77	1k	0	>100	0	0	0
1.15	77	1k	0	0	0	*	*

HSPICE_03: HSPICE 2003, HSPICE 2003-SP1, HSPICE 2005.3

HSPICE_05: HSPICE 2005.3-SP1

HSPICE benchmarking problems

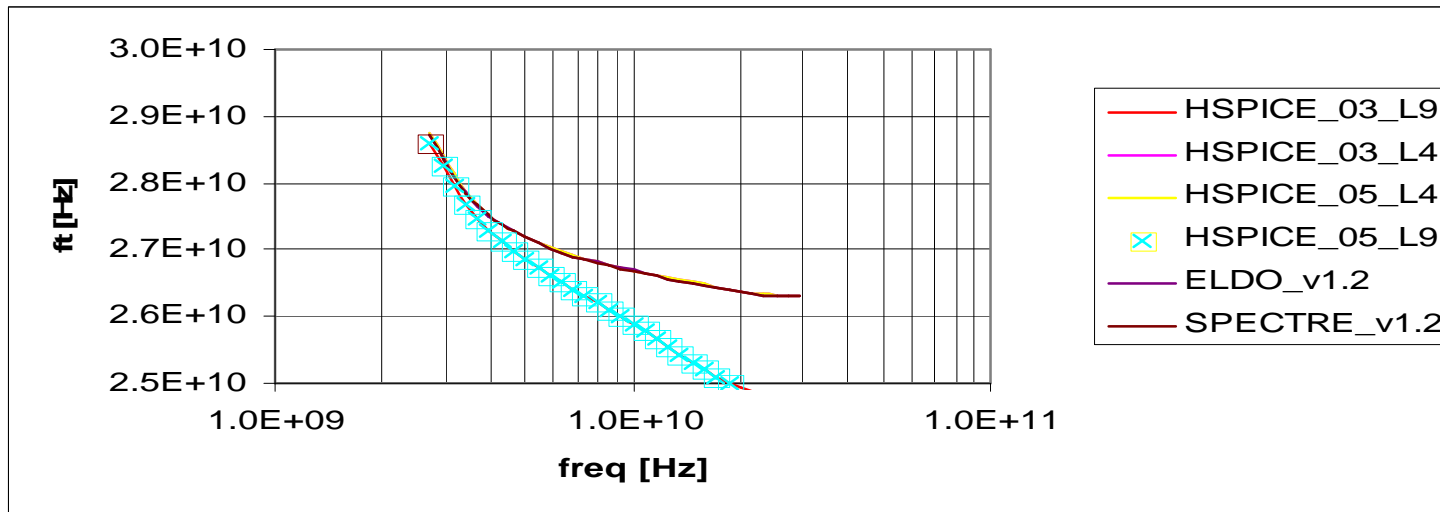
Simulation results compared to Spectre v1.20: diff [%]

Model: b (use of V1.15 parameters only / TD= 2p)

H21: VB=0.88V VCE=2.5V max diff at freq= 30GHz

H21	VERS	HSPICE_05SP1	HSPICE_03 *	ELDO
MAG	1.20	4	4	0
MAG	1.15	0	0	0
PHASE	1.20	1	1	0
PHASE	1.15	0	0	0

f_t calculated by linreg (mag(h21[dB]), log (freq)) around a given freq



HSPICE_03: HSPICE 2003, HSPICE 2003-SP1, HSPICE 2005.3

HSPICE_05: HSPICE 2005.3-SP1

- ELDO linked to ICCAP:

in case of convergence problems at high current
ICCAP does not continue

under certain conditions $I_{sub}=0$

- HSPICE default values:

v1.15: XRB, XRC, XRE, XRS= 1

v1.20: XRBI, XRBX, XRCI, XRCX= 0

- VBIC1.20 is available in many simulators but not in ADS
- Simulator benchmarking is time-consuming but necessary
- mostly there is self-consistency of the simulator results
- remaining problems must be solved

Thank you for your attention.