VBIC 1.20 Benchmarking

Axel Hammer
BIP-AK
28 October 2005, Reutlingen
**Facilities:** Erfurt, Germany (Headquarters)  
Lubbock, TX, USA  
Plymouth, UK

**Capacities:** ~ 28,000 Eight Inch equiv. wafer starts per month

**Processes:** 1.0 – 0.35 µm mixed signal CMOS and BiCMOS  
special: BCD, SOI, MEMS

**Services:** Design Kits, Prototyping

**Employees:** ~ 1,000 worldwide

**Sales (2004):** $ 177 m (€ 142,4 m)*
1960s
Production of microelectronics begins at the former Funkwerk Erfurt

1968
The semiconductor collective VEB Mikroelektronik Erfurt is founded to produce semiconductor components

1989
35m MOS IC (μP, dRAM, ..)
150m Diodes and MOSFET

1990 - 1999
The tradition-rich firm is privatized in stages
Beginning of the 90s two companies:

=> Thesys Gesellschaft fuer Mikroelektronik mbH
=> X-FAB Gesellschaft zur Fertigung von Wafern mbH
History

> 1999
> ELEX N.V. becomes majority shareholder of Thesys in 1999
> spins off its ASIC and ASSP business into today`s Melexis GmbH
> foundry business of Thesys Mikroelektronik
> and X-FAB Gesellschaft zur Fertigung von Wafern mbH
> =>  X-FAB Semiconductor Foundries GmbH

> 2000
> X-FAB Texas Inc. in Lubbock, Texas
> becomes a subsidiary firm of X-FAB Semiconductor Foundries GmbH

> 2001
> X-FAB Semiconductor Foundries GmbH becomes a private limited company
> =>  X-FAB Semiconductor Foundries AG

> 2002
> X-FAB Semiconductor Foundries acquires the Zarlink Plymouth Fab
> The new named X-FAB UK Ltd. becomes a subsidiary of the
> X-FAB Group
> X-FAB is a **PURE-PLAY FOUNDRY**

- we specialize in the manufacturing of integrated circuits for our customers

> X-FAB does not design ICs for internal consumption
## Sales by Customers' Origin

<table>
<thead>
<tr>
<th>Year</th>
<th>EMEA</th>
<th>North America</th>
<th>Asia Pacific</th>
<th>Japan</th>
</tr>
</thead>
<tbody>
<tr>
<td>2003</td>
<td>66%</td>
<td>32%</td>
<td>1%</td>
<td>1%</td>
</tr>
<tr>
<td>2004</td>
<td>60%</td>
<td>38%</td>
<td>1%</td>
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Supported Design Environments

**Frontend Design Environment**
- Synthesis
  - Verilog IEEE 1364 & VHDL VITAL 3.0 IEEE 1076.4 compliant simulators (e.g. VerilogXL)

**Digital Simulation**
- Synthesis
  - Digital Simulation
    - Verilog IEEE 1364 & VHDL VITAL 3.0 IEEE 1076.4 compliant simulators (e.g. VerilogXL)
    - Synthesis
      - AnalogArtist
        - ADVance MS
          - VCS-MX
    - Digital Simulation
      - Synthesis
        - Synopsys
          - PrimeTime
          - Adver Pro
    - Digital Simulation
      - Synthesis
        - ASPEC
          - Pearl
          - PrimeTime
          - Adver Pro
      - Synthesis
        - ADVance MS
          - VCS-MX

**Delay Calculation**
- Static Timing Analysis
  - Synthesis
    - Synopsys
      - PrimeTime
      - Adver Pro
    - Synthesis
      - ASPEC
        - Pearl
        - PrimeTime
        - Adver Pro
      - ADVance MS
        - VCS-MX

**Analog Simulation**
- Analog Simulation
  - AnalogArtist
  - Spectre-Verilog
  - AMS Designer
  - PSPICE

**Mixed Signal Environment**
- Mixed Signal Environment
  - Silicon Ensemble
    - First Encounter
  - Block-/Cell-Ensemble
    - Chip Assembly Router
  - Virtuoso-XL
  - DIVA
  - Dracula
    - Assura/AssuraRX
  - COSMOS LE
  - IC-Station
  - AutoCells
  - ICassemble
  - Virtuoso-XL
  - DIVA
    - Dracula
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                                                                                                                                                                                                      - Assura/AssuraRX
                                                                                                                                      *) Design Kits in development

**Floorplanning, P&R, Layout Verification**
- Floorplanning, P&R, Layout Verification
  - SILVACO Expert

The mixed signal foundry experts.
A lecture on VBIC v1.15 was given by

Gerhard Rappitsch
“VBIC – Simulator Implementation and Benchmarking”
BIP_AK 2003

The conclusion was that VBIC v1.15 is implemented correctly for most of the simulators

Some facts will be added in the following regarding VBIC v1.20
VBIC V1.20 updates  (24 September 1999)
- Base-emitter breakdown model added (IBBE, NBBE, VBBE)
- Reach-through model added for B-C depletion capacitance (VRT, ART)
- DTEMP local temperature difference parameter added
- NKF high current beta rolloff parameter added
- Temperature dependence added to IKF (XIKF)
- Ability to select SGP qb formulation added (QBM)
- Ability to separate IS for fwd and rev added (ISRR, )
- Fixed collector-substrate capacitance added (CCSO)
- Separate temperature coefficients added for RCX, RBX, RBP

- VERS and VREV (version revision) parameters added
- bug in psibi mapping with temperature fixed
- bugs in electrothermal derivatives and solver stamp fixed
- polarity of some branches reversed
## Model Implementation

<table>
<thead>
<tr>
<th>Simulator</th>
<th>Version</th>
<th>VBIC1.15</th>
<th>VBIC1.20</th>
</tr>
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<tbody>
<tr>
<td></td>
<td></td>
<td>Level</td>
<td>VERS</td>
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<tr>
<td>Spectre</td>
<td>5</td>
<td>vbi1.15</td>
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</tr>
<tr>
<td>ELDO</td>
<td>5.6</td>
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<td>ELDO</td>
<td>6.5</td>
<td></td>
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<tr>
<td>HSPICE</td>
<td>2005.3</td>
<td>4 (VBIC95)</td>
<td></td>
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<tr>
<td>Agilent-ADS</td>
<td>2003</td>
<td>vbi</td>
<td></td>
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<tr>
<td>SmartSpice</td>
<td>2.4</td>
<td>5</td>
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<tr>
<td>SmartSpice</td>
<td>2.16</td>
<td>4</td>
<td>?</td>
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<tr>
<td>PSPICE</td>
<td>-</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Forward Gummel
Reverse Gummel
Reverse IBvsVB
ICvsVC
H21

T=27, 77 deg C

Parameter Set:

a) real V1.2 set
   (QPM=0 => Qb equation compatible to SGP)

b) use of V1.15 parameters only
   (QBM=1 => Qb equation of V1.15)
Simulation: HSPICE_2005.3
Simulation results compared to Spectre v1.20: diff [%]

FG: VB=0.4.. 1.1V VCB=0
Model: b (use of V1.15 parameters only)

<table>
<thead>
<tr>
<th>VERS</th>
<th>TEMP</th>
<th>RTH</th>
<th>HSPICE_05SP1</th>
<th>HSPICE_03</th>
<th>ELDO</th>
<th>SmartSpice</th>
<th>Spectre_v1.15</th>
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<td>0</td>
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<td>1.15</td>
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<td>27</td>
<td>1k</td>
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<tr>
<td>1.2</td>
<td>77</td>
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<tr>
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<td>1.15</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>*</td>
<td>*</td>
</tr>
</tbody>
</table>

HSPICE_03: HSPICE 2003, HSPICE 2003-SP1, HSPICE 2005.3
HSPICE_05: HSPICE 2005.3-SP1
Simulation results compared to Spectre v1.20: diff [%]

Model: b (use of V1.15 parameters only / TD= 2p)

H21: VB=0.88V VCE=2.5V max diff at freq= 30GHz

<table>
<thead>
<tr>
<th></th>
<th>VERS</th>
<th>HSPICE_05SP1</th>
<th>HSPICE_03</th>
<th>ELDO</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAG</td>
<td>1.20</td>
<td>4</td>
<td>4</td>
<td>0</td>
</tr>
<tr>
<td>MAG</td>
<td>1.15</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>PHASE</td>
<td>1.20</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>PHASE</td>
<td>1.15</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Ft calculated by linreg (mag(h21[dB]), log (freq)) around a given freq

HSPICE_03: HSPICE 2003, HSPICE 2003-SP1, HSPICE 2005.3
HSPICE_05: HSPICE 2005.3-SP1
- ELDO linked to ICCAP:

  in case of convergence problems at high current
  ICCAP does not continue

  under certain conditions Isub=0

- HSPICE default values:

  v1.15: XRB, XRC, XRE, XRS= 1
  v1.20: XRBI, XRBX, XRCI, XRCX= 0
- VBIC1.20 is available in many simulators but not in ADS
- Simulator benchmarking is time-consuming but necessary
- mostly there is self-consistency of the simulator results
- remaining problems must be solved
Thank you for your attention.