

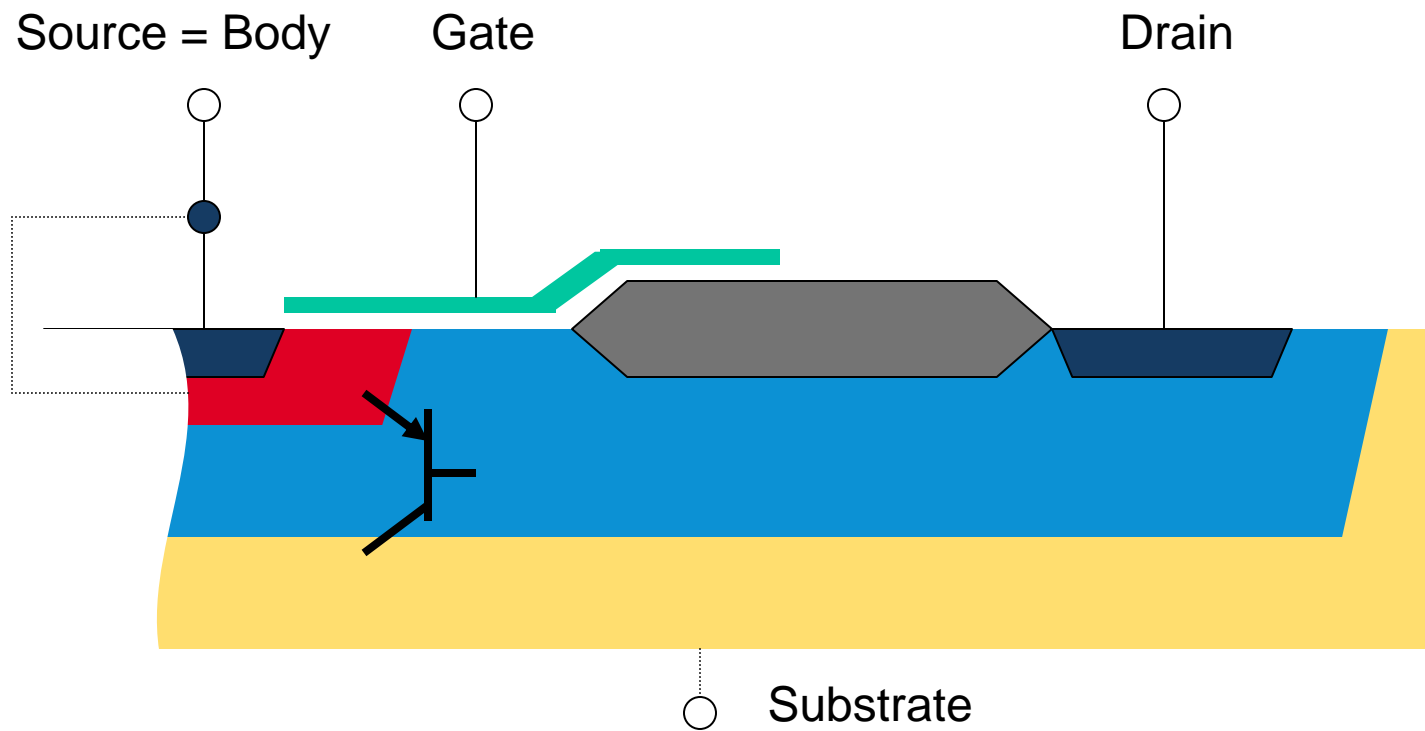
Modeling of Parasitic Bipolars in n-DMOS Transistors

Ch. Maier

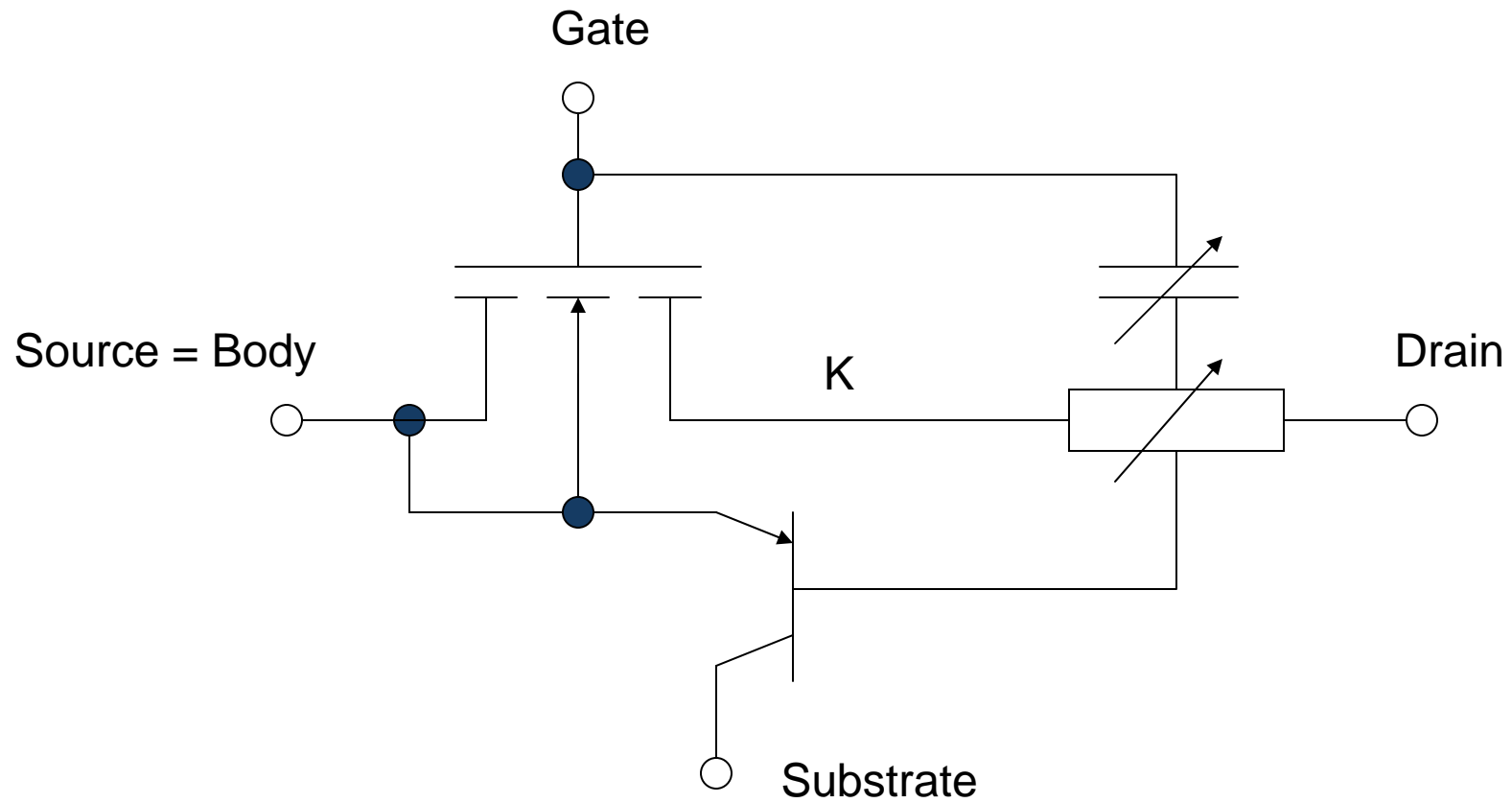
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LDMOS Cross Section



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Parasitic PNP Body - Drain - Substrate

Motivation for Modeling:

- Forward Biasing of Drain-Body Diode
- Current Gain of Parasitic PNP > 1
- Drain-Body and Drain-Substrate Diodes already implemented in DMOS subcircuit model

Model Features:

- Gummel-Poon-Model
- Scalable: eg. $IS = IS0 + JSA * a_{body}$

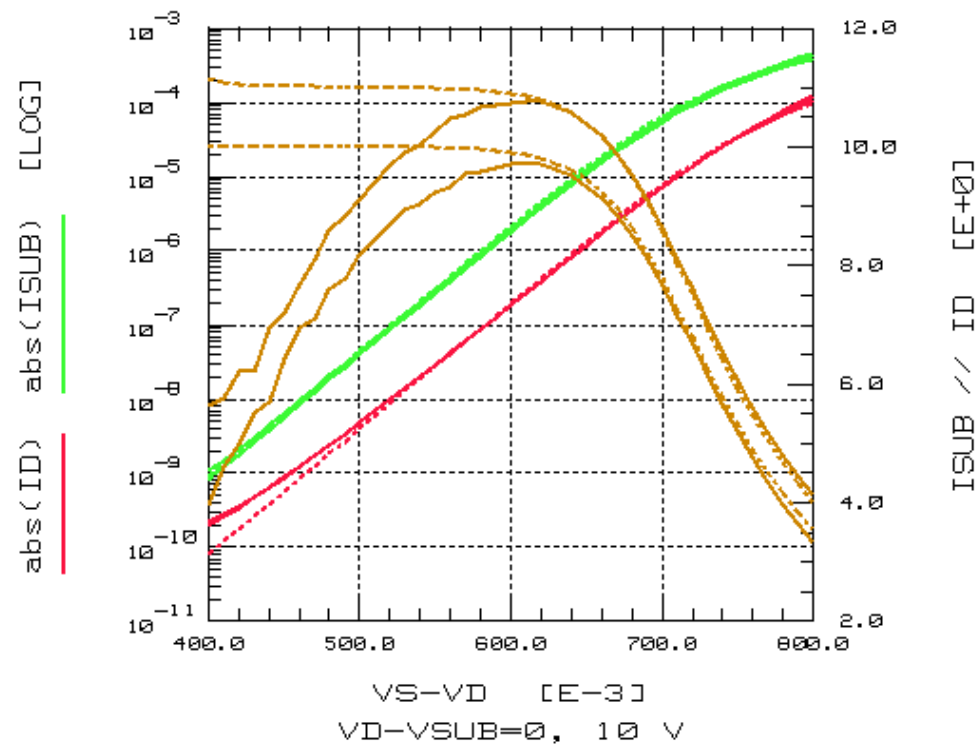
Model Usage

- Standard Model for Circuit Simulation

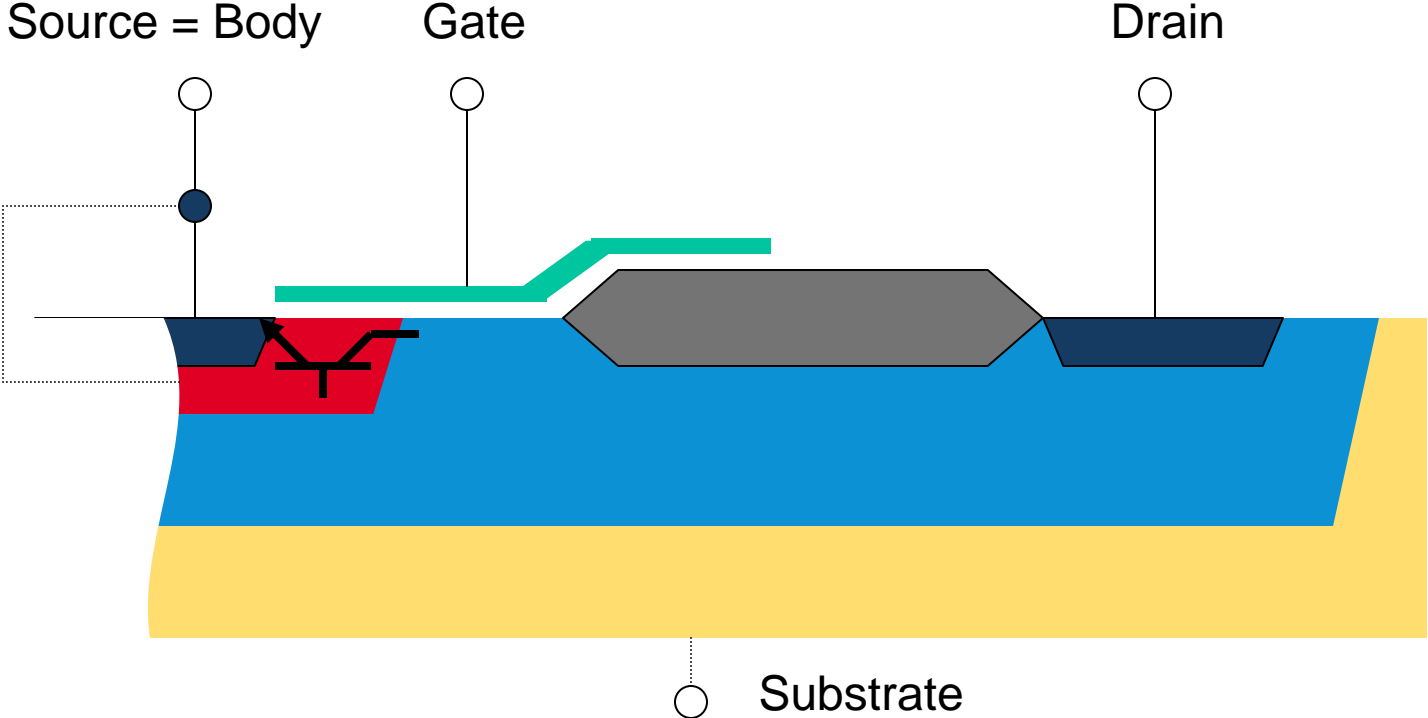


Influence of parasitic pnp Body=Source - Drain - Substrate

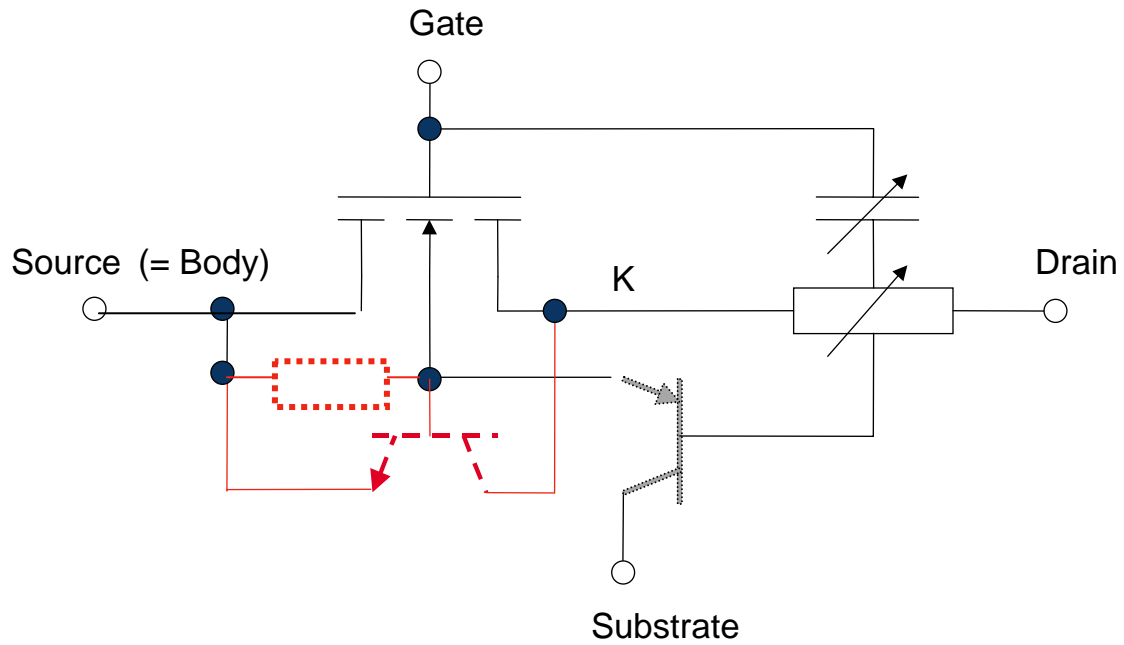
Plot LD40/LD40_40u/Parasit/parPNP (On)



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Parasitic NPN Source - Body - Drain

Motivation for Modeling:

- Simulation of Snapback Effect for VDMOS ESD Investigations

Model Features:

- Extended Ebers-Moll Model
- Current Source for Avalanche Breakdown Modeling

Model Usage

- Only for ESD Simulations



Parasitic NPN Source - Body - Drain of VDMOS Device Measurement vs Simulation

