BVCER simulations with HICUM

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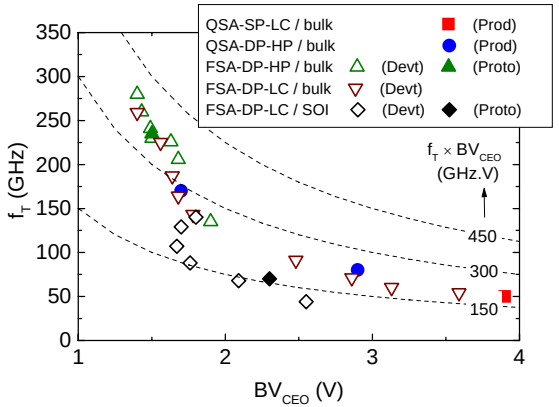
FTM CROLLES / TPS / MODELLING

BVCER SIMULATIONS WITH HICUM

Motivations

With the great increase of RF performances state-of-the-art bipolar transistors suffer from lower Collector to Emitter breakdown capability.



Unfortunately the power supply standard values have not reduced with the same scale, so designing circuit with bipolar transistors used in bias conditions 'beyond B_{VCEO}' is a common designer's wish.

These 'beyond B_{VCEO}' conditions are used in various circuits, PA, VCO, differential pairs...in which bipolar transistors could be biased in static, pulsed or transient mode.

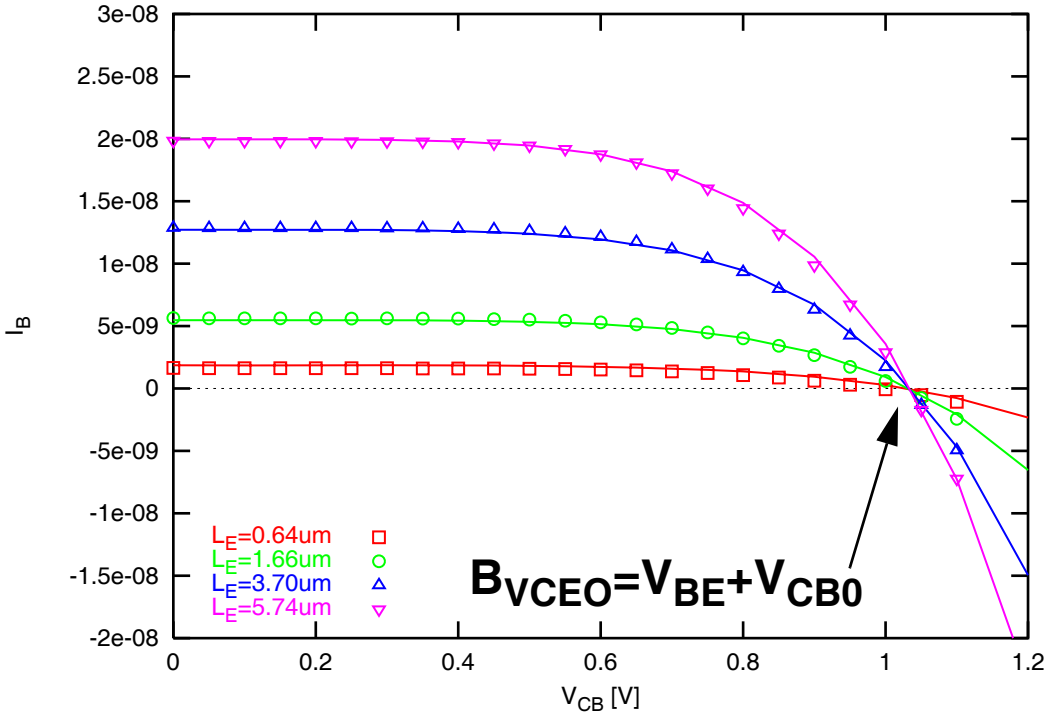
Device modeling engineers should answer to the question: is your model library accurate in these bias conditions?...

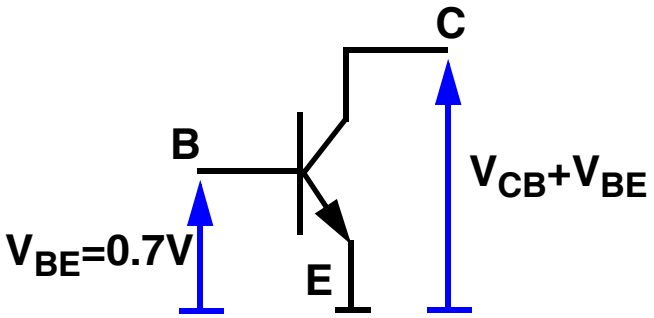
Goal of this presentation

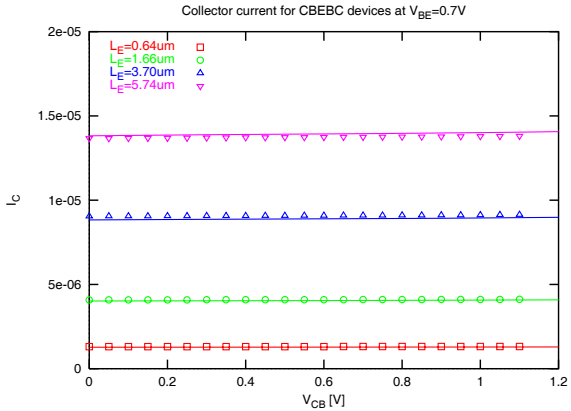
- Open the discussion about which electrical characteristics at the transistor level are the more relevant to check model accuracy for 'beyond B_{VCEO}' conditions in circuits?
- Show comparisons between HICUM model and measurements for B_{VCEO}, B_{VCBO} and B_{VCER} bias conditions.

BVCEO definition:

- B_{VCEO} is measured at a constant low V_{BE} sweeping V_{CB}, when I_B becomes negative. It is supposed to mimic the situation where the base is 'open' which is rather difficult to measure:

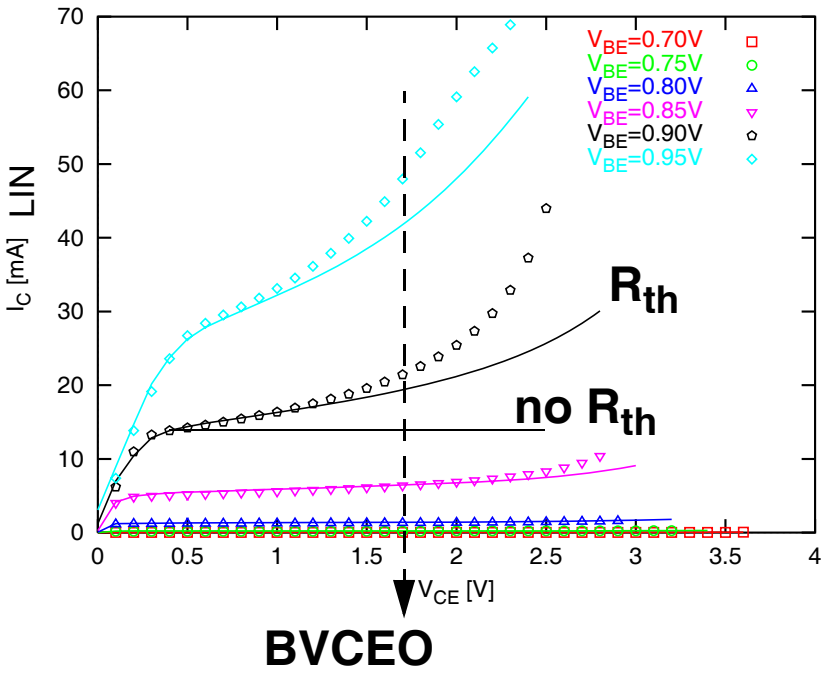


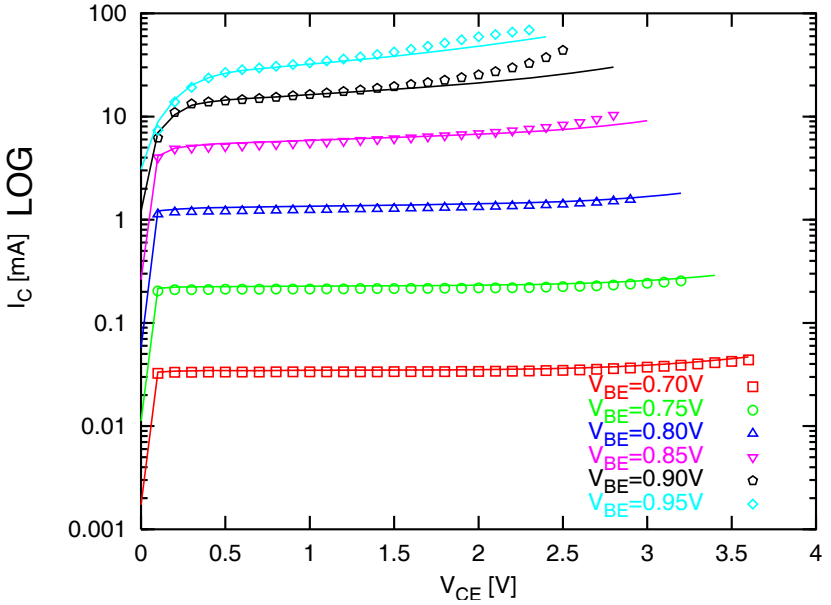




- Obviously very good accuracy with HICUM simulations (points=meas., lines=simu.).
- I_C increases slightly (avalanche current is negligible compared to I_C value).

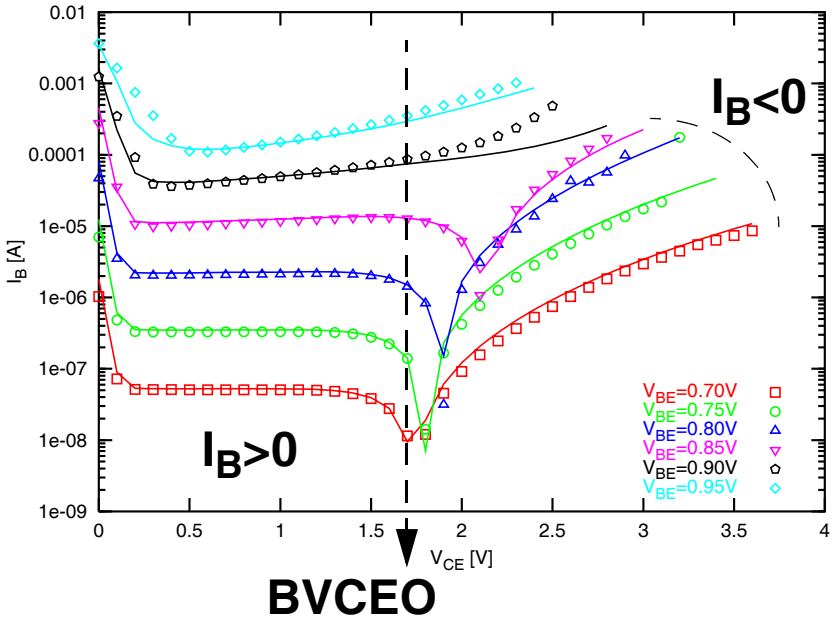
- V_{CE} could actually be increased higher than the B_{VCEO}, depending on the V_{BE} value:





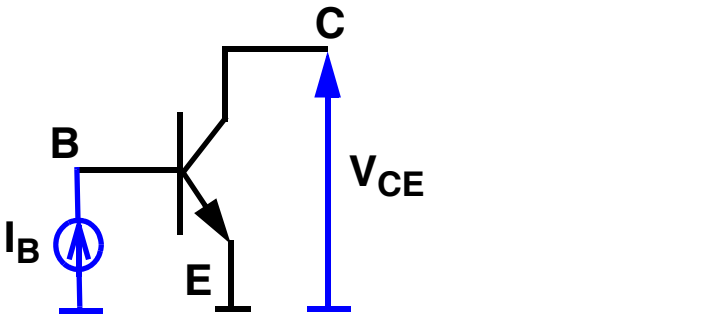
- For high V_{BE} values the collector current increases slightly due to avalanche current and strongly due to self-heating. So the V_{CE} is mainly restricted by thermal breakdown.
- Good accuracy with the HICUM model including a R_{TH} realistic value.

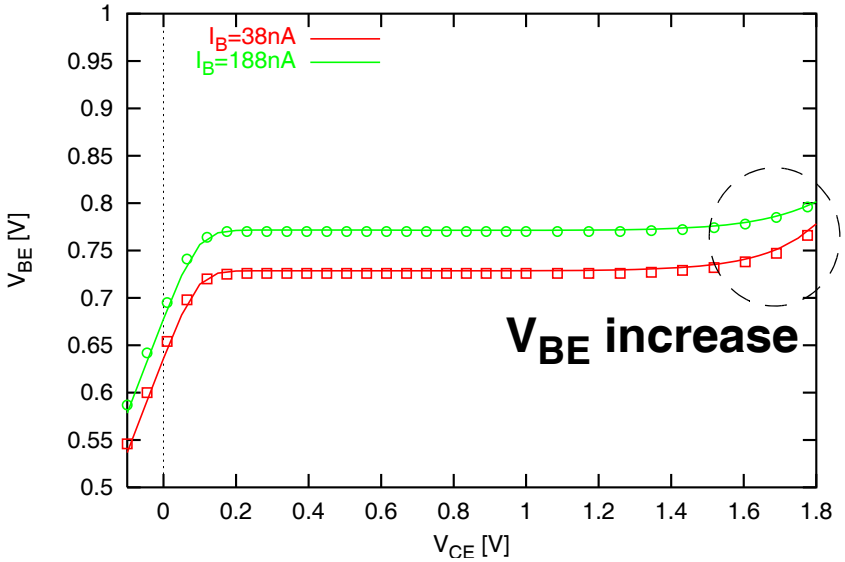
- The accuracy with the HICUM model is good even for base current:

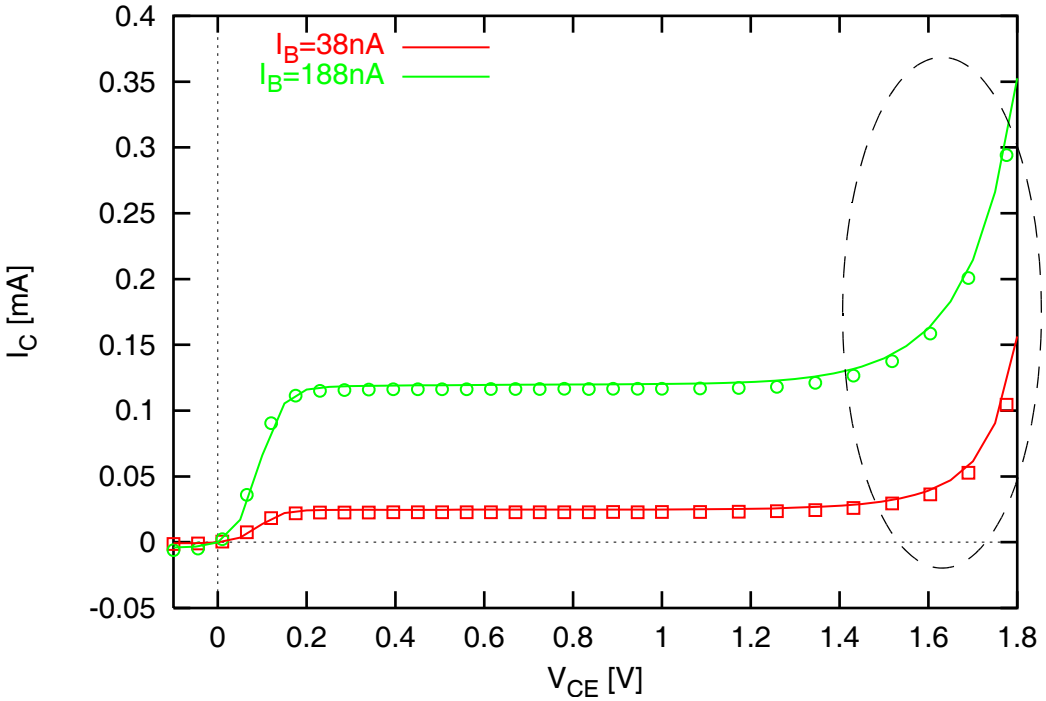


- The negative Base current value is not a blocking point for using the device beyond B_{VCEO} limit as long as it is not destructive.

B_{VCEO} is a limit in case of forced I_B characteristics (Output Char.):



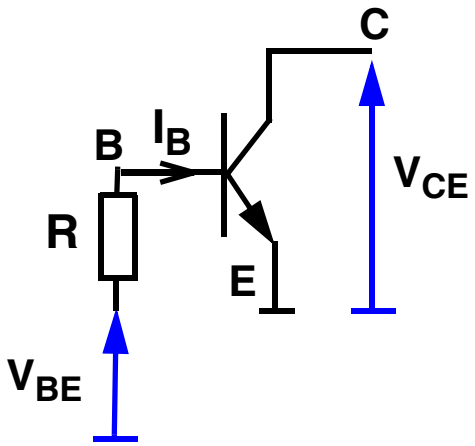


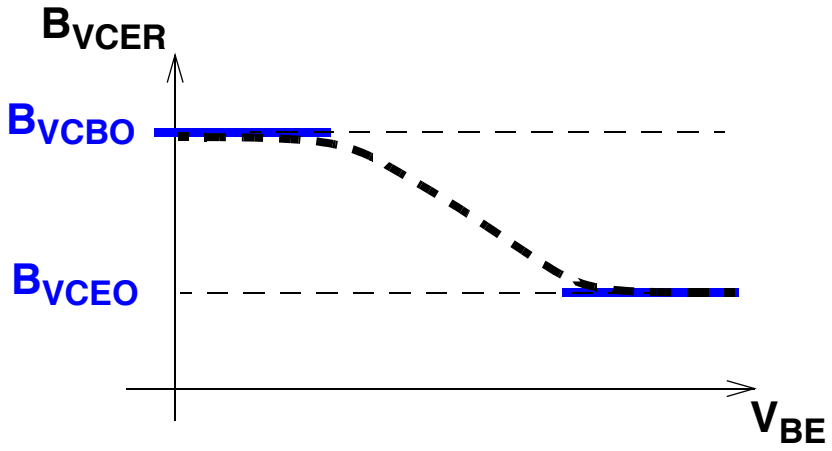


- I_B is forced positive, so the effective V_{BE} increases of few mV to compensate the negative avalanche current when getting close to the B_{VCEO}. I_C increases abruptly (because of the V_{BE} increase), B_{VCEO} limit is reached!
- HICUM model accuracy is good.

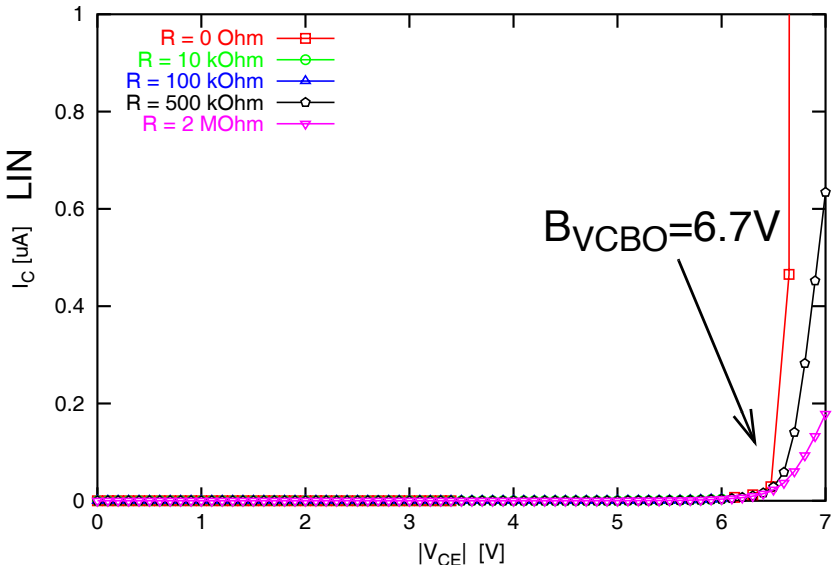
BVCER definition:

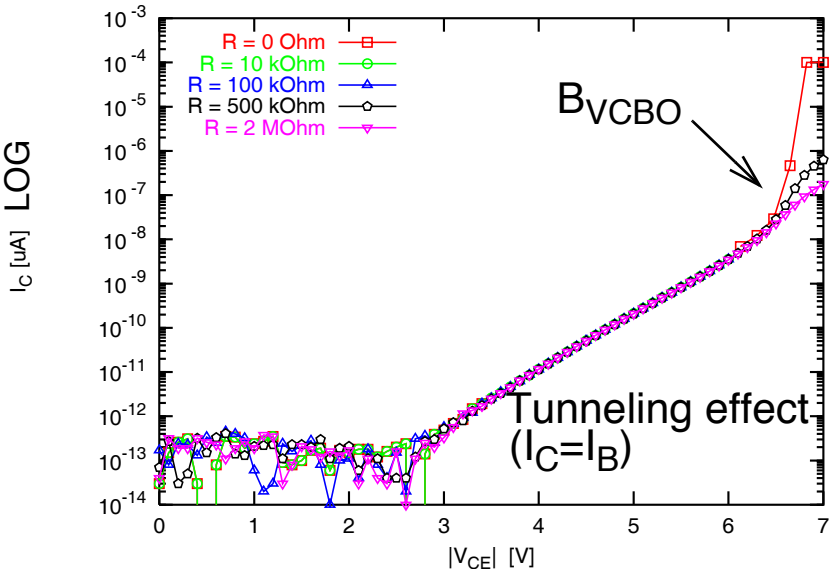
- B_{VCER} is the Collector to Emitter breakdown when the base is biased trough a resistance named R.
- Its value is limited:
  - ➢ at low V_{BE}, by the Base-Collector junction breakdown, B_{VCBO} (if R=0, the base is shorted)
  - ➢ at high V_{BE}, by the B_{VCEO}, because the base could be considered as 'open' if R is increased.

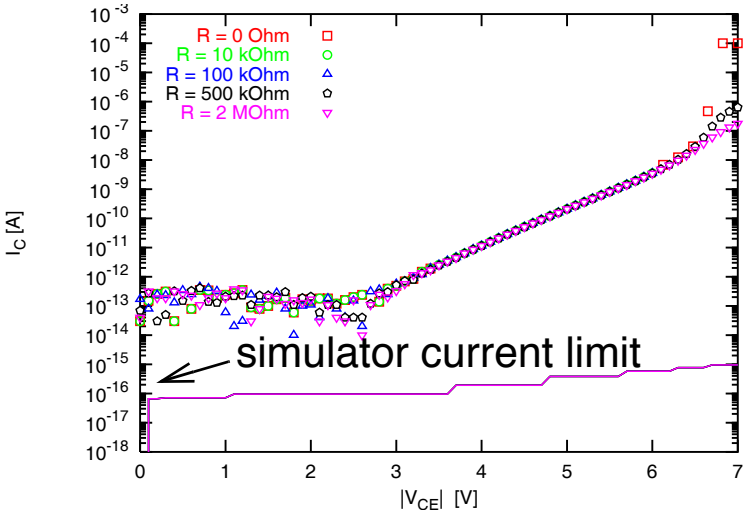




- B_{VCBO} has been measured and simulated on a 0.3µmx10µm CBE device for resistances in the 10kOHM to 2MOhm range:

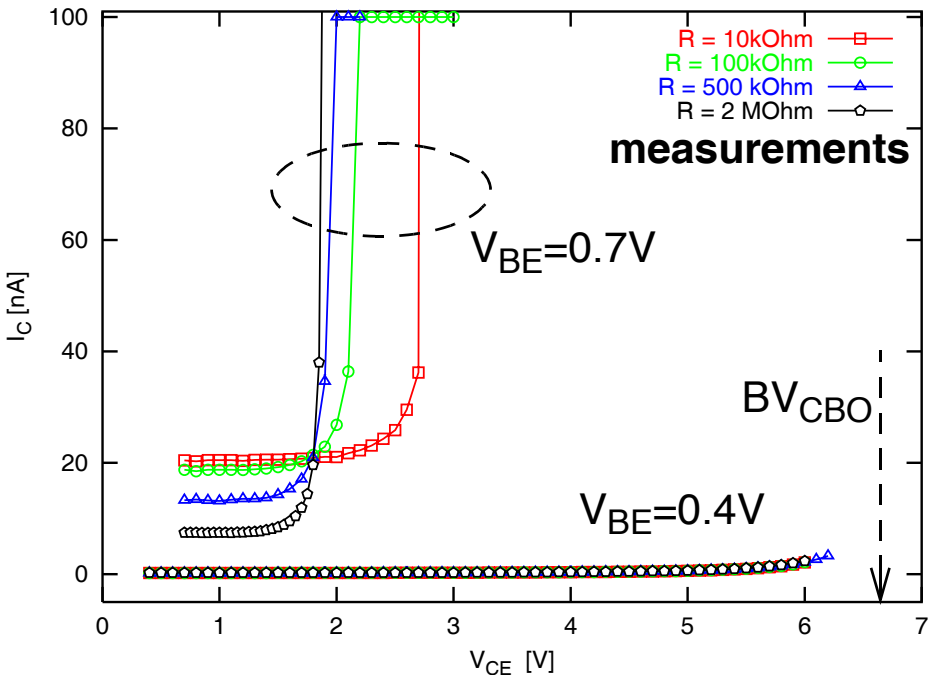


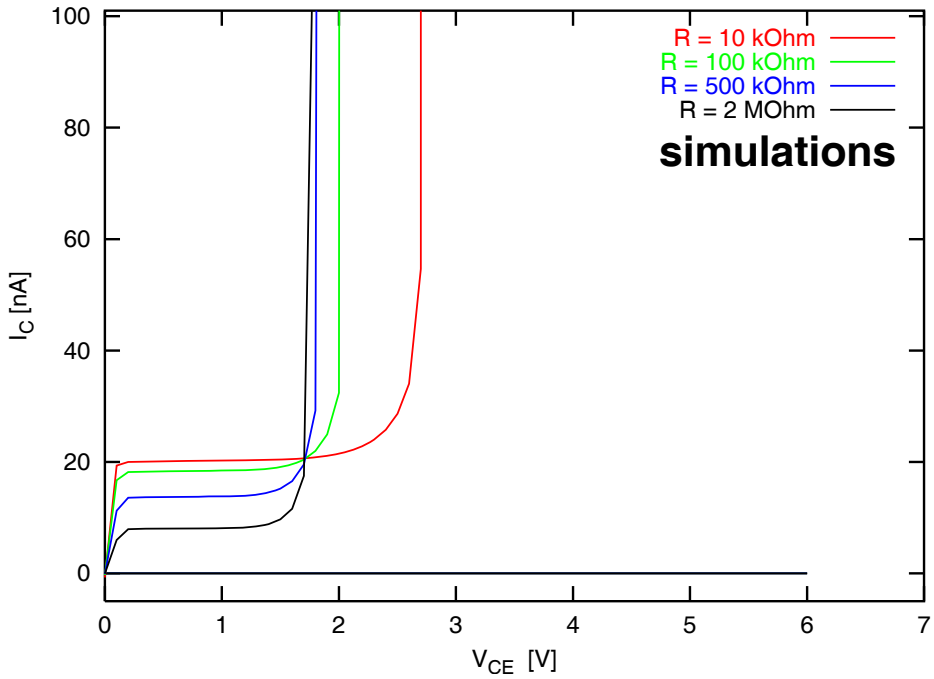




- HICUM fails to capture the B_{VCBO} value because the pure base-collector breakdown is not accounted in the model.
- When this breakdown is triggered on by the BE junction (B_{VCEO} case, multiplication factor M), it works fine.
- The breakdown value is the same whatever R.

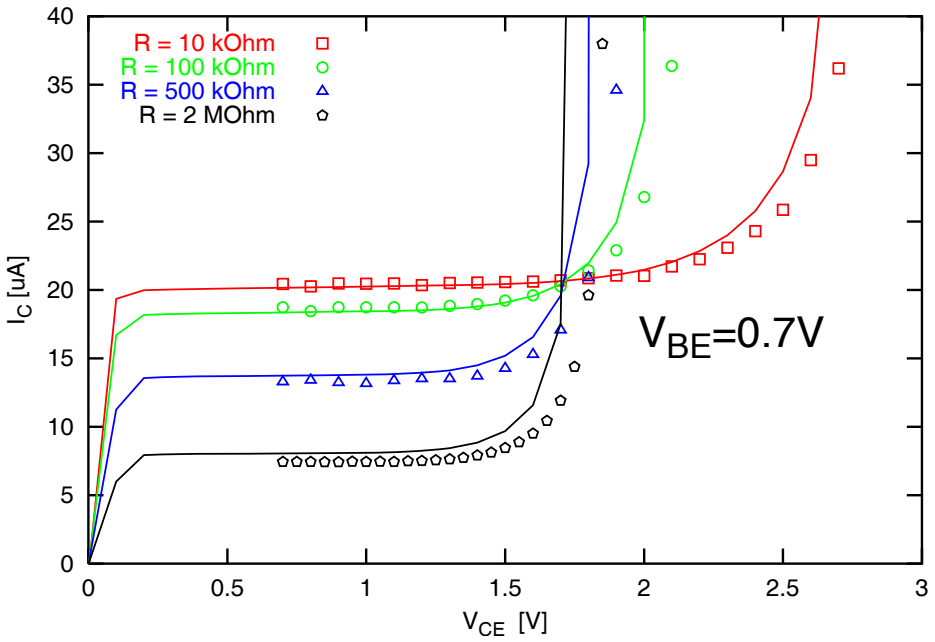
- B_{VCER} has been measured and simulated from V_{BE}=0.2 to 0.7V:

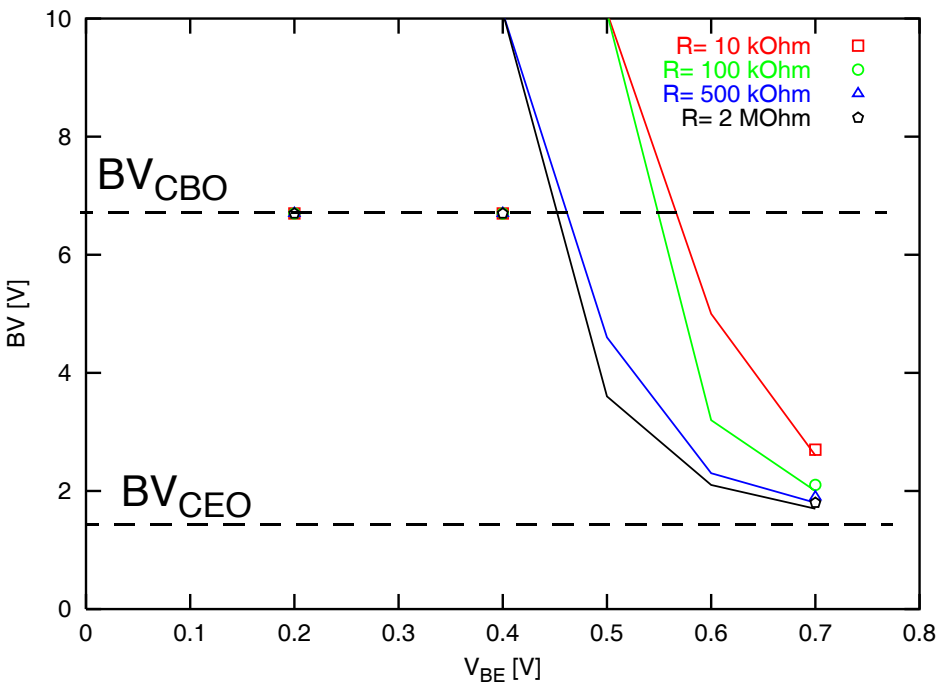




- The HICUM model fails to match the breakdown when it is triggered by the pure base-collector junction (low V_{BE} value).
- But for higher V_{BE} values when the BE junction is ON, the model is accurate.

Summary:





- The model seems accurate for B_{VCER} for high V_{BE} (around 0.7V). More measurements are needed to confirm this point.
- The model doesn't capture low V_{BE} behaviour, when the device breakdowns at the B_{VCBO} value.
- Complementary measurements are needed to confirm that the model behaves correctly when the B_{VCER} reach the B_{VCBO} limit.

Conclusion:

- The HICUM model captures B_{VCEO} and B_{VCER} phenomenon, but miss the B_{VCBO} breakdown (not accounted).
- Should the B_{VCBO} limit be accounted in the HICUM model?
- Is the three figures of merit, B_{VCEO}, B_{VCER}, B_{VCBO} relevant to check 'beyond B_{VCEO}' bias conditions in real circuit design? Is there another electrical characteristic at the transistor level that have to be checked?