Modelling of Parasitic PNP in CMOS Process

B. Senapati

austriamicrosystems AG

Unterpremstaetten, Austria

Bipolar Arbeitskreis, 27 October 2006, Erfurt, Germany

a leap ahead

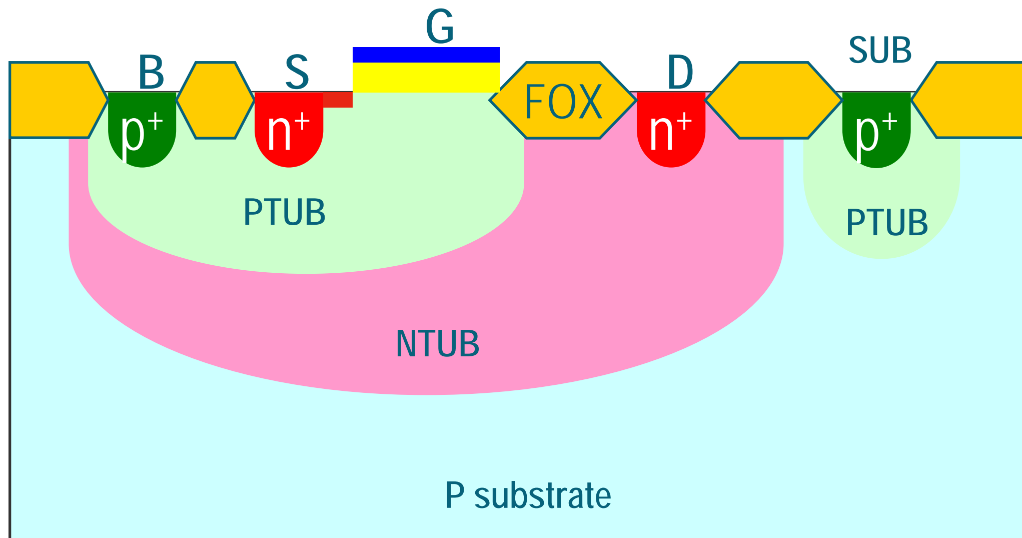
Outline

- Cross-section of parasitic PNP
- Why we need model for parasitic PNP and its scaling
- Different sizes and measurements conditions
- Measurement results and problem
- Scalable model
- Summary

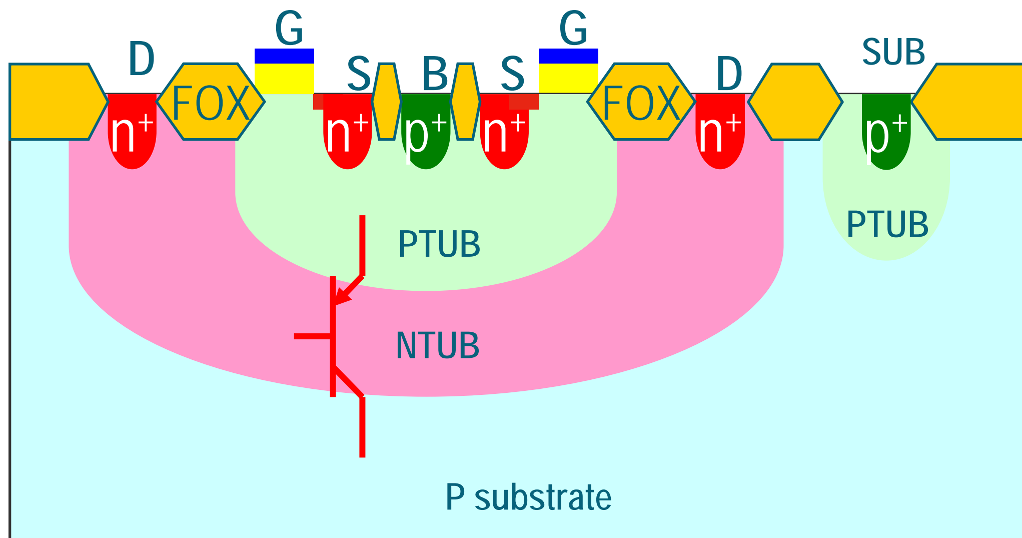
strictly confidential copyright ©2006 austriamicrosystems AG

Cross-Section of NMOSI and PNP

NMOSI



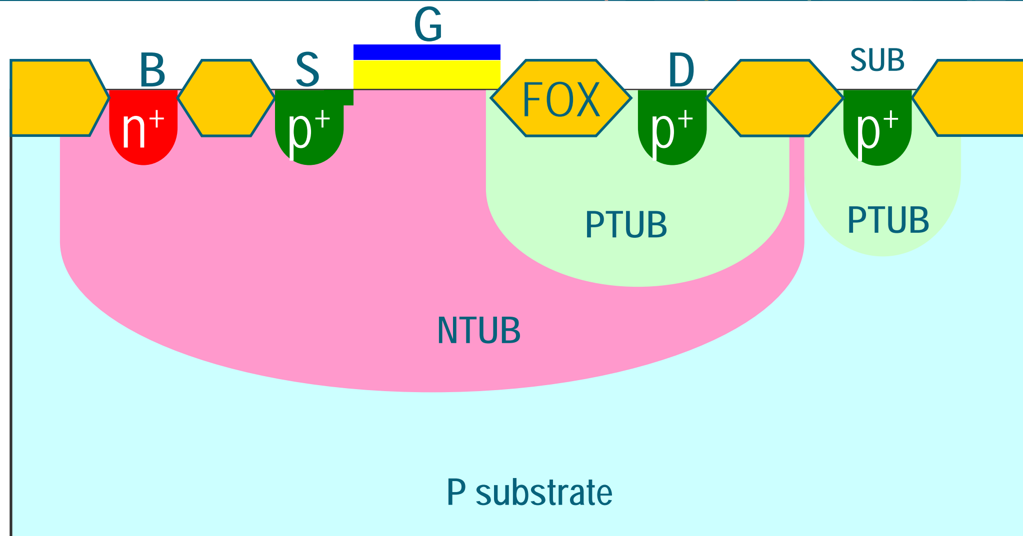
PNP



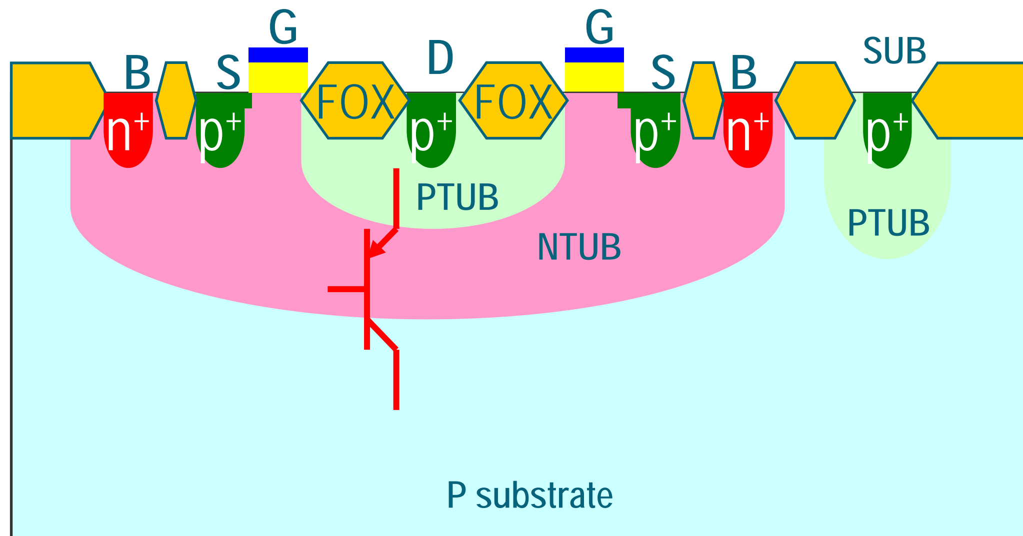
strictly confidential copyright ©2006 austriamicrosystems AG

Cross-Section of PMOS and PNP

PMOS



PNP



strictly confidential copyright ©2006 austriamicrosystems AG

Why We Need Model for Parasitic PNP and Its Scaling

- PNP transistor between body/source (emitter), drain (base) and substrate (collector) of NMOSI
- PNP transistor between drain (emitter), body/source (base) and substrate (collector) of PMOS
- Bipolar effects occur, when parasitic diode is forward biased and results in reasonable substrate current
- Models must be scalable for enabling to select MOS devices of arbitrary length (L) and width (W)
- Standard SPICE Gummel-Poon model is used for the parasitic PNP
- Special equations are introduced to describe the scaling for bipolar current
- MOS transistor substrate current is modeled as collector current of the parasitic bipolar

strictly confidential copyright ©2006 austriamicrosystems AG

Different Sizes and Measurement Condition

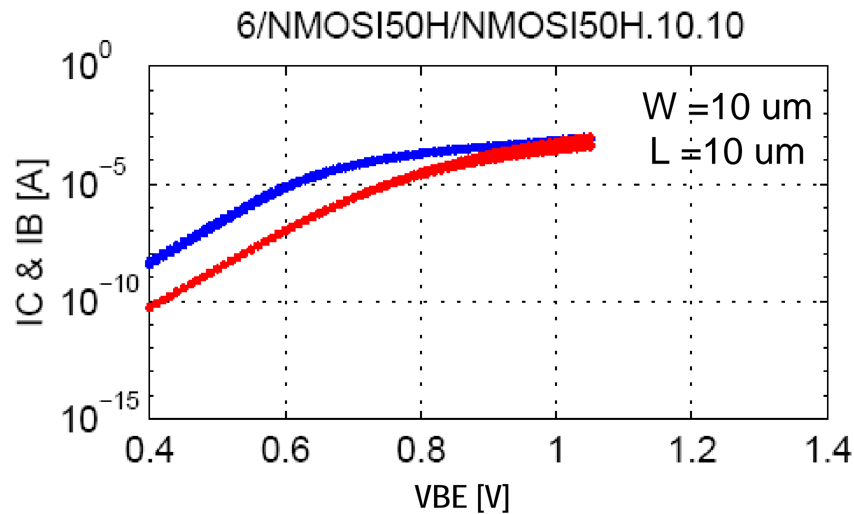
- Different geometries of PNP for NMOSI50T, NMOSI50M, NMOSI50H transistors

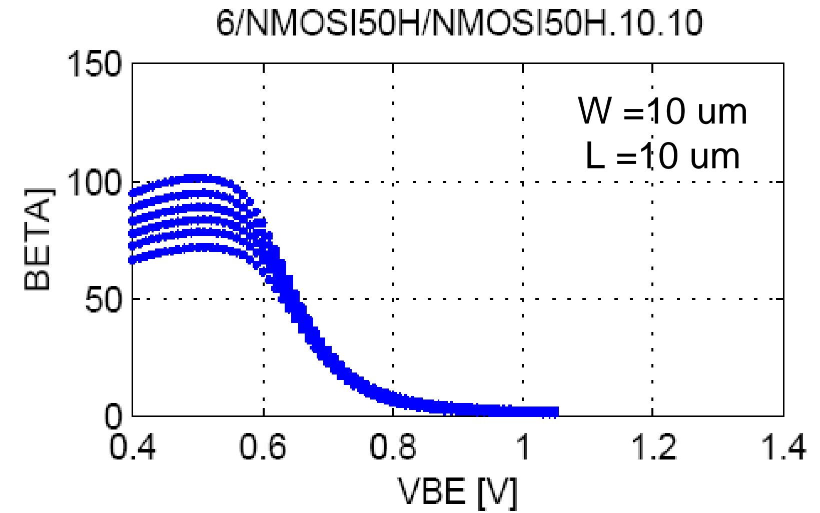
W	10	20	40	40	40	**40**	10	15	40	1000	100
L	0.5	0.5	0.3	0.5	1	**2**	10	10	10	0.5	20
W*L	5	10	12	20	40	80	100	150	400	500	2000

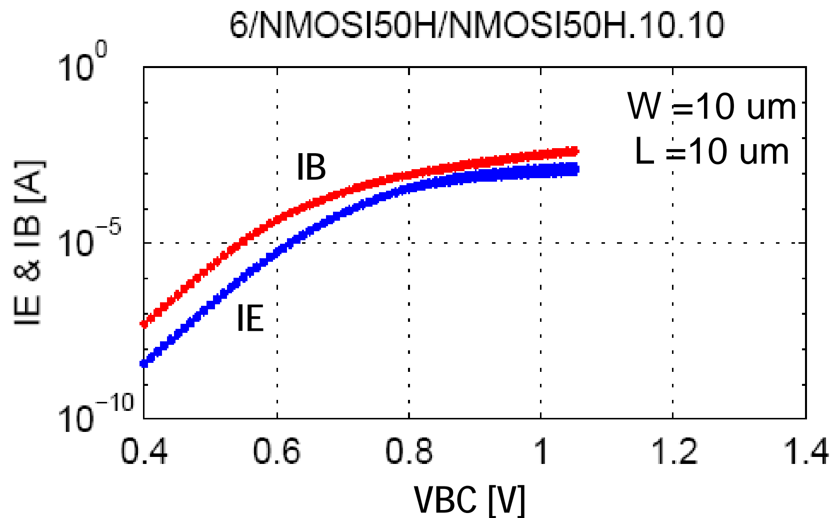
- Similar geometries for PMOS50T, PMOS50H, PMOS50M transistors
- Measurements were made with VB = VS connected together
- Additionally VG = -1 V was applied at the gate terminal for NMOSI and VG = 2 V for PMOS to off the channel
- Biasing was made up to the allowable maximum rating of the device e.g. Vpsub_dntub = 50V for NMOSI50/PMOS50 device group

strictly confidential copyright ©2006 austriamicrosystems AG

Measurement results: NMOSI50M



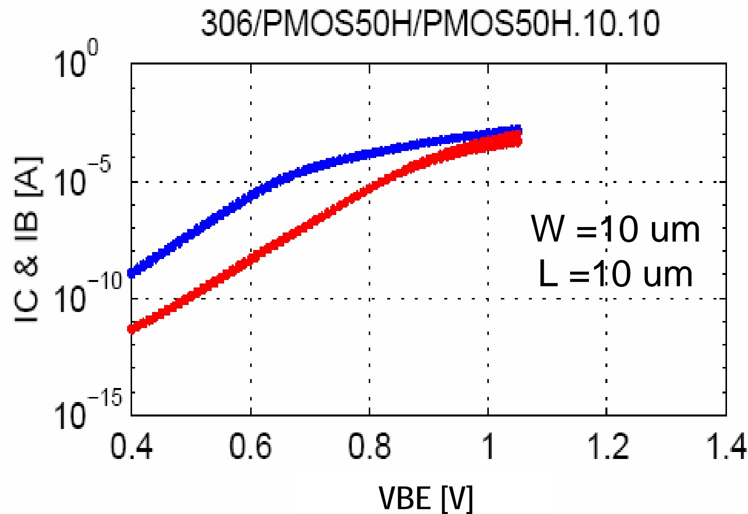


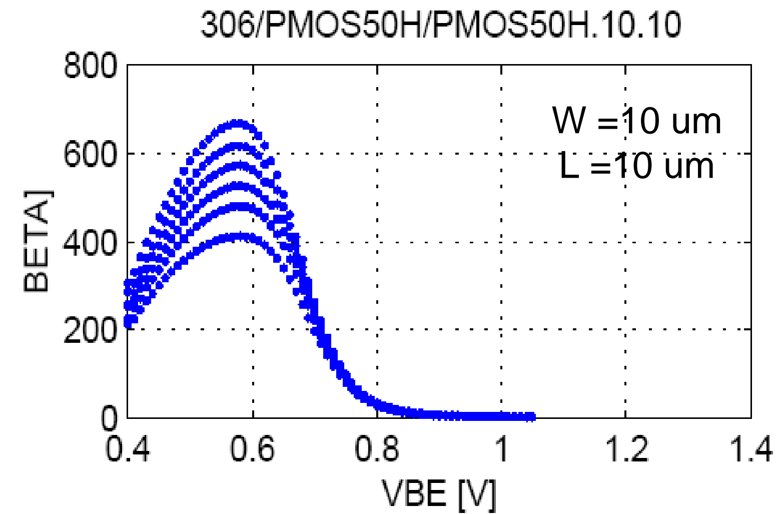


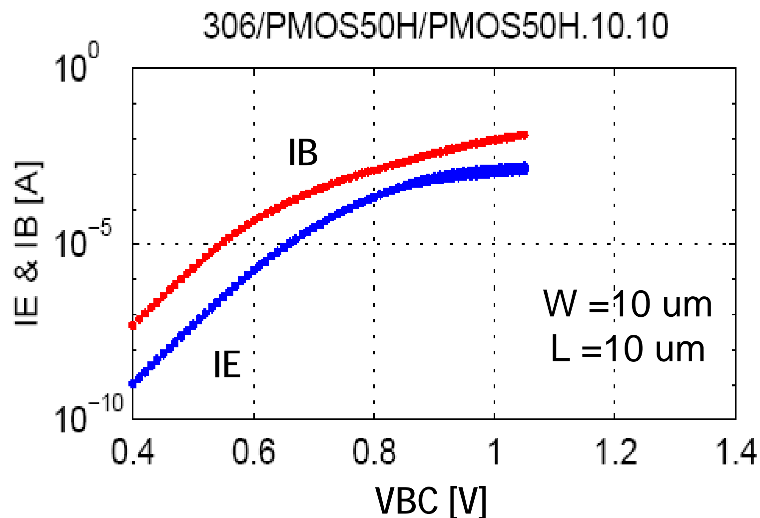
- Good forward Gummel measurement
- Reverse Gummel shows beta <1

strictly confidential copyright ©2006 austriamicrosystems AG

Measurement results: PMOS50H



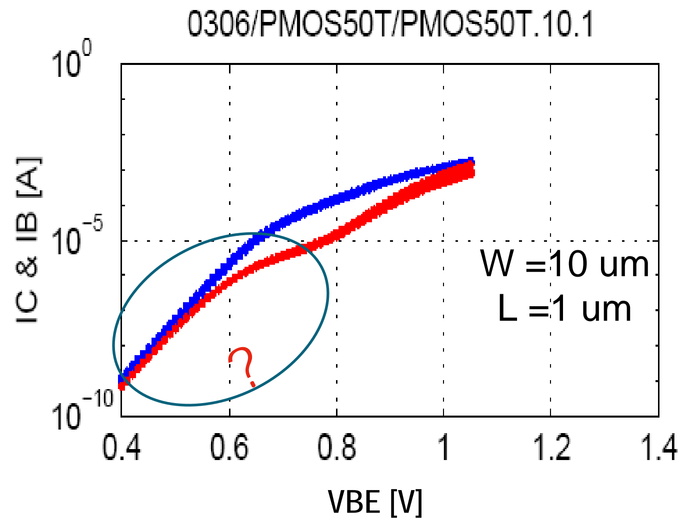


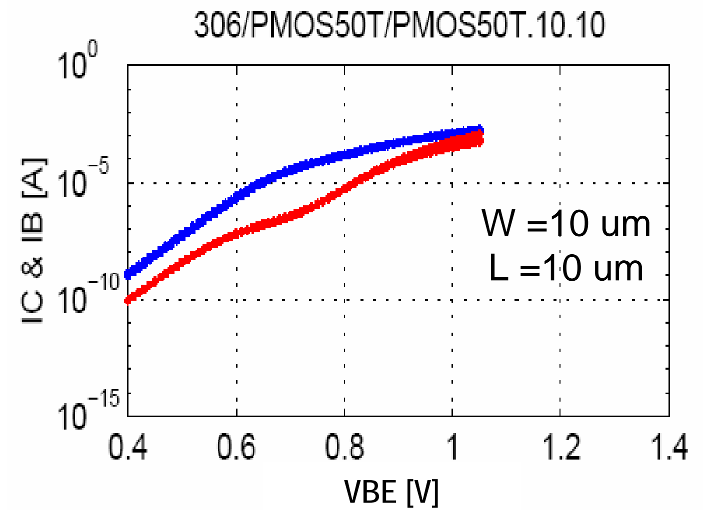


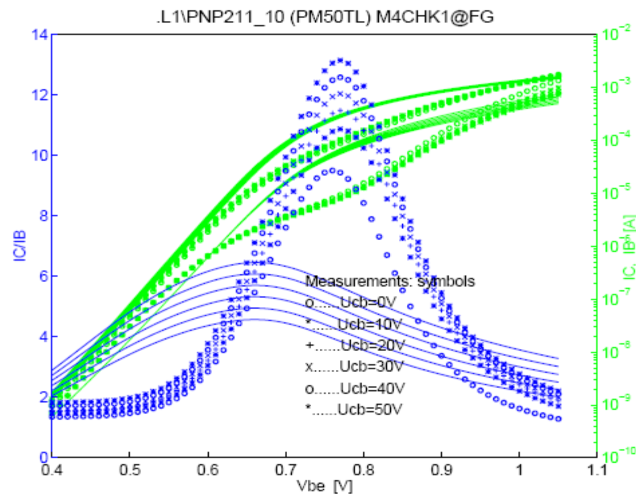
- Good forward Gummel measurement
- Forward current gain > 600 **? ?**
- Reverse Gummel shows beta <1

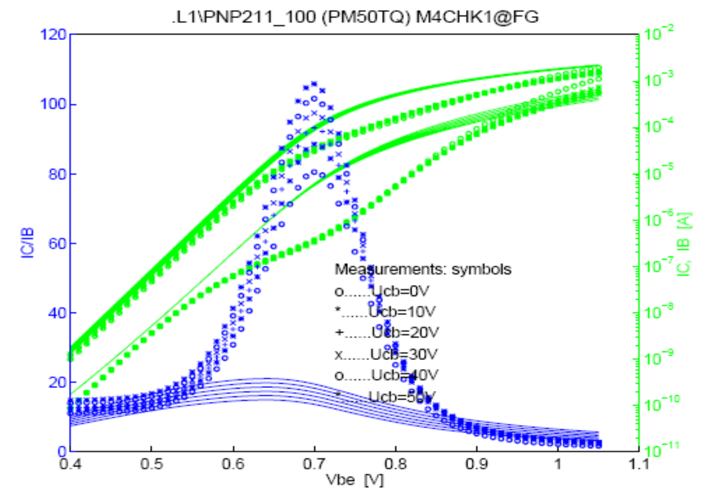
strictly confidential copyright ©2006 austriamicrosystems AG

Measurement results: PMOS50T









strictly confidential copyright ©2006 austriamicrosystems AG

Scalable Model

- Parasitic bipolar scaling is assumed by the device area
- Area parameter of the parasitic bipolar transistor is combination of MOS transistor length (L) and width (W)
- Parameters scaling apply with *area (A) =W*L*
- Scaling has been applied for parameters: IS, IKF, BF, VAF, ISE, RB, RC, CJE, CJC
- Scaling equation is used after fitting of each parameter with equation

$$par = par_ + parL_ \cdot \frac{1}{A}$$

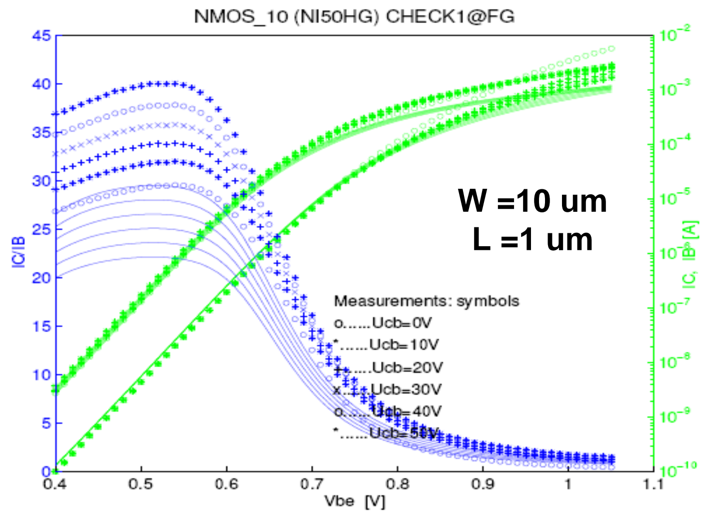
or

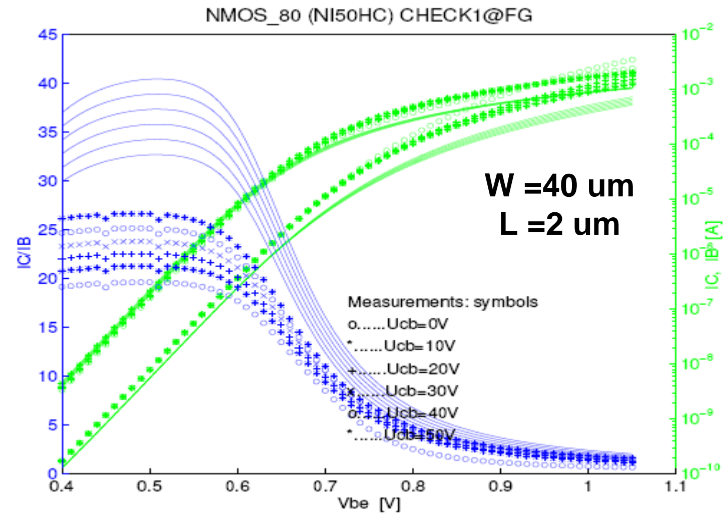
$$par = \exp\left[par_ + \frac{parL_}{A + par0} \right]$$

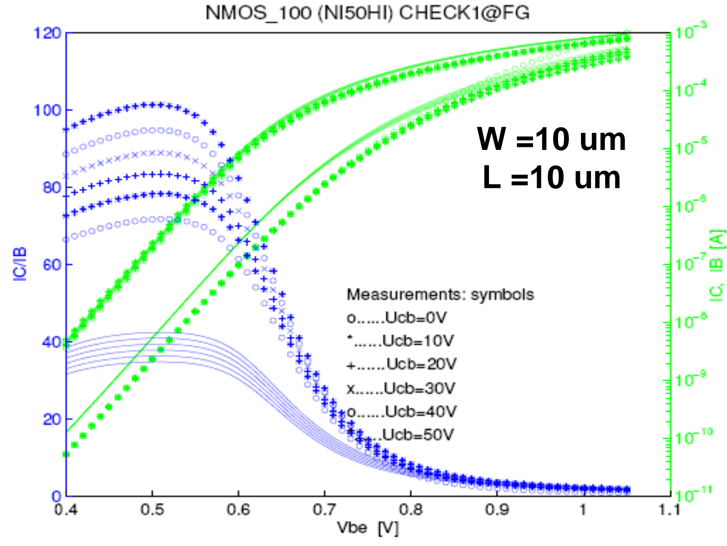
strictly confidential copyright ©2006 austriamicrosystems AG

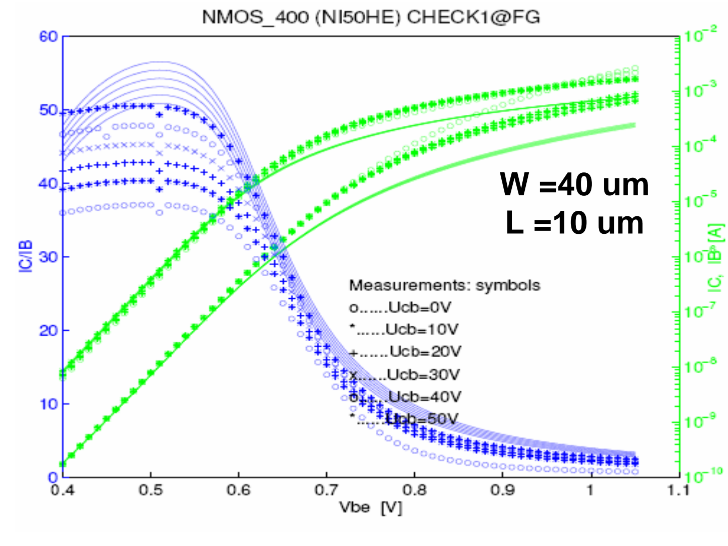
austriamicrosystems

Scalable Model: NMOSI50M



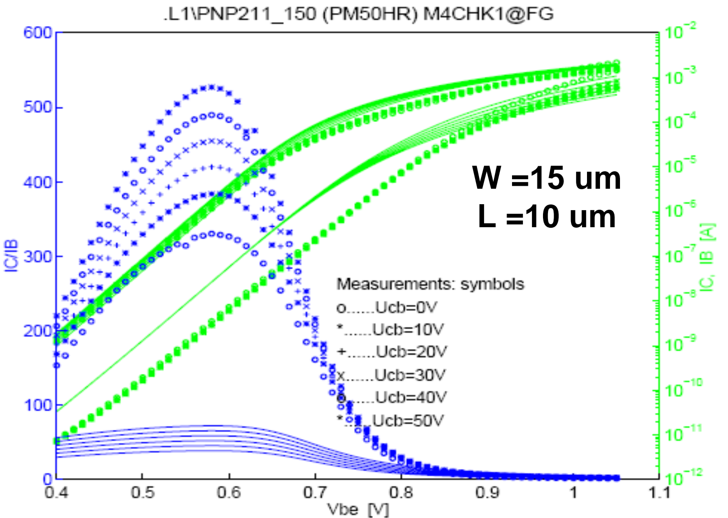


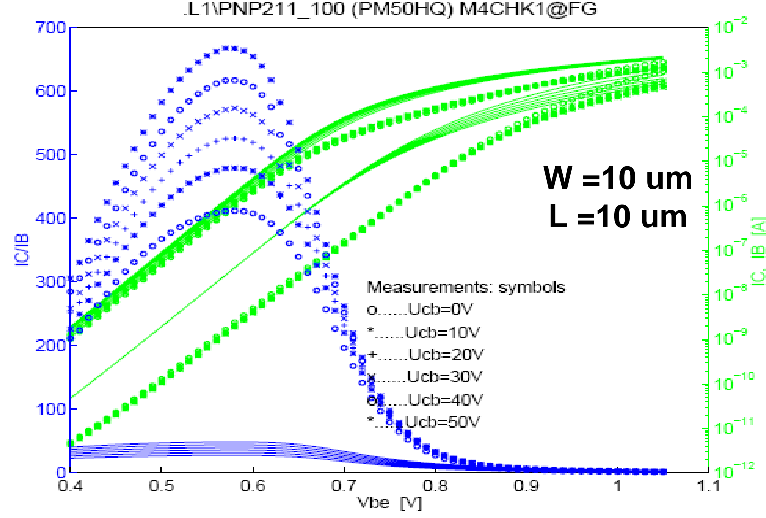


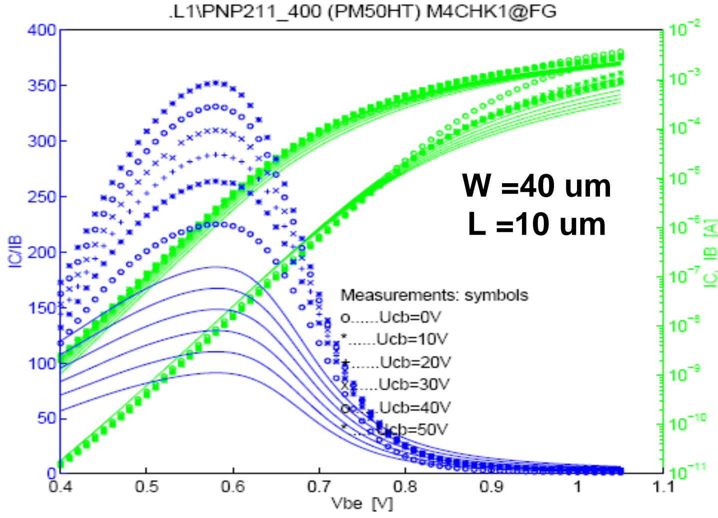


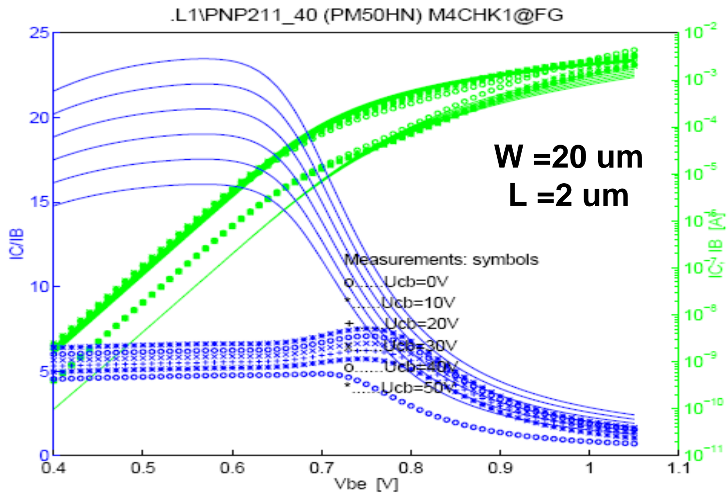
strictly confidential copyright ©2006 austriamicrosystems AG

Scalable Model: PMOS50M









strictly confidential copyright ©2006 austriamicrosystems AG

Summary

- Parasitic PNP is good behaved in forward mode measurement
- Reverse Gummel measurement shows current gain <1
- PNP in PMOS transistor has very high current gain > 600
- Difficult to model forward Gummel of PNP (PMOS50T) device
- Scalable model is not sufficient for all geometries

strictly confidential copyright ©2006 austriamicrosystems AG