Modelling of Parasitic PNP in CMOS Process

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Outline

- Cross-section of parasitic PNP
- Why we need model for parasitic PNP and its scaling
- Different sizes and measurements conditions
- Measurement results and problem
- Scalable model
- Summary
Cross-Section of NMOSI and PNP

NMOSI

PNP
Cross-Section of PMOS and PNP

PMOS

PNP
Why We Need Model for Parasitic PNP and Its Scaling

- PNP transistor between body/source (emitter), drain (base) and substrate (collector) of NMOSI
- PNP transistor between drain (emitter), body/source (base) and substrate (collector) of PMOS
- Bipolar effects occur, when parasitic diode is forward biased and results in reasonable substrate current
- Models must be scalable for enabling to select MOS devices of arbitrary length (L) and width (W)
- Standard SPICE Gummel-Poon model is used for the parasitic PNP
- Special equations are introduced to describe the scaling for bipolar current
- MOS transistor substrate current is modeled as collector current of the parasitic bipolar
Different Sizes and Measurement Condition

- Different geometries of PNP for NMOSI50T, NMOSI50M, NMOSI50H transistors

<table>
<thead>
<tr>
<th>W</th>
<th>10</th>
<th>20</th>
<th>40</th>
<th>40</th>
<th>40</th>
<th>40</th>
<th>10</th>
<th>15</th>
<th>40</th>
<th>1000</th>
<th>100</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>0.5</td>
<td>0.5</td>
<td>0.3</td>
<td>0.5</td>
<td>1</td>
<td>2</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>0.5</td>
<td>20</td>
</tr>
<tr>
<td>W*L</td>
<td>5</td>
<td>10</td>
<td>12</td>
<td>20</td>
<td>40</td>
<td>80</td>
<td>100</td>
<td>150</td>
<td>400</td>
<td>500</td>
<td>2000</td>
</tr>
</tbody>
</table>

- Similar geometries for PMOS50T, PMOS50H, PMOS50M transistors

- Measurements were made with VB = VS connected together

- Additionally VG = -1 V was applied at the gate terminal for NMOSI and VG = 2 V for PMOS to off the channel

- Biasing was made up to the allowable maximum rating of the device e.g. Vpsub_dntub = 50V for NMOSI50/PMOS50 device group
Measurement results: NMOSI50M

- **Good forward Gummel measurement**
- **Reverse Gummel shows beta <1**
Measurement results: PMOS50H

- Good forward Gummel measurement
- Forward current gain > 600
- Reverse Gummel shows beta < 1
Measurement results: PMOS50T

0306/PMOS50T/PMOS50T.10.1

W = 10 um
L = 1 um

306/PMOS50T/PMOS50T.10.10

W = 10 um
L = 10 um

L1:FNP211_10 (PM50TL) M4CHK1@FG

L1:FNP211_100 (PM50TQ) M4CHK1@FG

IC & IB [A]

VBE [V]
Scalable Model

- Parasitic bipolar scaling is assumed by the device area.
- Area parameter of the parasitic bipolar transistor is combination of MOS transistor length (L) and width (W).
- Parameters scaling apply with area \( A = W \times L \).
- Scaling has been applied for parameters: \( IS, IKF, BF, VAF, ISE, RB, RC, CJE, CJC \).
- Scaling equation is used after fitting of each parameter with equation:

\[
par = \text{par}_0 + \text{par}_L \cdot \frac{1}{A} \quad \text{or} \quad par = \exp \left[ \text{par}_0 + \frac{\text{par}_L}{A + \text{par}_0} \right]
\]
Scalable Model: NMOSI50M

NMOS_10 (NI50HG) CHECK1@FG

W = 10 um
L = 1 um

NMOS_40 (NI50HC) CHECK1@FG

W = 40 um
L = 2 um

NMOS_100 (NI50HI) CHECK1@FG

W = 10 um
L = 10 um

NMOS_400 (NI50HE) CHECK1@FG

W = 40 um
L = 10 um
Scalable Model: PMOS50M

- W = 15 um, L = 10 um
- W = 10 um, L = 10 um
- W = 40 um, L = 10 um
- W = 20 um, L = 2 um
Summary

- Parasitic PNP is good behaved in forward mode measurement
- Reverse Gummel measurement shows current gain <1
- PNP in PMOS transistor has very high current gain > 600
- Difficult to model forward Gummel of PNP (PMOS50T) device
- Scalable model is not sufficient for all geometries