Simulation of IB Degradation after Stress

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Outline

• Reliability Stress Tests on HBT

• Degradation Mechanisms

• Modeling of Base Current Degradation

• Influences on
  – HBT RF Behavior ?
  – Circuit Behavior ?
Reliability Stress Tests

- During technology qualification ➔ MTTF
- But how to define failure?
- Typical: 10% base current degradation after application of stress bias
- But: 10% @ which $V_{BE}$? Which stress conditions?
- Typical stress test types
  - reverse emitter-base stress ($V_{EB}$, low temperature)
  - high current stress ($V_{CB} = 0V$, forced high $I_E$, high temperature)
  - mixed-mode stress ($V_{CB} >> BV_{CEO}$, forced medium/high $I_E$, medium/low temperature)
Degradation Mechanisms – High Current Stress

• Stress conditions
  \[ V_{CB} = 0V, \text{forced } I_E \sim \text{up to } 4x I_C \text{ @ max. } f_T, T >> 100^\circ \text{C} \]

• Main observations
  – increase of \( I_B \) for low \( V_{BE} (<0.6 \text{ V}) \),
  – decrease of \( I_B \) in mid-\( V_{BE} (0.6 \ldots 0.8 \text{V}) \) range,
  – emitter resistance decrease for high-\( V_{BE} (> 0.8 \text{V}) \)

• Explanations
  – electromigration effects
  – hot carriers created by Auger recombination
  – recombination enhanced impurity diffusion (REID)
High-Current Stress Test Results

- **Stress Conditions**
  \[ T = 125^\circ C, J_E \sim -37 \text{ mA/}\mu\text{m}^2, V_{CB} = 0V \]
- **Stress time:** 67h
- **Results**
  - \( I_B \) increase
  - no change of \( I_C \) observed
  - \( \beta \) degradation
    - \( V_{BE} = 0.7V \): 9%
    - \( V_{BE} = 0.8V \): 5%
    - \( V_{BE} = 0.9V \): 4%

![Graph showing Base Current, Collector Current vs. V_{BE}](image)
Degradation Mechanisms – Mixed-mode Stress

- **Stress Conditions**
  
  \[ V_{CB} >> BV_{CEO}, \text{ medium/high } I_E \]

- **Observations**
  
  Increase of \( I_B \), esp. for low \( V_{BE} \)

- **Explanations**
  
  - Electron/hole pairs created in CB space charge region by impact ionization
  - Hot carriers get sufficient energy to traverse base region
  - Trapped holes in BE oxide spacer
  - Recombination with electrons
  - Enhanced BE recombination current

  (Vanhoucke et al., BCTM 2006)
Mixed-Mode Stress Test Results

- **Stress Conditions**
  \( J_E \sim -5 \text{ mA/}\mu\text{m}^2, V_{CB} = 3V \)
- **Stress time:** up to 97h
- **Results**
  - \( I_B \) increase
  - no change of \( I_C \) observed
  - degradation more expressed @ low temperatures
Modeling of Base Current Degradation I

- **HBT type**
  - npn200: $f_T/f_{max} \sim 190/190$ GHz, $BV_{CE0} = 1.9$ V, $BV_{CB0} = 4.5$ V
- **Standard stress conditions**
  - Mixed-mode stress bias: $IE = -4$ mA, $V_{CB} = 2.0/2.3/2.7/3.0$ V
  - Stress duration: 120 min
  - Temperature: $T = 27°C$
Modeling of Base Current Degradation II

- Simple variation of model parameter affecting non-ideal base current
  - Change only non-ideal BE saturation current $I_{BEN}$ → simulation sufficient esp. for low $V_{BE}$
  - Change only emission coefficient $N_{EN}$ → simulation not satisfying
  - Change both: $I_{BEN}$ and $N_{EN}$ → simulation sufficient esp. for medium voltages
Modeling of Base Current Degradation III

- Simple variation of model parameter effecting non-ideal base current
  - Change only non-ideal BE saturation current IBEN \( \Rightarrow \) simulation sufficient
  - Fit of IBEN(t) with simple power function

\[
IBEN(t) = IBEN_0 \times (1 + 11.036 \times (t/t_0)^{0.36})
\]

\[
IBEN_0 = 9 \text{A}, \quad t_0 = 1 \text{min}
\]
Modeling of Base Current Degradation IV

• Variation of transistor compact model I
  – introduction of additional time dependent BE diode

\[ I_B = I_{BEI} + I_{BEN} + \Delta I_B \]
\[ I_B = I_{BEI} \cdot \exp\left(\frac{qV_{BE}}{N_{IE} \cdot kT}\right) + I_{BEN} \cdot \exp\left(\frac{qV_{BE}}{N_{EN} \cdot kT}\right) + \Delta I_B \]

– temperature dependence of base current increase after Ruat et al. (BCTM 2006)

\[ \Delta I_B(T,t) = \frac{P}{A} \cdot I_s(T,t) \cdot \left(\frac{t}{t_0}\right)^{a(T)} \cdot \exp\left(\frac{qV_{BE}}{n(T) \cdot kT}\right) \]
\[ a(T) = a_0 \cdot \exp\left(-\frac{E_A}{kT}\right) \]

\( a(T) \) = acceleration factor
P/A ratio for peripheral localization of degradation
Activation energy \( E_A \) depending on stress type (high current, reverse or mixed-mode)
Modeling of Base Current Degradation V

- Variation of transistor compact model II
  - Goal: $\Delta I_B$ as function of stress bias voltage $V_{CB}$, $I_E$, and $T$

$$\Delta I_B(t) = I_S(V_{CB}, I_E, T) \cdot \left(\frac{t}{t_0}\right)^a(V_{CB}, I_E, T) \cdot \exp\left[\frac{V_{BE}}{n(V_{CB}, I_E T)kT}\right]$$

- Implementation into verilog-A
- First step: $V_{CB}$ variation, $I_E$, $T$ constant
- Concentration on optimum fit around $V_{BE} \sim 0.6V$
  Example: optimization of $n(V_{CB})$ @ $t = 60min$
Modeling of Base Current Degradation

- Variation of transistor compact model III

\[ I_E = -4 \text{ mA}, \ T = 300\text{K}, \ V_{CB} = 2.0/2.3/2.7/3.0 \text{ V} \]

Estimation of coefficients by empirical functions

\[
\Delta I_B(t) = I_S'(V_{CB}) \cdot \left( \frac{t}{t_0} \right)^a(V_{CB}) \cdot \exp \left[ \frac{V_{BE}}{n(V_{CB})kT} \right]
\]

\[ I_S' = I_{S0} \exp \left[ \frac{V_{CB} - V_{CB0}}{V_{S0}} \right], \]

\[ a = a_0 + a_{10} \cdot \exp \left[ -\frac{V_{CB}}{a_{11}} \right], \]

\[ n = \sum_{i=0}^{2} n_i \cdot (V_{CB} - V_{CB0})^i \]
Variation of transistor compact model IV
\[ I_E = -4 \text{ mA}, \quad T = 300K, \quad V_{CB} = 2.3/2.7/3.0 \text{ V} \]
Variation of transistor compact model $V$

$I_E = -4 \ mA$, $T = 300K$, $V_{CB} = 2.0/2.3/2.7/3.0 \ V$
Influence on RF Behavior

• Check of RF behavior after 2h and 200h simulation with simple IBEN(t) model @
  \( V_{CB} = 2.7V, I_E = 4mA, T = 27^\circ C \)

• Attention: model does not take into account possible “degradation saturation”
  at long stress times

• After 200h: \( \Delta I_B/I_B = -10\% \) @ \( V_{BE} = 0.9V \)
Influence on RF Behavior II

- No significant degradation @ f > 1 GHz
- No influence on $f_t, f_{max}$
- Up to 40% degradation of $h_{21}$ observable below 1 GHz

![Graph showing current gain $h_{21}$ vs. frequency for different stress times and $V_{BE}$ values.]
Influence on IC Behavior?

- Test IC: differential VCO with oscillation frequency $f_{osc} \sim 77$ GHz
  - 200h stress simulation showed only very small impact on $f_{osc}$ and output power $P_{out}$
  - To be confirmed: phase noise behavior
Summary

• Simulation of mixed-mode stress induced $I_B$ degradation with
  – simple model parameter variation
  – introduction of additional BE diode

• Influence on rf behavior checked
  – only influence @ $f < 1$GHz

• Simulation showed no degradation of test circuit 77GHz-VCO