

Bandgap Reference Simulation

Principles and Problems

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Never stop thinking

Table of contents

■ **Bandgap reference basics**

■ **Bandgap reference error sources**

■ **Summary**

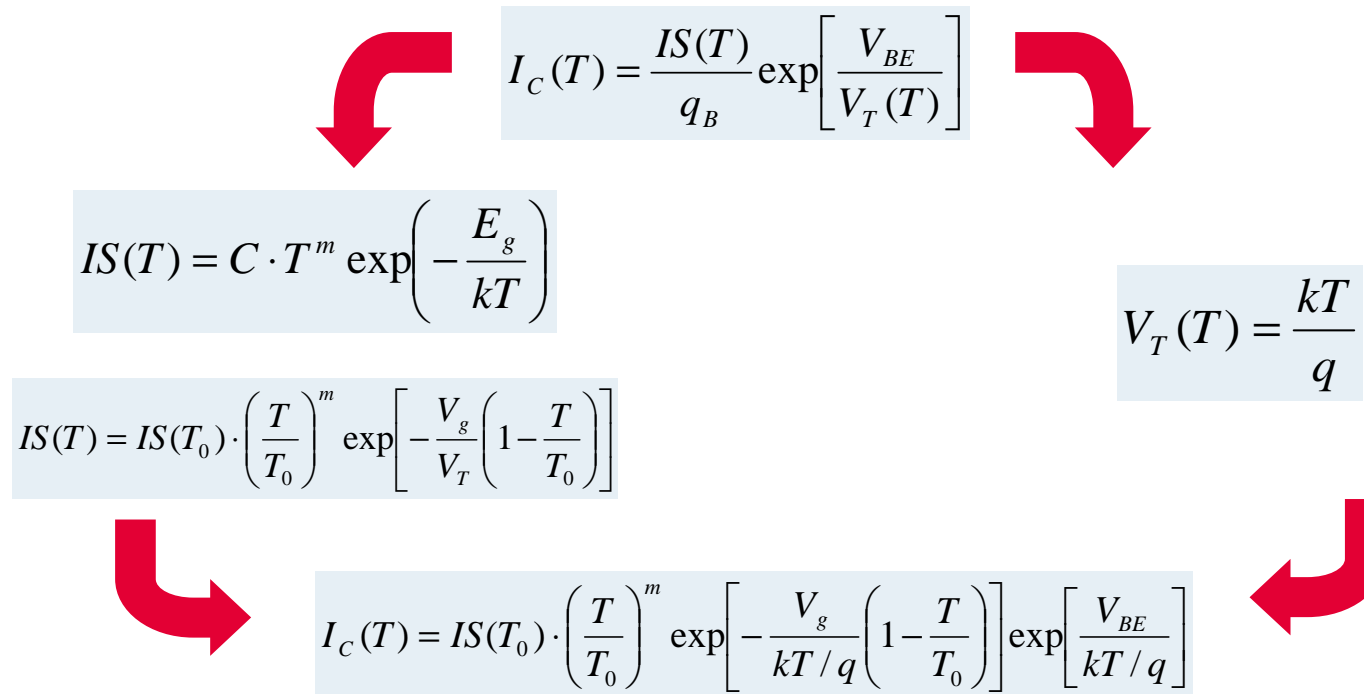
■ **Appendix**

Bandgap reference basics

IC temperature dependence



- IC depends on T vs. $I_S(T)$ and $V_T(T)$
- I_S includes $\mu(T)$ and $n_i^2(T)$
- m (=XTI) represents the mobility temperature dependence
- E_g represents the band gap of the material

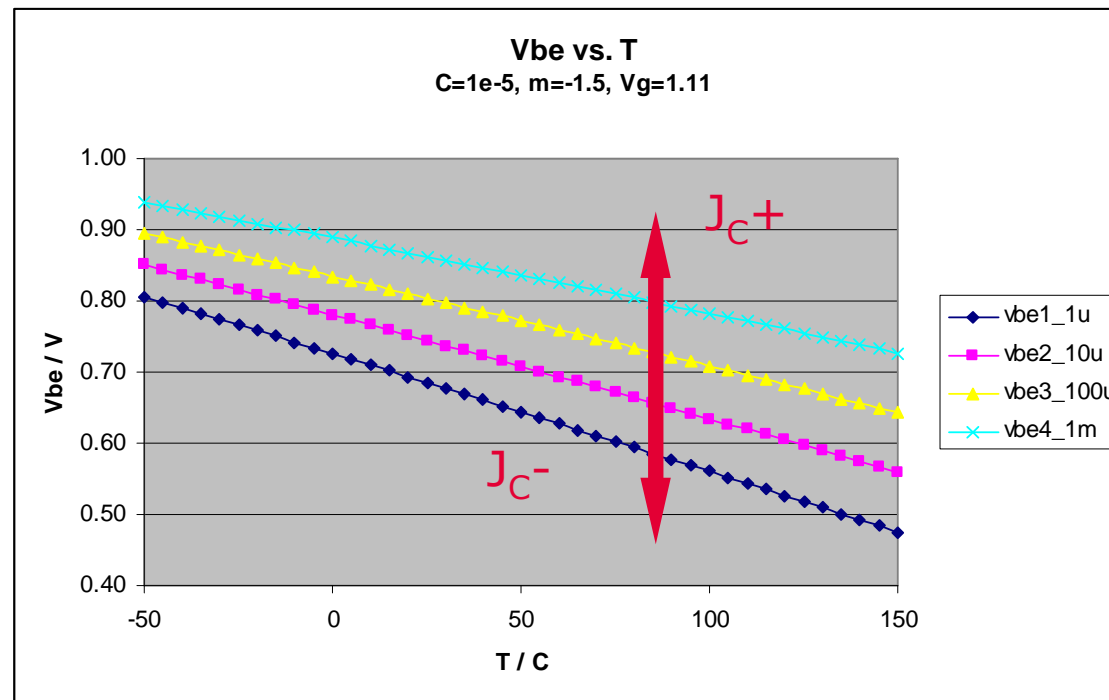


Bandgap reference basics

VBE temperature dependence



- V_{BE} decreases with T (neg. TC)
- Slope of $V_{BE}(T)$ depends complementary on current density J_C
- Note: The slope changes with temperature. This nonlinearity is the reason for the nonlinearity of VBG vs. T
- Important observation: ΔV_{BE} increases vs. T (pos. TC)

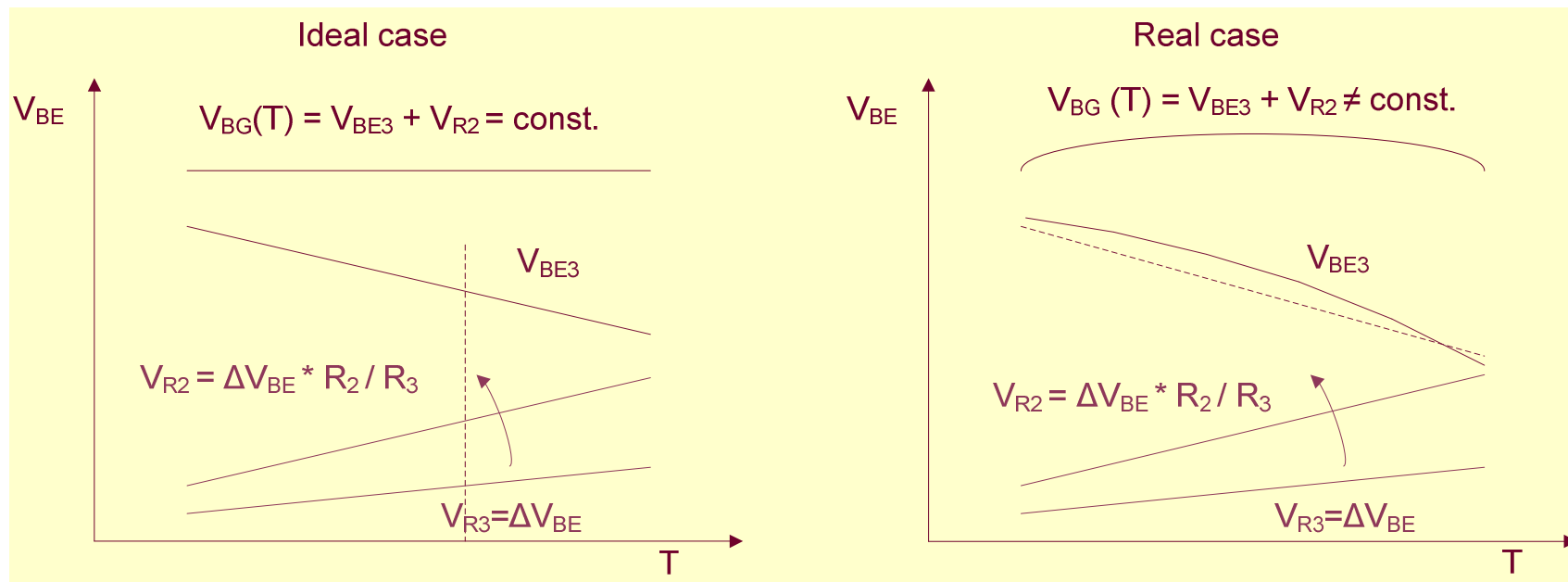


Bandgap reference basics

Widlar diode



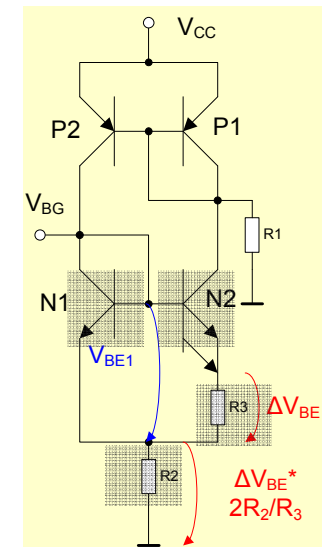
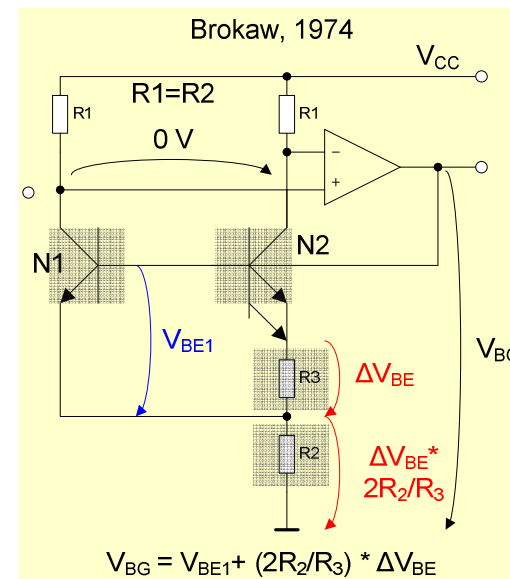
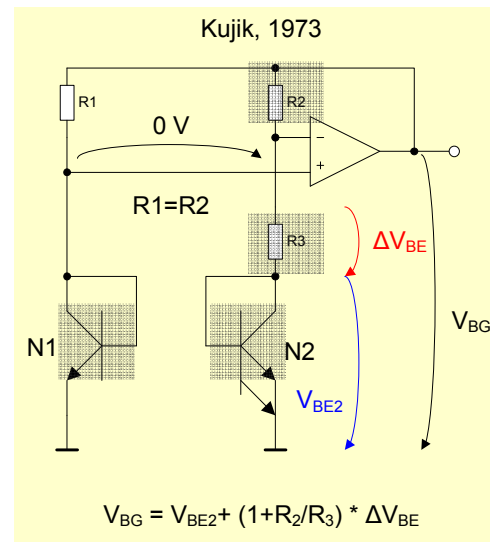
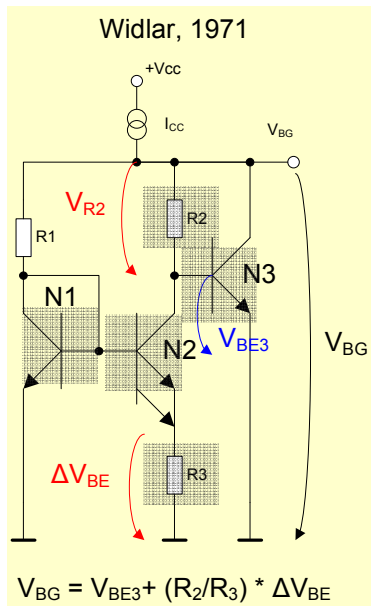
- Basic principle of a Bandgap reference is explained here using the circuit proposed by Widlar in 1971
- Fundamental idea of Widlar: compensate the negative TC of a base emitter voltage V_{BE} by adding a second voltage V_{R2} with positive TC
- Problem: pos. TC (ΔV_{BE}) < neg. TC (V_{BE})
- Solution: Amplification of ΔV_{BE} necessary



Bandgap reference basics

Circuit variations

- Bandgap principle may be realized using different circuit techniques
- 1. Widlar, 1971: N1, N2, N3, R1, R2, R3 used for bandgap core
- 2. Kujik, 1973: N1, N2 are diode connected, bandgap core with only four devices, N1, N2, R2 and R3, which is shifted upwards, $I_{R1} = I_{R2}$ by OA
- 3. Brokaw, 1974: N1, N2 base connected, R2 shifted downwards
- 4. Simplified realization of Brokaw circuit, R1 = start resistance

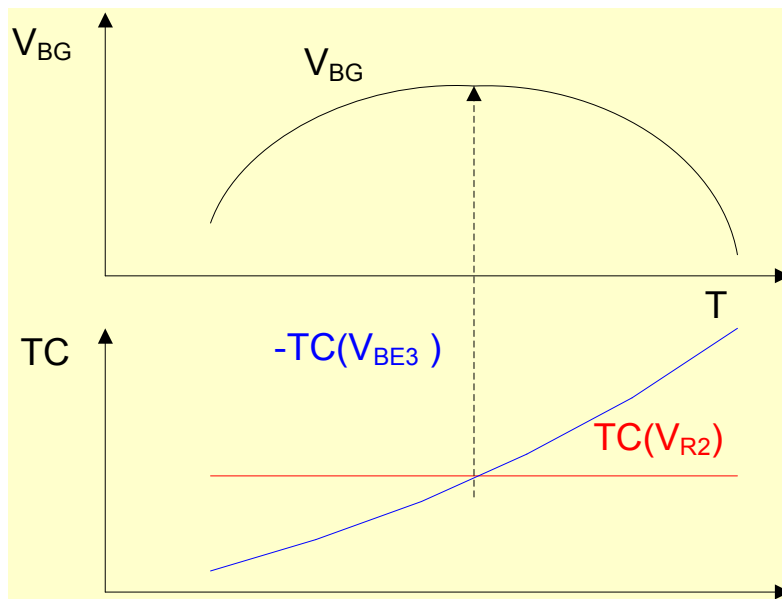


Bandgap reference basics

Bandgap voltage maximum



- Designer's goal is, to place the $V_{BG}(T)$ maximum at the temperature of normal device operating conditions
- Note: Maximum of $V_{BG}(T)$ appears at that point where the absolute values of the temperature coefficients of V_{R2} and V_{BE3} are equal



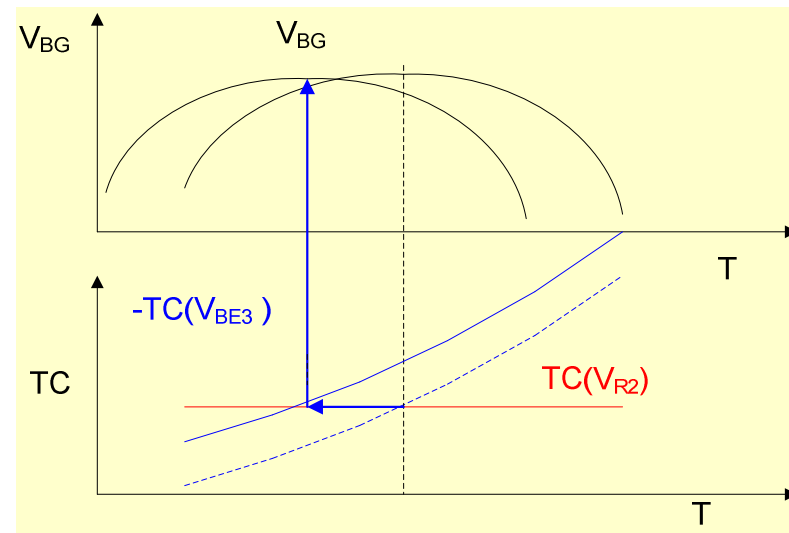
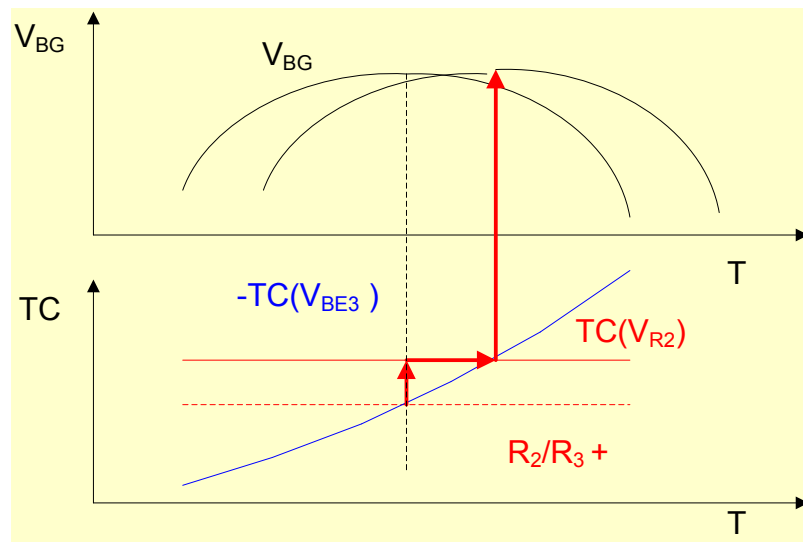
$$-TC(V_{BE3}) = TC(V_{R2})$$

Bandgap reference basics

Bandgap voltage maximum



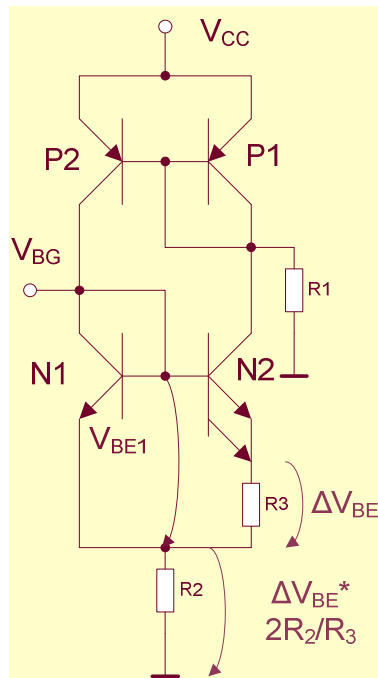
- Effect of an increase of the **positive** temperature coefficient
- Increase may be realized by increasing the ratio $r = R_2 / R_3$ or the ratio $a = A_{E2} / A_{E3}$
- Result: shift of the V_{BG} maximum towards higher temperatures
- Effect of increasing the **negative** temperature coefficient
- This may be realized by decreasing the collector current density of T_3 (changing I_{CT3} or A_{ET3})
- Result: shift of the V_{BG} maximum towards lower temperatures



Bandgap reference basics

PTAT current

- PTAT = **P**roportional **T**o **A**bsolute **T**emperature
- In all Bandgap circuits, the current through R3 is PTAT, because it is defined by ΔV_{BE}
- In a Widlar diode I_{CT2} is proportional to absolute temperature (PTAT) because the current is defined by ΔV_{BE} , which is PTAT
- If $R_1 = R_2$ and $I_{CT1} = I_{CT2} = I_{CT3}$, this is valid for I_{CT1} too



$$I_{CT2} = \frac{V_{R3}}{R_3} = \frac{\Delta V_{BE}}{R_3}$$

$$\Delta V_{BE} = \frac{kT}{q} \ln \left[\frac{I_{S_{T2}}}{I_{S_{T1}}} \right]$$

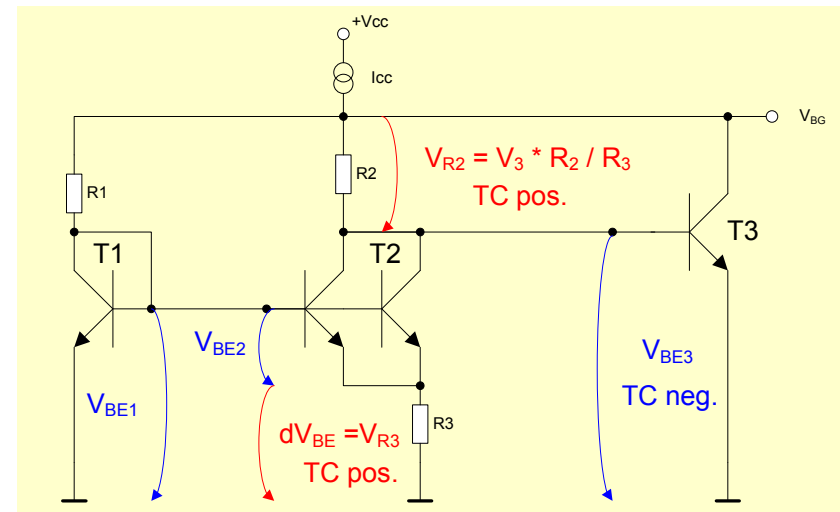


Table of contents

- **Bandgap reference basics**

- **Bandgap reference error sources**

- **Summary**

- **Appendix**

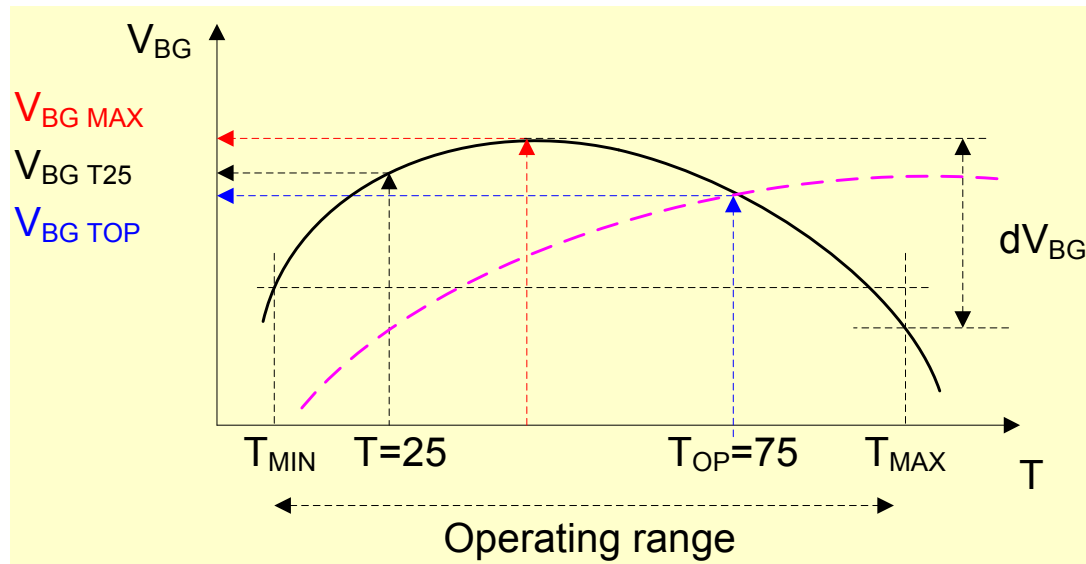
Bandgap reference error sources

Criteria for bandgap evaluation



To evaluate a Bandgap simulation or measurement result, we need a definition of the criteria

- Evaluating DC results we may use:
 1. Bandgap voltage at V_{BG} @ $T=T_{OP}$ or $T=25$
 2. Locus of V_{BGmax}
 3. V_{BG} temperature coefficient $TC_{V_{BG}}$ (in ppm)
- Other important Bandgap criteria from designers point of view are:
 1. Power supply voltage rejection $PSRR = dV_{BG} / dV_{CC}$
 2. Current consumption
 3. Dynamic behavior: switch on time, stability
 4. Noise behavior

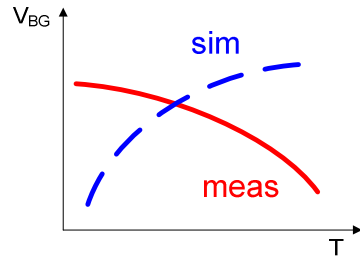


$$TC_{V_{BG}} = \frac{(V_{BG\ MAX} - V_{BG\ MIN})}{(T_{MAX} - T_{MIN})} \cdot \frac{1}{V_{BG}(T = 25)}$$

Need to talk about the same things, that is, to use the same definitions

Bandgap reference error sources

Problem definition



Problem: simulated and measured Bandgap voltage are different

Designers conclusion is often: the transistor model is wrong!

Request: improved device models



If a problem is defined, the solution is half-on way

(J.Huxley, Biologist, 1897-1975)

Task: Identify the error sources in BG design

First, we have to distinguish:

The problem appears for a

packaged device

on wafer device

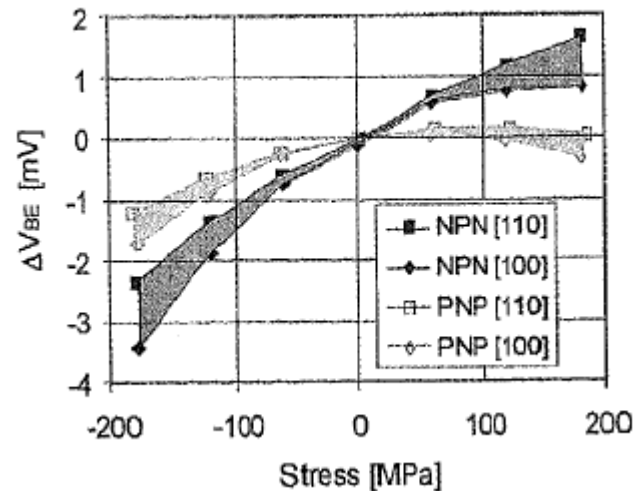
Bandgap reference error sources

Mechanical stress

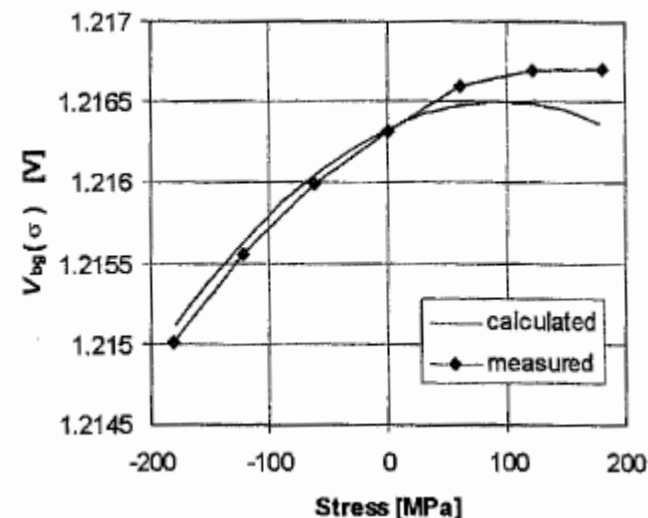


- “Mechanical stress is the main cause of long term drift and package induced inaccuracy in band reference voltages”
- Reason: piezjunction effect changes both mobility and intrinsic carrier concentration in the base
- Result: change in IS resp. VBE in the order of -3 mV to +2 mV (calculated)
- VBG is changed by 1.7 mV for a CMOS bandgap

Source: Fruett et.al. SSC, vol.38, No.7, July 2003, p.1288 ...



5mV

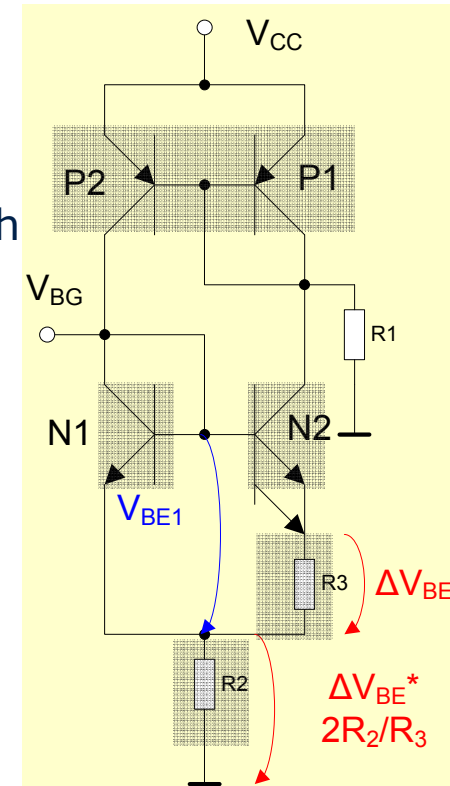


1.7 mV

Bandgap reference error sources

Mismatch effects

- Considering the right hand side Bandgap cell, we may identify six error sources:
 1. pnp mirror mismatch, caused by I_B and Early effect
 2. R2 and R3 absolute resistor tolerance (changes the branch currents, but not the ratio $R2 / R3$)
 3. R2 and R3 resistor mismatch (changes the ratio $R2 / R3$)
 4. R2 and R3 absolute TC (changes the absolute value of R2 and R3 and in this way the branch currents)
 5. R2 and R3 mismatch of TC (changes the ratio of $R2 / R3$)
 6. I_C mismatch of N1 and N2, caused e.g. by emitter size mismatch (creates a additional delta V_{BE})



“It has been found, that resistor tolerances and current mirror mismatch are the dominant sources of error in bandgap circuits”

(Source: Gupta, MSCS 2002, p. III-575...)

Bandgap reference error sources

SGP model parameters



- Which SGP model parameters are important for bandgap simulation?

1. IS
2. XTI
3. EG
4. XTB
5. VAR

$$I_C(T) = IS(T_0) \left(\frac{T}{T_0} \right)^m \exp \left[-\frac{V_g}{kT/q} \left(1 - \frac{T}{T_0} \right) \right] \exp \left[\frac{V_{BE}}{kT/q} \right]$$

- Staveren (TCS, 1996, pp.418) investigated for a Si-technology the effect of VAR on VBG and found an error in the order of 10 mV

$$V_{Error} = \frac{V_T}{VAR} * V_{REF}$$

$$V_{Error} = \frac{26mV}{2.6V} 1.2V = 12mV$$

THE INFLUENCE OF THE V_{AR} ON THE TEMPERATURE BEHAVIOR

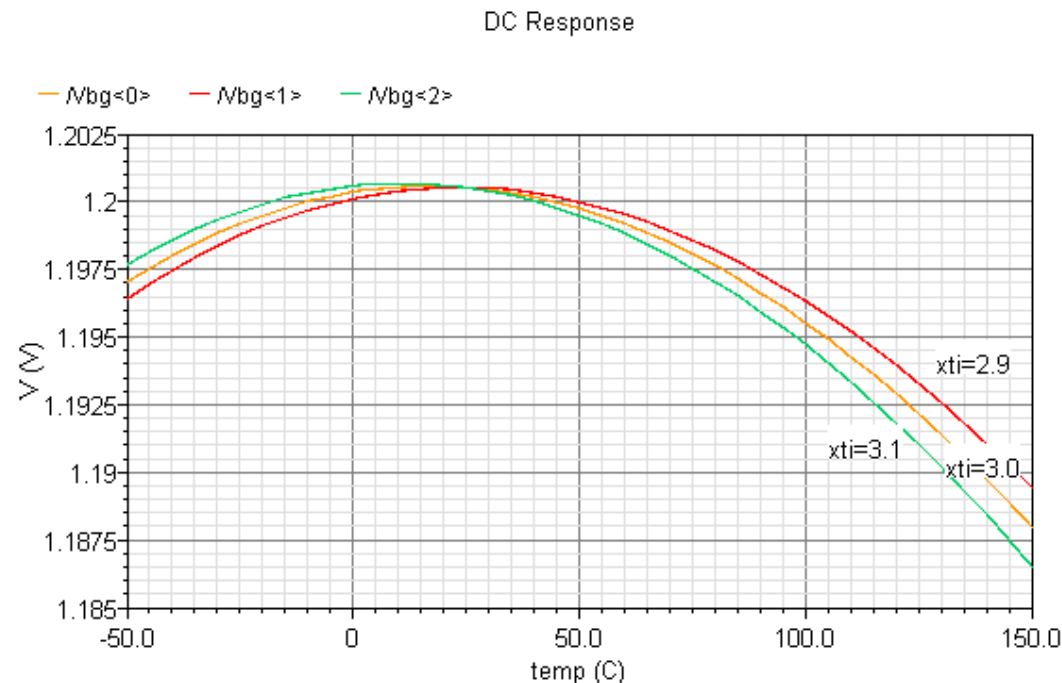
Case	Mean error
$V_{AR} = \infty$, no influence of the reverse Early effect	19 ppm/K
$V_{AR} = 4V$ and not taken into account	30 ppm/K
$V_{AR} = 4V$ and taken into account	20 ppm/K

Bandgap reference error sources

SGP model parameters: Effect of XTI



- Increasing XTI results in an increasing $TC(V_{BET3})$, -TC component of the Widlar circuit is enlarged and the maximum is shifted to lower temperatures (green curve)
- Decreasing XTI results in a decreasing $TC(V_{BET3})$, -TC component of the Widlar circuit is reduced and the maximum is shifted to higher temperatures (red curve)



Bandgap reference error sources

SGP model parameters: Effect of EG



- Increasing EG results in an increasing $TC(V_{BET3})$, -TC component is enlarged and the maximum is shifted to lower temperatures (green curve)
- Decreasing EG results in an decreasing $TC(V_{BET3})$, -TC component of the Widlar circuit is reduced and the maximum is shifted to lower temperatures (red curve)

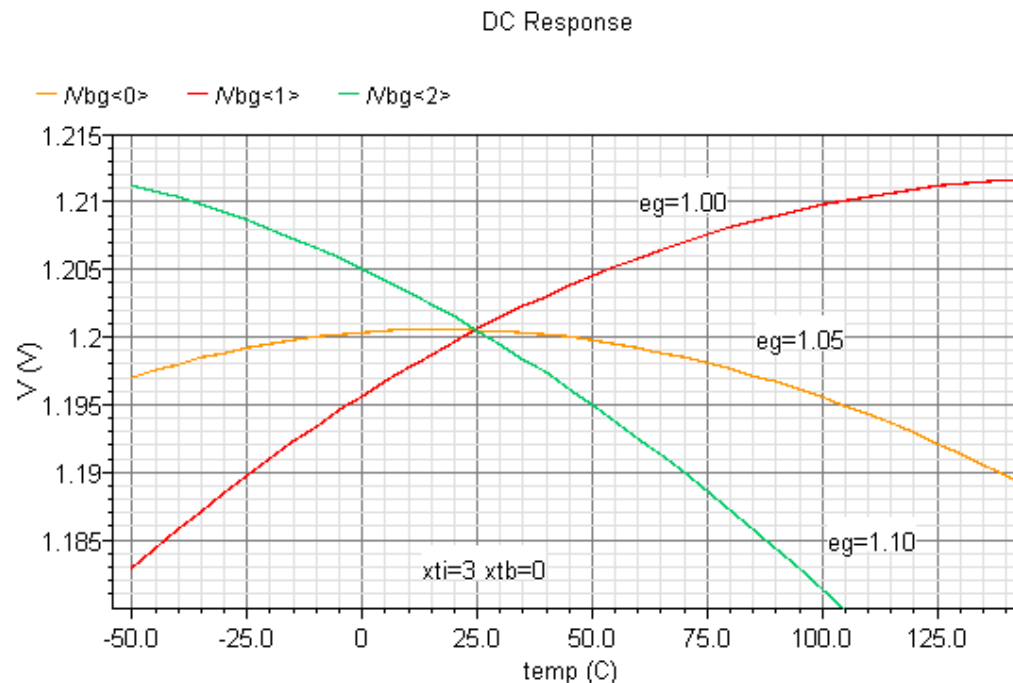


Table of contents

- **Bandgap reference basics**

- **Bandgap reference error sources**

- **Summary**

- **Appendix**

Summary

There are different possible reasons for Bandgap simulation and measurement errors:

- for packaged devices: mechanical stress
- for on wafer circuits:
 1. pnp mirror mismatch
 2. R2 and R3 tolerance and mismatch, TC tolerance and mismatch
 3. npn IC matching and
 4. npn IC(T) modeling (EG, XTI, XTB, IS, VAR)

To evaluate these effects on bandgap simulation results it is necessary to

1. use special bandgap modeling test circuits, which allow to separate these effects
2. apply improved extraction methods for EG, XTI (e.g. proposed by Beckrich et.al. at CMRF2004)

Table of contents

- **Bandgap reference basics**

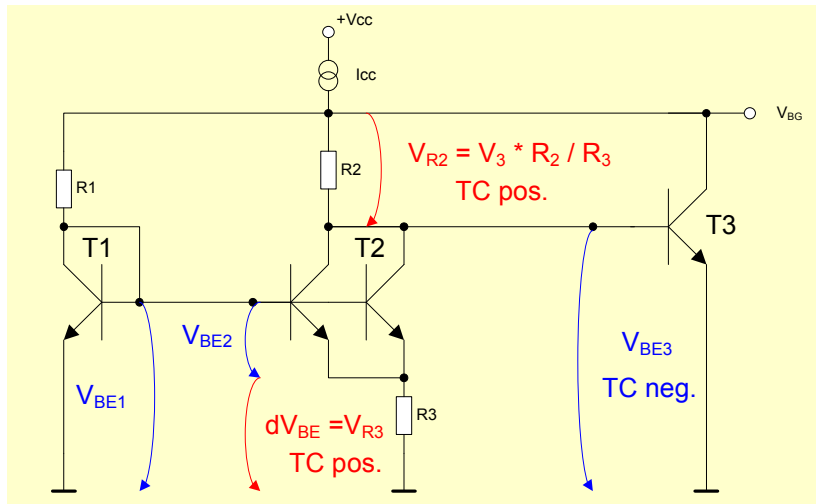
- **Bandgap reference error sources**

- **Summary**

- **Appendix**

Appendix Widlar Bandgap dimensioning

■ How to choose R3?



- Example:
choosing $i=1$ and $a=8$ we get
 $\Delta V_{BE} = 54 \text{ mV}$
- Setting I_{R3} we may calculate R3

$$i = \frac{I_{C1}}{I_{C2}}$$

$$a = \frac{A_{E2}}{A_{E1}} = \frac{IS_{T2}}{IS_{T1}}$$

$$\Delta V_{BE} = V_T \ln \left[\frac{I_{CT1}}{IS_{T1}} \cdot \frac{IS_{T2}}{I_{CT2}} \right] = V_T \ln[a * i]$$

$$R_3 = \frac{54 \text{ mV}}{20 \mu\text{A}} = 2.7 \text{ kOhm}$$

Appendix

Widlar Bandgap dimensioning



- How to choose R2?
- We want now to compensate the negative TC of VBE3 adding a voltage with a positive TK, which may be created by ΔV_{BE} multiplied with a factor $r = R2 / R3$
- The TC of both terms should cancel each other
- We have to choose R2 appropriate, to reach the necessary gain factor g

$$V_{BG} = \underbrace{V_{BE}}_{neg.TC} + r \cdot \underbrace{\Delta V_{BE}}_{pos.TC}$$

$$-\frac{dV_{BE}}{dT} \approx \frac{d(r \cdot \Delta V_{BE})}{dT} = r \cdot \ln(i * a) \frac{dV_T}{dT}$$

with

r = resistor ratio

i = collector current ratio

a = emitter area ratio

$$g = r \cdot \ln(i * a) = \frac{\left(-\frac{dV_{BE}}{dT} \right)}{\left(\frac{k}{q} \right)}$$

- How to choose R1?
- In practice R1=R2 is proven as useful

$$g = r \cdot \ln(i * a) = \frac{1.1mV / K}{0.08614mV / K} = 12.77$$

Appendix

Widlar Bandgap dimensioning



■ Example calculation for r using different TC(VBE)

TC_vbe	k	q	k_q	g	i	a	ln_ia	r
-1.00E-03	1.38E-23	1.602E-19	8.6E-05	11.61	1	4	1.39	8.37
-1.50E-03	1.38E-23	1.602E-19	8.6E-05	17.41	1	4	1.39	12.56
-2.00E-03	1.38E-23	1.602E-19	8.6E-05	23.22	1	4	1.39	16.75
-1.00E-03	1.38E-23	1.602E-19	8.6E-05	11.61	1	8	2.08	5.58
-1.10E-03	1.38E-23	1.602E-19	8.6E-05	12.77	1	8	2.08	6.14
-1.50E-03	1.38E-23	1.602E-19	8.6E-05	17.41	1	8	2.08	8.37
-2.00E-03	1.38E-23	1.602E-19	8.6E-05	23.22	1	8	2.08	11.17