Bipolar Working Group Meeting
NXP in Hamburg

A brief introduction

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Hamburg, 30.10.2008
My personality and professional history

- **1955 - Born** in Berlin

- **1977 - Electrical Engineering Study** at “Ingenieurhochschule Wismar”
  - Finished with the degree of “Diplom-Ingenieur” for communication techniques

- **1981 - Work at “Institut für Nachrichtentechnik”**
  - Chip Designs in various technologies (Analog Bipolar, I²L and ECL) for special communication circuits, e.g., PCM-Repeaters, Controllers and Subscriber Line Interface Circuits (SLIC)
  - Circuit simulations with Spice-like tools, implemented transistor models were Ebers-Moll, later, with more computing power, the Gummel-Poon Model
My personality and professional history

- **1990 - Take over to the Research Center of Alcatel-SEL AG, Stuttgart**
  - Work on various chip designs in fast Bipolar- and BiCMOS technologies from different semiconductor fabs (IBM, Infineon, ST, TEMIC)
  - Work on Transceiver chips for SDH-Transmission-Systems (622 Mbit/s), Laser Drivers, A/D Converter for Cable-TV (2.5 Gbit/s), AGC with TIA (12 Gbit/s), Mux/Demux-IC’s (12 Gbit/s)
  - Simulations with HSpice, Spectre, Layout and Verification with Cadence Tools

- **Now - Alcatel-Lucent Deutschland AG, Bell Labs Germany**
  - Work on IC-designs for high speed optical transmission systems up to 110 Gbit/s in the frame of the 100GET project
  - Various chip developments as Electronic Equalizers (LE, DFE), fast DFF’s, Multiplexers for 55 Gbit/s up to 110 Gbit/s and a 43 Gs/s ADC with 3 bit resolution for present research tasks
Design Example Linear Equalizer for 43 Gbit/s

Linear equalizer

5-tap feed-forward equaliser
Taps: 4-quadrant multipliers
Delay by linear amplifiers
Fractionally spaced
Single-ended data input
Differential data output
CML architecture
Chip area 2.0 x 1.5 mm²

Architecture of the LE
C1,…C5: tap coefficients

"43 Gbit/s SiGe Based Electronic Equalizer for PMD and Chromatic Dispersion Mitigation"
B. Franz (1), D. Rössener (1), R. Dischler (1), F. Buchali (1), B. Junginger (1), T.F. Meister (2),
K. Aufinger (2), We1.3.1, ECOC 2005, Glasgow
Design Example Multiplexer for 85 Gbit/s

Application within worldwide first binary 85 Gbit/s ETDM system

85.32 Gb/s output signal of 2:1 MUX
measured on-wafer

Ver.: 100mV/div, hor. 5 ps/div, 70 GHz sampling scope

"85.4 Gbit/s ETDM Transmission over 401 km SSMF Applying UFEC",
K. Schuh, B. Junginger, H. Rempp, P. Klose, D. Rösener, E. Lach,
Post-deadline paper Th4.1.4, ECOC 2005, Glasgow
Simulation Aspects

- All circuit simulations of high speed transistors were made with SGP models

- Some problems with SGP:
  - Insufficient high frequency behavior at high current densities (e.g. further $f_T$ increase at higher currents)
  - Self heating isn’t modeled (e.g. operating point drifts in dependence of the signal pattern can’t be simulated)
  - No Avalanche-Effect (Problem with ultra high speed transistors in the range between the breakdown voltages $BV_{CEO}$ and $BV_{CES}$)
  - No parasitic substrate transistor (additional currents into the substrate are neglected)
Thank you for your interest!

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